


<p align="center"><b>TEST REPORT</b>  <b>EN IEC 62680-1-2</b>  <b>Universal serial bus interfaces for data and power</b>  <b>Part 1-2: Common components USB Power Delivery specification</b>  <b>EN IEC 62680-1-3</b>  <b>Universal serial bus interfaces for data and power</b>  <b>Part 1-3: Common components — USB</b>  <b>Type-C(r) cable and connector specification</b></p>	
Report Number.....	TCT250208S001
Date of issue.....	2025-03-05
Total number of pages .....	215 pages (not included attachments)
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<b>Test specification:</b>	
Standard .....	EN IEC 62680-1-2:2022 EN IEC 62680-1-3:2022
Test procedure .....	Type-test
Non-standard test method .....	N/A
Test Report Form No. ....	62680_1_2B 62680_1_3B
Test Report Form(s) Originator ....	TCT
Master TRF .....	Dated 2024-10-09
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<b>Test item description</b> ..... :	Smartphone	
<b>Trade Mark</b> ..... :	CUBOT	
<b>Manufacturer</b> .....	same as applicant	
<b>Model/Type reference</b> .....	KINGKONG POWER 5	
<b>Rating</b> .....	DC5.0V,3.0A,DC9.0V,3.0A,DC12.0V,2.75A	
<b>Testing Laboratory:</b> Shenzhen TCT Testing Technology Co., Ltd.		
Testing location/ address .....	TCT testing Industrial Park, Fuqiao 5th Industrial Zone, Fuhai Street, Bao'an District, Shenzhen	
<b>Tested by (name, function + signature)</b> ..... :	Kevin Li	
<b>Approved by (name, function + signature)</b> ..... :	Ringko.Shi	
<b>Testing procedure: CTF Stage 1</b>		
Testing location/ address .....		
<b>Tested by (name, function + signature)</b> ..... :		
<b>Approved by (name, function + signature)</b> ..... :		
<b>Testing procedure: CTF Stage 2</b>		
Testing location/ address .....		
<b>Tested by (name, function + signature)</b> ..... :		
<b>Witnessed by (name, function + signature):</b>		
<b>Approved by (name, function + signature)</b> ..... :		
<b>Testing procedure: CTF Stage 3:</b>		
<b>Testing procedure: CTF Stage 4:</b>		
Testing location/ address .....		
<b>Tested by (name, function + signature)</b> ..... :		
<b>Witnessed by (name, function + signature):</b>		
<b>Approved by (name, function + signature)</b> ..... :		
<b>Supervised by (name, function + signature):</b>		

<b>List of Attachments (including a total number of pages in each attachment):</b> Attachment NO.1: GRL-USB-PD Compliance Test Solution, 109 pages. Attachment NO.2: Photo documentation, 3 pages.	
<b>Summary of testing:</b>	
<b>Tests performed (name of test and test clause):</b> All applicable testes.	<b>Testing location:</b> See above for details.

**Copy of marking plate:**

**The artwork below may be only a draft. The use of certification marks on a product must be authorized by the respective NCBs that own these marks.**

N/A

<b>Test item particulars</b> .....:
<b>Classification of installation and use</b> .....: --
<b>Supply Connection</b> .....: Type C -port
<b>Possible test case verdicts:</b> - test case does not apply to the test object.....: N/A - test object does meet the requirement.....: P (Pass) - test object does not meet the requirement.....: F (Fail)
<b>Testing</b> .....:
<b>Date of receipt of test item</b> .....: 2025-02-08
<b>Date (s) of performance of tests</b> .....: 2025-02-14 to 2025-02-14
<b>General remarks:</b> "(See Enclosure #)" refers to additional information appended to the report. "(See appended table)" refers to a table appended to the report. Note: All reference Table and Figure are shown in the original standard <b>Throughout this report a <input type="checkbox"/> comma / <input checked="" type="checkbox"/> point is used as the decimal separator.</b>
<b>When differences exist; they shall be identified in the General product information section.</b>
<b>Name and address of factory (ies)</b> .....: same as applicant
<b>General product information:</b> 1. The specified Maximum ambient temperature is 25°C, and apparatus used in door only. 2. According to EN IEC 62680-1-3:2022-USB Type-C Cable and Connector Specification which released by TTL: B23N01590-REC

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Clause	Requirement + Test	Result - Remark	Verdict

<b>3</b>	<b>Mechanical</b>		N/A
<b>3.1</b>	<b>Overview</b>		N/A
	This chapter defines the USB Type-C® connectors and wired cable assemblies. Cables which include active elements in the data path are defined in Chapter 6 (Active Cables).		N/A
<b>3.1.1</b>	<b>Compliant Connectors</b>		N/A
	The USB Type-C specification defines the following standard connectors:		N/A
	USB Full-Featured Type-C receptacle		N/A
	USB 2.0 Type-C receptacle		N/A
	USB Full-Featured Type-C plug		N/A
	USB 2.0 Type-C plug		N/A
	USB Type-C Power-Only plug		N/A
<b>3.1.2</b>	<b>Compliant Cable Assemblies</b>		N/A
	Table 3-1 summarizes the USB Type-C standard cable assemblies along with the primary differentiating characteristics. All USB Full-Featured Type-C cables shall support simultaneous, independent signal transmission on both USB 3.2 and USB4™ (TX and RX pairs) data buses. For USB Power Delivery, each cable assembly is identified as being either only usable for Standard Power Range (SPR) operation or usable for both SPR and Extended Power Range (EPR) operation. Existing SPR 5 A cables are being deprecated and replaced by EPR cables. All cables that are either full-featured and/or are rated at more than 3A current are Electronically Marked Cables.		N/A
	USB Type-C products are also allowed to have a captive cable. See Section 3.4.3.		N/A
<b>3.1.3</b>	<b>Compliant USB Type-C to Legacy Cable Assemblies</b>		N/A
	Table 3-2 summarizes the USB Type-C legacy cable assemblies along with the primary differentiating characteristics. The cable lengths listed in the table are informative and represents the practical length based on cable performance requirements. USB 3.2 Type-C legacy cables assemblies that only offer performance up to USB 3.1 Gen1 are not allowed by this specification. All USB Type-C to legacy cable assemblies are only defined specific to USB 2.0 and USB 3.2 as there are no USB Type-C to legacy cables that are uniquely applicable to USB4.		N/A

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	For USB Type-C legacy cable assemblies that incorporate Rp termination, the value of this termination is required to be specified to the Default setting of USB Type-C Current even though the cable assemblies are rated for 3 A. The Rp termination in these cables is intended to represent the maximum current of a compliant legacy USB host port, not the current rating of the cable itself. The cable current rating is intentionally set to a higher level given that there are numerous non-standard power chargers that offer more than the Default levels established by the USB 2.0 and USB 3.1 specifications.		N/A
<b>3.1.4</b>	<b>Compliant USB Type-C to Legacy Adapter Assemblies</b>		N/A
	Table 3-3 summarizes the USB Type-C legacy adapter assemblies along with the primary differentiating characteristics. The cable lengths listed in the table are informative and represents the practical length based on cable performance requirements. All USB Type-C to legacy adapter assemblies are only defined specific to USB 2.0 and USB 3.2 as there are no USB Type-C to legacy adapters that are uniquely applicable to USB4.		N/A
<b>3.2</b>	<b>USB Type-C Connector Mating Interfaces</b>		N/A
	This section defines the connector mating interfaces, including the connector interface drawings, pin assignments, and descriptions. All dimensions in figures are in millimeters		N/A
<b>3.2.1</b>	<b>Interface Definition</b>		N/A
	Figure 3-1 and Figure 3-3 show, respectively, the USB Type-C receptacle and USB Full-Featured Type-C plug interface dimensions.		N/A
	Figure 3-11 shows the USB 2.0 Type-C plug interface dimensions. The dimensions that govern the mating interoperability are specified. All the REF dimensions are provided for reference only, not hard requirements.		N/A
	Key features, configuration options, and design areas that need attention:		N/A
	1. Figure 3-1 shows a vertical-mount receptacle. Other PCB mounting types such as right-angle mount and mid-mount are allowed.		N/A
	2. A mid-plate is required between the top and bottom signals inside the receptacle tongue to manage crosstalk in full-featured applications. The mid-plate shall be connected to the PCB ground with at least two grounding points. The mid-plate shall be designed such that plug pins A4, A5, A6, A7, A8, A9, and B4, B5, B6, B7, B8, B9 do not short to ground during the connector mating process with an effective 6.2 mm		N/A

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	receptacle shell implementation. If the receptacle connector has a short shell or no shell, the connector manufacturer shall provide an effective length shell fixture for compliance testing. A reference design of the mid-plate is provided in Section 3.2.2.1.		
	3. Retention of the cable assembly in the receptacle is achieved by the side-latches in the plug and features on the sides of the receptacle tongue. Side latches are required for all plugs except plugs used for docking with no cable attached. Side latches shall be connected to ground inside the plug. A reference design of the side latches is provided in Section 3.2.2.2 along with its grounding scheme. Docking applications may not have side latches, requiring special consideration regarding EMC (Electromagnetic Compatibility).		N/A
	4. The EMC shielding springs are required inside the cable plug. The shielding spring shall be connected to the plug shell. No EMC shielding spring finger tip of the USB Full-Featured Type-C plug or USB 2.0 Type-C plug shall be exposed in the plug housing opening of the unmated USB Type-C plug (see Figure 3-12). Section 3.2.2.3 shows reference designs of the EMC spring.		N/A
	5. Shorting of any signal or power contact spring to the plug metal shell is not allowed. The spring in the deflected state should not touch the plug shell. An isolation layer (e.g., Kapton tape placed on the plug shell) is recommended to prevent accidental shorting due to plug shell deformation.		N/A
	6. The USB Type-C receptacle shall provide an EMC ground return path through one of the following options:		N/A
	a system of specific points of contact on the receptacle outer shell (e.g., spring fingers or spring fingers and formed solid bumps),		N/A
	internal EMC pads, or		N/A
	a combination of both points of contact on the receptacle outer shell and internal EMC pads.		N/A
	If points of contacts are used on the receptacle, then the receptacle points of contact shall make connection with the mated plug within the contact zones defined in Figure 3-2. A minimum of four separate points of contact are required. Additional points of contact are allowed. See Section 3.2.2.4 for a reference design of receptacle outer shell. The reference design includes four spring fingers as points of contact. Alternate configurations may include spring fingers on the A contact side or B contact side and formed solid bumps (e.g., dimples) on the		N/A



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	B contact side or A contact side, respectively. Spring fingers are required on a minimum of one side to provide a pressure fit on opposing sides of the plug shell. Additional bumps may be used, but if bumps are on opposing sides of the receptacle shell, the minimum distance between the bumps shall be greater than the maximum plug shell defined dimension.		
	If internal EMC pads are present in the receptacle, then they shall comply with the requirements defined in Figure 3-1. The shielding pads shall be connected to the receptacle shell. If no receptacle shell is present, then the receptacle shall provide a means to connect the shielding pad to ground. See Section 3.2.2.3 for a reference design of the shielding pad and ground connection.		N/A
	7. This specification defines the USB Type-C receptacle shell length of 6.20 mm as a reference dimension. The USB Type-C receptacle is designed to have shell length of $6.20 \pm 0.20$ mm to provide proper mechanical and electrical mating of the plug to the receptacle (e.g., full seating of the plug in the receptacle and protection of the receptacle tongue during insertion/withdrawal). The USB Type-C receptacle at the system level should be implemented such that the USB Type-C receptacle connector mounted in the associated system hardware has an effective shell length equal to $6.20 \pm 0.20$ mm.		N/A
	8. The USB Type-C connector mating interface is defined so that the electrical connection may be established without the receptacle shell. To prevent excessive misalignment of the plug when it enters or exits the receptacle, the enclosure should have features to guide the plug for insertion and withdrawal when a modified receptacle shell is present. If the USB Type-C receptacle shell is modified from the specified dimension, then the recommended lead in from the receptacle tongue to the plug point of entry is 1.5 mm minimum when mounted in the system. This specification allows receptacle configurations with a conductive shell, a nonconductive shell, or no shell. The following requirements apply to the receptacle contact dimensions shown in SECTION A-A and ALTERNATE SECTION A-A shown in Figure 3-1:		N/A
	If the receptacle shell is conductive, then the receptacle contact dimensions of SECTION A-A or ALTERNATE SECTION A-A shown in Figure 3-1 shall be used.		N/A
	If the receptacle shell is non-conductive, then		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	the receptacle contact dimensions of ALTERNATE SECTION A-A shown in Figure 3-1 shall be used. The contact dimensions of SECTION A-A are not allowed.		
	If there is no receptacle shell, then the receptacle contact dimensions of either SECTION A-A or ALTERNATE SECTION A-A shown in Figure 3-1 shall be used. If there is no receptacle shell and the receptacle is used in an implementation that does not effectively provide a conductive shell, then a receptacle with the contact dimensions of ALTERNATE SECTION A-A shown in Figure 3-1 should be used.		N/A
	9. A paddle card (e.g., PCB) may be used in the USB Type-C plug to manage wire termination and electrical performance. Section 3.2.2.5 includes the guidelines and a design example for a paddle card.		N/A
	10. This specification does not define standard footprints. Figure 3-4 shows an example SMT (surface mount) footprint for the vertical receptacle shown in Figure 3-1. Additional reference footprints and mounting configurations are shown in Figure 3-5, Figure 3-6, Figure 3-7, Figure 3-8, Figure 3-9 and Figure 3-10.		N/A
	11. The receptacle shell shall be connected to the PCB ground plane.		N/A
	12. All VBUS pins shall be connected together in the USB Type-C plug.		N/A
	13. All Ground return pins shall be connected together in the USB Type-C plug.		N/A
	14. All VBUS pins shall be connected together at the USB Type-C receptacle when it is in its mounted condition (e.g., all VBUS pins bussed together in the PCB).		N/A
	15. All Ground return pins shall be connected together at the USB Type-C receptacle when it is in its mounted condition (e.g., all Ground return pins bussed together in the PCB).		N/A
	16. The USB Type-C Power-Only plug is a depopulated version of the USB Full-Featured Type-C plug or the USB 2.0 Type-C plug. The interface dimensions shall conform to Figure 3-3 or Figure 3-11. Contacts for CC, VBUS, and GND (i.e., A1, A4, A5, A9, A12, B1, B4, B9, and B12) shall be present. Physical presence of contacts in the other 15 contact locations is optional. The USB Type-C Power-Only plug shall only be used on a non-charger captive cable application. Implementation of Rd or CC communication on pin A5 is required in the application.		N/A

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	Figure 3-7 Reference Footprint for a USB Type-C Mid-Mount Dual-Row SMT Receptacle (Informative)		N/A
	Only the contacts necessary to support USB PD and USB 2.0 are required in the plug. All other pin locations may be unpopulated. See Table 3-5. All contacts are required to be present in the mating interface of the USB Type-C receptacle connector.		N/A
	Unlike the USB Full-Featured Type-C plug, the internal EMC springs may be formed from the same strip as the signal, power, and ground contacts. The internal EMC springs contact the inner surface of the plug shell and mate with the receptacle EMC pads when the plug is seated in the receptacle. Alternately, the USB 2.0 Type-C plug may use the same EMC spring configuration as defined for the USB Full-Featured Type-C plug. The USB 2.0 Type-C plug four EMC spring locations are defined in Figure 3-11. The alternate configuration using the six spring locations is defined in Figure 3-1. Also refer to the reference designs in 3.2.2.3 for further clarification.		N/A
	A paddle card inside the plug may not be necessary if wires are directly attached to the contact pins.		N/A
<b>3.2.2</b>	<b>Reference Designs</b>		N/A
	This section provides reference designs for a few key features of the USB Type-C connector. The reference designs are provided as acceptable design examples. They are not normative.		N/A
<b>3.2.2.1</b>	<b>Receptacle Mid-Plate (Informative)</b>		N/A
	The signals between the top and bottom of the receptacle tongue are isolated by a mid-plate inside the tongue. Figure 3-13 shows a reference design of the mid-plate. It is important to pay attention to the following features of the middle plate:		N/A
	The distance between the signal contacts and the mid-plate should be accurately controlled since the variation of this distance may significantly impact impedance of the connector.		N/A
	The mid-plate in this particular design protrudes slightly beyond the front surface of the tongue. This is to protect the tongue front surface from damage caused by missinsertion of small objects into the receptacle.		N/A
	The mid-plate is required to be directly connected to the PCB ground with at least two grounding points.		N/A
	The sides of the mid-plate mate with the plug side latches, making ground connections to		N/A

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	reduce EMC. Proper surface finishes are necessary in the areas where the side latches and mid-plate connections occur.		
3.2.2.2	Side Latch (informative)		N/A
	The side latches (retention latches) are located in the plug. Figure 3-14 shows a reference design of a blanked side latch. The plug side latches should contact the receptacle mid-plate to provide an additional ground return path.		N/A
3.2.2.3	Internal EMC Springs and Pads (Informative)		N/A
	Figure 3-16 is a reference design of the internal EMC spring located inside the USB Full-Featured Type-C plug. Figure 3-17 is a reference design of the internal EMC spring located inside the USB 2.0 Type-C plug.		N/A
	It is critical that the internal EMC spring contacts the plug shell as close to the EMC spring mating interface as possible to minimize the length of the return path.		N/A
	The internal EMC pad (i.e., ground plate) shown in Figure 3-18 is inside the receptacle. It mates with the EMC spring in the plug. To provide an effective ground return, the EMC pads should have multiple connections with the receptacle shell.		N/A
3.2.2.4	Optional External Receptacle EMC Springs (Informative)		N/A
	Some applications may use receptacles with EMC springs that contact the outside of the plug shell. Figure 3-19 shows a reference receptacle design with external EMC springs. The EMC spring contact landing zones for the fully mated condition are normative and defined in Section 3.2.1.		N/A
3.2.2.5	USB Full-Featured Type-C Plug Paddle Card (Informative)		N/A
	The use of a paddle card is expected in the USB Full-Featured Type-C Plug. Figure 3-20 illustrates the paddle card pin assignment and contact spring connection location for a USB Full-Featured Type-C plug. The following guidelines are provided for the paddle card design:		N/A
	The paddle card should use high performance substrate material. The recommended paddle card thickness should have a tolerance less than or equal to $\pm 10\%$ .		N/A
	The SuperSpeed USB traces should be as short as possible and have a nominal differential characteristic impedance of $85 \Omega$ .		N/A
	The wire attach should have two high speed differential pairs on one side and two other high-speed differential pairs on the other side, separated as far as practically allowed.		N/A

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	It is recommended that a grounded coplanar waveguide (CPWG) system be selected as a transmission line method.		N/A
	Use of vias should be minimized.		N/A
	VBUS pins should be bussed together on the paddle card.		N/A
	GND pins should be bussed together on the paddle card.		N/A
<b>3.2.3</b>	<b>Pin Assignments and Descriptions</b>		N/A
	The usage and assignments of the 24 pins for the USB Type-C receptacle interface are defined in Table 3-4.		N/A
	The usage and assignments of the signals necessary for the support of only USB 2.0 with the USB Type-C mating interface are defined in Table 3-5.		N/A
<b>3.3</b>	<b>Cable Construction and Wire Assignments</b>		N/A
	This section discusses the USB Type-C cables, including cable construction, wire assignments, and wire gauges.		N/A
<b>3.3.1</b>	<b>Cable Construction (Informative)</b>		N/A
	Figure 3-21 illustrates an example of USB Full-Featured Type-C cable cross-section, using micro-coaxial wires for TX/RX pairs. There are four groups of wires: USB D+/D- (typically unshielded twisted pairs (UTP)), TX/RX signal pairs (coaxial wires, twin-axial or shielded twisted pairs), sideband signal wires, and power and ground wires. In this example, the optional VCONN wire is shown whereas in Figure 3-22 the example is shown with the VCONN wire removed – the inclusion of VCONN or not relates to the implementation approach chosen for Electronically Marked Cables (See Section 4.9).		N/A
	The USB D+/D- signal pair is intended to transmit the USB 2.0 Low-Speed, Full-Speed and High-Speed signaling while the TX/RX signal pairs are used for either USB 3.2 or USB4 signaling. Shielding is needed for the TX/RX differential pairs for signal integrity and EMC performance.		N/A
<b>3.3.2</b>	<b>Wire Assignments</b>		N/A
	Table 3-6 defines the full set of possible wires needed to produce all standard USB Type-C cables assemblies. For some cable assemblies, not all of these wires are used. For example, a USB Type-C cable that only provides USB 2.0 functionality will not include wires 6–15.		N/A
	Table 3-7 defines the full set of possible wires needed to produce USB Type-C to legacy cable		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
	assemblies. For some cable assemblies, not all of these wires are needed. For example, a USB Type-C to USB 2.0 Standard-B cable will not include wires 5–10.		
<b>3.3.3</b>	<b>Wire Gauges and Cable Diameters (Informative)</b>		N/A
	This specification does not specify wire gauge. Table 3-8 and Table 3-9 list typical wire gauges for reference purposes only. A large gauge wire incurs less loss, but at the cost of cable diameter and flexibility. Multiple wires may be used for a single wire such as for VBUS or Ground. It is recommended to use the smallest possible wire gauges that meet the cable assembly electrical and mechanical requirements.		N/A
	To maximize cable flexibility, all wires should be stranded, and the cable outer diameter should be minimized as much as possible. A typical USB Full-Featured Type-C cable outer diameter may range from 4 mm to 6 mm while a typical USB 2.0 Type-C cable outer diameter may range from 2 mm to 4 mm. A typical USB Type-C to USB 3.1 legacy cable outer diameter may range from 3 mm to 5 mm.		N/A
<b>3.4</b>	<b>Standard USB Type-C Cable Assemblies</b>		N/A
	Two standard USB Type-C cable assemblies are defined and allowed by this specification. In addition, captive cables are allowed (see Section 3.4.3). Shielding (braid) is required to enclose all the wires in the USB Type-C cable. The shield shall be terminated to the plug metal shells. The shield should be physically connected to the plug metal shell as close to 360° as possible, to control EMC.		N/A
<b>3.4.1</b>	<b>USB Full-Featured Type-C Cable Assembly</b>		N/A
	Figure 3-23 shows a USB Full-Featured Type-C standard cable assembly.		N/A
	Table 3-10 defines the wire connections for the USB Full-Featured Type-C standard cable assembly.		N/A
<b>3.4.2</b>	<b>USB 2.0 Type-C Cable Assembly</b>		N/A
	A USB 2.0 Type-C standard cable assembly has the same form factor shown in Figure 3-23.		N/A
	Table 3-11 defines the wire connections for the USB 2.0 Type-C standard cable assembly.		N/A
<b>3.4.3</b>	<b>USB Type-C Captive Cable Assemblies</b>		N/A
	A captive cable assembly is a cable assembly that is terminated on one end with a USB Type-C plug and has a vendor-specific connect means (hardwired or custom detachable) on the opposite end. The cable assembly that is		N/A

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	hardwired is not detachable from the device.		
	The assembly wiring for captive USB Type-C cables follow the same wiring assignments as the standard cable assemblies (see Table 3-10 and Table 3-11) with the exception that the hardwired attachment on the device side substitutes for the USB Type-C Plug #2 end.		N/A
	The CC wire in a captive cable shall be terminated and behave as appropriate to the function of the product to which it is captive (e.g. host or device).		N/A
	A device (Sink, UFP or DRP) with a captive cable assembly shall respond to SOP' cable identity inquiries when the device either sinks higher than 3A current or supports USB4 operation. The physical location of the eMarker can be either within the captive cable or the device with the cable.		N/A
	This specification does not define how the hardwired attachment is physically done on the device side.		N/A
<b>3.4.4</b>	<b>USB Type-C Thumb Drive Assemblies</b>		N/A
	A thumb drive assembly is an assembly that incorporates a USB Type-C plug as its primary USB interface. This assembly does not functionally include a cable assembly.		N/A
	A thumb drive device (Sink, UFP or DRP) shall respond to SOP' cable identity inquiries when it either sinks higher than 3A current or supports USB4 operation.		N/A
<b>3.5</b>	<b>Legacy Cable Assemblies</b>		N/A
	To enable interoperability between USB Type-C-based products and legacy USB products, the following standard legacy cable assemblies are defined. Only the cables defined within this specification are allowed.		N/A
	Legacy cable assemblies that source power to a USB Type-C connector (e.g. a USB Type-C to USB Standard-A plug cable assembly and a USB Type-C plug to USB Micro-B receptacle adapter assembly) are required to use the Default USB Type-C Current Rp resistor (56 kΩ). The value of Rp is used to inform the Sink how much current the Source can provide. Since the legacy cable assembly does not comprehend the capability of the Source it is connected to, it is only allowed to advertise Default USB Type-C Current as defined by the USB 2.0, USB 3.1 and USB BC 1.2 specifications. No other Rp values are permitted because these may cause a USB Type-C Sink to overload a legacy power supply.		N/A
<b>3.5.1</b>	<b>USB Type-C to USB 3.1 Standard-A Cable Assembly</b>		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
3.5.2	USB Type-C to USB 2.0 Standard-A Cable Assembly		N/A
3.5.3	USB Type-C to USB 3.1 Standard-B Cable Assembly		N/A
3.5.4	USB Type-C to USB 2.0 Standard-B Cable Assembly		N/A
3.5.5	USB Type-C to USB 2.0 Mini-B Cable Assembly		N/A
3.5.6	USB Type-C to USB 3.1 Micro-B Cable Assembly		N/A
3.5.7	USB Type-C to USB 2.0 Micro-B Cable Assembly		N/A
3.6	Legacy Adapter Assemblies		N/A
	To enable interoperability between USB Type-C-based products and legacy USB products, the following standard legacy adapter assemblies are defined. Only the adapter assemblies defined in this specification are allowed.		N/A
3.6.1	USB Type-C to USB 3.1 Standard-A Receptacle Adapter Assembly		N/A
3.6.2	USB Type-C to USB 2.0 Micro-B Receptacle Adapter Assembly		N/A
3.7	Electrical Characteristics		N/A
	This section defines the USB Type-C raw cable, connector, and cable assembly electrical requirements, including signal integrity, shielding effectiveness, and DC requirements. Chapter 3.11.1 defines additional requirements regarding functional signal definition, host/device discovery and configuration, and power delivery.		N/A
	Unless otherwise specified, all measurements are made at a temperature of 15° to 35° C, a relative humidity of 25% to 85%, and an atmospheric pressure of 86 to 106 kPa and all Sparameters are normalized with an 85 $\Omega$ differential impedance.		N/A
3.7.1	Raw Cable (Informative)		N/A
	Informative raw cable electrical performance targets are provided to help cable assembly manufacturers manage the procurement of raw cable. These targets are not part of the USB Type-C compliance requirements. The normative requirement is that the cable assembly meets the performance characteristics specified in Sections 3.7.2 and 3.7.5.3.		N/A
	The differential characteristic impedance for shielded differential pairs is recommended to		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
	be $90\ \Omega \pm 5\ \Omega$ . The single-ended characteristic impedance of coaxial wires is recommended to be $45\ \Omega \pm 3\ \Omega$ . The impedance should be evaluated using a 200 ps (10%-90%) rise time; a faster rise time is not necessary for raw cable since it will make cable test fixture discontinuities more prominent.		
3.7.1.1	Intra-Pair Skew (Informative)		N/A
	The intra-pair skew for a differential pair is recommended to be less than 10 ps/m. It should be measured with a Time Domain Transmission (TDT) in a differential mode using a 200 ps (10%-90%) rise time with a crossing at 50% of the input voltage.		N/A
3.7.1.2	Differential Insertion Loss (Informative)		N/A
	Cable loss depends on wire gauges, plating and dielectric materials. Table 3-21 and Table 3-22 show examples of differential insertion losses.		N/A
3.7.2	<b>USB Type-C to Type-C Passive Cable Assemblies (Normative)</b>		N/A
	A USB Type-C to Type-C cable assembly shall be tested using a test fixture with the receptacle tongue fabricated in the test fixture. This is illustrated in Figure 3-33. The USB Type-C receptacles are not present in the test fixture. Hosts and devices should account for the additional signal degradation the receptacle introduces.		N/A
	The requirements are for the entire signal path of the cable assembly mated with the fixture PCB tongues, not including lead-in PCB traces. As illustrated in Figure 3-33, the measurement is between TP1 (test point 1) and TP2 (test point 2). Refer to documentation located at Cables and Connectors page on the USB-IF website for a detailed description of a standardized test fixture.		N/A
	The cable assembly requirements are divided into informative and normative requirements. The informative requirements are provided as design targets for cable assembly manufacturers. The normative requirements are the pass/failure criteria for cable assembly compliance.		N/A
3.7.2.1	Recommended TX/RX Passive Cable Assembly Characteristics (USB 3.2 Gen2 and USB4 Gen2)		N/A
	The recommended electrical characteristics defined in this section are informative design guidelines. Cable assemblies that do not meet these recommended electrical characteristics may still pass USB certification testing. Similarly,		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	cable assemblies that meet these recommended electrical characteristics may or may not pass USB certification testing.		
3.7.2.1.1	Differential Insertion Loss (Informative – USB 3.2 Gen2 and USB4 Gen2)		N/A
	Figure 3-34 shows the differential insertion loss limit for a USB 3.2 Gen2 or a USB4 Gen2 Type-C cable assembly, which is defined by the following vertices: (100 MHz, –2 dB), (2.5 GHz, –4 dB), (5.0 GHz, –6 dB), (10 GHz, –11 dB) and (15 GHz, –20 dB).		N/A
3.7.2.1.2	Differential Return Loss (Informative – USB 3.2 Gen2 and USB4 Gen2)		N/A
3.7.2.1.3	Differential Near-End and Far-End Crosstalk between TX/RX Pairs (Informative – USB 3.2 Gen2 and USB4 Gen2)		N/A
	Both the near-end crosstalk (DDNEXT) and far-end crosstalk (DDFEXT) are specified, as shown in Figure 3-36. The DDNEXT/DDFEXT limits are defined by the following vertices: (100 MHz, –40 dB), (5 GHz, –40 dB), (10 GHz, –35 dB), and (15 GHz, –32 dB).		N/A
3.7.2.1.4	Differential Crosstalk between USB D+/D– and TX/RX Pairs (Informative –USB 3.2 Gen2 and USB4 Gen2)		N/A
	The differential near-end and far-end crosstalk between the USB D+/D– pair and the TX/RX pairs should be managed not to exceed the limits shown in Figure 3-37. The USB D+/D– pair and the TX/RX pairs should be considered in the context of both an aggressor and a victim. It should also be considered that the D+/D– pair maximum frequency for similar tests is 1.2 GHz (see Table 3-31), but in this case the crosstalk on the D+/D– pair is extended to 7.5 GHz. The limits are defined by the following points: (100 MHz, –35 dB), (5 GHz, –35 dB), and (7.5 GHz, –30 dB).		N/A
3.7.2.2	Recommended TX/RX Passive Cable Assembly Characteristics (USB4 Gen3)		N/A
3.7.2.2.1	Differential Insertion Loss (Informative – USB4 Gen3)		N/A
	Figure 3-38 shows the recommended differential insertion loss limit for a USB4 Gen3 Type-C cable assembly, which is defined by the following vertices: (100 MHz, –1 dB), (2.5 GHz, –4.2 dB), (5.0 GHz, –6 dB), (10 GHz, –7.5 dB), (12 GHz, –9.3 dB), and (15 GHz, –11 dB).		N/A
3.7.2.2.2	Differential Return Loss (Informative – USB4 Gen3)		N/A
	The informative differential return loss mask is identical in Section 3.7.2.1.2.		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
3.7.2.2.3	Differential Near-End and Far-End Crosstalk between TX/RX Pairs (Informative – USB4 Gen3)		N/A
	The recommended near-end crosstalk (DDNEXT) and far-end crosstalk (DDFEXT) are defined in Section 3.7.2.1.3. To minimize crosstalk, it is important to optimize the paddle card and wire termination designs inside the cable plug.		N/A
3.7.2.2.4	Differential Crosstalk between USB D+/D– and TX/RX Pairs (Informative – USB4 Gen3)		N/A
	The informative near-end and far-end crosstalk between the USB D+/D– pair and the TX/RX pairs are the same as in Section 3.7.2.1.4.		N/A
3.7.2.3	Normative TX/RX Passive Cable Assembly Requirements (USB 3.2 Gen2 and USB4 Gen2)		N/A
	The integrated parameters are used for cable assembly compliance (except for insertion loss and differential-to-common-mode conversion) to avoid potential rejection of a functioning cable assembly that may fail the traditional S-parameters spec at a few frequencies.		N/A
3.7.2.3.1	Insertion Loss Fit at Nyquist Frequencies (Normative – USB 3.2 Gen2 and USB4 Gen2)		N/A
	The insertion loss fit at Nyquist frequency measures the attenuation of the cable assembly. To obtain the insertion loss fit at Nyquist frequency, the measured cable assembly differential insertion loss is fitted with a smooth function. A standard fitting algorithm and tool shall be used to extract the insertion loss fit at Nyquist frequencies.		N/A
	Figure 3-39 illustrates an example of a measured cable assembly insertion loss fitted with a smooth function; the insertion loss fit at the Nyquist frequency of SuperSpeed USB Gen2 (5.0GHz) is –5.8 dB.		N/A
	The insertion loss fit at Nyquist frequency (ILfitatNq) shall meet the following requirements:		N/A
	$\geq -4$ dB at 2.5 GHz,		N/A
	$\geq -6$ dB at 5 GHz, and		N/A
	$\geq -11$ dB at 10 GHz.		N/A
	2.5 GHz, 5.0 GHz and 10 GHz are the Nyquist frequencies for SuperSpeed USB Gen1, SuperSpeed USB Gen2, and USB4 Gen3 data rate, respectively.		N/A
3.7.2.3.2	Integrated Multi-reflection (Normative – USB 3.2 Gen2 and USB4 Gen2)		N/A
3.7.2.3.3	Integrated Crosstalk between TX/RX Pairs (Normative – USB 3.2 Gen2 and USB4 Gen2)		N/A
3.7.2.3.4	Integrated Crosstalk between TX/RX Pairs to		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	USB 2.0 D+/D- (Normative – USB 3.2 Gen2 and USB4 Gen2)		
	IDDXT_1NEXT + FEXT $\leq$ -34.5 dB,		N/A
	IDDXT_2NEXT $\leq$ -33 dB.		N/A
3.7.2.3.5	Integrated Return Loss (Normative – USB 3.2 Gen2 and USB4 Gen2)		N/A
3.7.2.3.6	Differential-to-Common-Mode Conversion (Normative – USB 3.2 Gen2 and USB4 Gen2)		N/A
	The differential-to-common-mode conversion is specified to control the injection of common mode noise from the cable assembly into the host or device. Figure 3-43 illustrates the differential-to-common mode conversion (SCD12/SCD21) requirement. A mated cable assembly passes if its SCD12/SCD21 is less than or equal to -20 dB from 100 MHz to 10GHz.		N/A
3.7.2.4	TX/RX Passive Cable Assembly Requirements for USB 3.2 Gen1 and USB4 Gen2 (Normative)		N/A
3.7.2.4.1	Insertion Loss Fit at Nyquist Frequencies		N/A
	The integrated S-parameter requirements for USB 3.2 Gen1 and USB4 Gen2 follow the same methodology as defined in Section 3.7.2.3. There are parameter adjustments made to suit the USB4 Gen2 data rate. Unless otherwise specified, the following parameters shall be used to calculate insertion loss fit and integrated parameters:		N/A
	Tb, the unit interval, is set to 100 ps, reflecting the USB4 Gen2 data rate.		N/A
	Tr, the rise time, remains at 0.4 * Tb.		N/A
	fmax, the maximum frequency over which the integration or fitting is performed is increased to 12.5 GHz.		N/A
	The fitting equation is defined by the following equation:		N/A
	The insertion loss fit at Nyquist frequency (ILfitatNq) shall meet the following requirements:		N/A
	$\geq$ -7.0 dB at 2.5 GHz, and		N/A
	$>$ -11.5 dB at 5 GHz.		N/A
3.7.2.4.2	Integrated Multi-reflection		N/A
3.7.2.4.3	Integrated Crosstalk from TX/RX Pairs		N/A
	The largest values of INEXT and IFEXT shall meet the following requirements:		N/A
	INEXT $\leq$ -40 dB to 12.5GHz, for TX1 to RX1, TX2 to RX2, TX1 to RX2, TX2 to RX1, TX1 to TX2, and RX1 to RX2,		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	IFEXT $\leq -40$ dB to 12.5GHz, for TX1 to RX1, TX2 to RX2, TX1 to RX2, TX2 to RX1, TX1 to TX2, and RX1 to RX2.		N/A
	The port-to-port crosstalk (TX1 to RX2, TX2 to RX1, TX1 to TX2, and RX1 to RX2) is specified to support the usages in which all the four high speed pairs transmit or receive signals simultaneously (e.g., USB dual-lane operation).		N/A
3.7.2.4.4	Integrated Crosstalk from TX/RX Pairs to USB 2.0 D+/D-		N/A
	Crosstalk from the TX/RX pairs to USB 2.0 D+/D- shall be controlled to ensure the robustness of the USB 2.0 link. Since USB Type-C to Type-C Full-Featured cable assemblies may support the usage of USB 3.2, USB4 or an Alternate Mode (e.g., DisplayPort™), the crosstalk from the four high speed differential pairs to D+/D- may be from near-end crosstalk, far-end crosstalk, or a combination of the two. The integrated crosstalk to D+/D- is calculated with the following equations:		N/A
	The integration shall be done for NEXT + FEXT and 2NEXT on D+/D- from the two differential pairs located at A2, A3, B10 and B11 (see Figure 2-2) and for NEXT + FEXT and 2NEXT on D+/D- from the two differential pairs located at B2, B3 A10 and A11 (see Figure 2-2). Measurements are made in two sets to minimize the number of ports required for each measurement.		N/A
	The integrated differential crosstalk on D+/D- shall meet the following requirements:		N/A
	The integrated differential crosstalk on D+/D- shall meet the following requirements:		N/A
	IDDXT_2NEXT $\leq -33$ dB.		N/A
3.7.2.4.5	Integrated Return Loss		N/A
3.7.2.4.6	Differential-to-Common-Mode Conversion		N/A
	The differential-to-common-mode conversion is specified to control the injection of common mode noise from the cable assembly into the host or device. A mated cable assembly passes if its SCD12/SCD21 is less than or equal to -17 dB from 100 MHz to 10 GHz.		N/A
3.7.2.5	Normative TX/RX Passive Cable Assembly Requirements (USB4 Gen3)		N/A
	The integrated S-parameter requirements for USB4 Gen3 follow the same methodology as defined in Section 3.7.2.3. There are parameter adjustments made to suit the USB4 Gen3 data rate. Unless otherwise specified, the following parameters shall be used to calculate insertion		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	loss fit and integrated parameters:		
	Tb, the unit interval, is set to 50 ps, reflecting the USB4 Gen3 data rate.		N/A
	Tr, the rise time, remains at 0.4 * Tb.		N/A
	fmax, the maximum frequency over which the integration or fitting is performed is increased to 20 GHz.		N/A
	An f-square term is added to the insertion loss fit equation to improve fitting quality:		N/A
	USB4 Gen3 introduces a system-level COM (Channel Operating Margin) specification for the cable assembly. The details are defined in Section 3.7.2.5.7.		N/A
3.7.2.5.1	Insertion Loss Fit at Nyquist Frequencies (Normative – USB4 Gen3)		N/A
	The insertion loss fit at Nyquist frequency (ILfitatNq) shall meet the following requirements:		N/A
	≥ -1 dB at 100 MHz,		N/A
	≥ -4.2 dB at 2.5 GHz,		N/A
	≥ -6 dB at 5 GHz,		N/A
	≥ -7.5 dB at 10 GHz,		N/A
	≥ -9.3 dB at 12.5 GHz, and		N/A
	≥ -11 dB at 15 GHz.		N/A
3.7.2.5.2	Integrated Multi-Reflection (Informative – USB4 Gen3)		N/A
3.7.2.5.3	Integrated Crosstalk between TX/RX Pairs (Normative – USB4 Gen3)		N/A
	The integrated crosstalk within a port for TX1 to RX1 and TX2 to RX2 is recommended to meet the following informative requirements:		N/A
	INEXT ≤ -43 dB and		N/A
	IFEXT ≤ -43 dB.		N/A
	The recommended informative requirement for the integrated port-to-port crosstalk for TX1 to RX2, TX2 to RX1, TX1 to TX2, and RX1 to RX2) are defined as:		N/A
	INEXT_p2p ≤ -50 dB and		N/A
	IFEXT_p2p ≤ -50 dB.		N/A
3.7.2.5.4	Integrated Crosstalk from TX/RX Pairs to USB 2.0 D+/D- (Normative –USB4 Gen3)		N/A
	The requirements for the integrated crosstalk from the TX/RX pairs to USB 2.0 D+/D- are defined in Section 3.7.2.3.4.		N/A
3.7.2.5.5	Integrated Return Loss (Normative – USB4 Gen3)		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
3.7.2.5.6	Differential-to-Common-Mode Conversion (Normative – USB4 Gen3)		N/A
	Figure 3-48 illustrates the differential-to-common mode conversion (SCD12/SCD21) requirement. A mated cable assembly passes if its SCD12/SCD21 is less than or equal to -17 dB from 100 MHz to 10 GHz. Note that -17 dB is the worst-case limit; no USB4 Gen3 Type-C cable is allowed to exceed it.		N/A
3.7.2.5.7	COM Requirement (Normative – USB4 Gen3)		N/A
	Channel Operating Margin (COM) is a figure of merit to measure the channel electrical quality. The technical detail of COM may be found in IEEE Std 802.3bj™-2014 Clause 93a.		N/A
	COM is essentially the channel signal-to-noise ratio:		N/A
	To calculate COM, reference hosts/devices, which represent the worst-case hosts/devices, shall be defined and the reference TX and RX shall be used. As illustrated in Figure 3-49, the measured cable assembly S-parameters are cascaded with the reference host and reference device models to form the complete channel; the TX and RX die-loading and equalizers are then applied to the channel to calculate COM.		N/A
	To support the calculation of the cable assembly COM, the following collaterals is provided and may be obtained from USB-IF website:		N/A
	Reference host/device S-parameter models		N/A
	Reference TX and RX die-loading S-parameter models		N/A
	COM configuration file		N/A
	Tool to compute COM		N/A
3.7.2.6	Low-Speed Signal Requirements (Normative)		N/A
	This section specifies the electrical requirements for CC and SBU wires and the coupling among CC, USB D+/D-, VBUS and SBU.		N/A
3.7.2.6.1	CC to USB D+/D- (Normative)		N/A
	The differential coupling between the CC and D+/D- shall be below the limit shown in Figure 3-50. The limit is defined with the vertices of (0.3 MHz, -60.5 dB), (1 MHz, -50 dB), (10 MHz, -30 dB), (16 MHz, -26 dB) and (100 MHz, -26 dB).		N/A
3.7.2.6.2	VBUS Coupling to SBU_A/SBU_B, CC, and USB D+/D- (Normative)		N/A
	The differential coupling between VBUS and USB D+/D- shall be less than the limit shown		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	in Figure 3-53. The limit is defined by the following vertices: (0.3 MHz, -40 dB), (1 MHz, -40 dB), (30 MHz, -40 dB), and (100 MHz, -30 dB).		
	The maximum VBUS loop inductance shall be 900 nH and the maximum mutual inductance (M) between VBUS and low speed signal lines (CC, SBU_A, SBU_B, D+, D-) shall be as specified in Table 3-26 to limit VBUS inductive noise coupling on low speed signal lines. For fullfeatured cables, the range of VBUS bypass capacitance shall be 8nF up to 500nF as any of the values in the range is equally effective for high-speed return-path bypassing.		N/A
3.7.2.6.3	Coupling between SBU_A and SBU_B (Normative)		N/A
	The single-ended coupling between SBU_A and SBU_B shall be less than the limit shown in Figure 3-54. The limit is defined with the vertices of (0.3 MHz, -56.5 dB), (1 MHz, -46 dB), (10 MHz, -26 dB), (11.2 MHz, -25 dB), and (100 MHz, -25 dB).		N/A
3.7.2.6.4	Coupling between SBU_A/SBU_B and CC (Normative)		N/A
	The single-ended coupling between SBU_A and CC, and between SBU_B and CC shall be less than the limit shown in Figure 3-55. The limit is defined with the vertices of (0.3 MHz, -65 dB), (1 MHz, -55 dB), (18 MHz, -30 dB), and (100 MHz, -30 dB).		N/A
3.7.2.6.5	Coupling between SBU_A/SBU_B and USB D+/D- (Normative)		N/A
	The coupling between SBU_A and differential D+/D-, and between SBU_B and differential D+/D- shall be less than the limit shown in Figure 3-56. The limit is defined with the vertices of (0.3 MHz, -80 dB), (30 MHz, -40 dB), and (100 MHz, -40 dB).		N/A
3.7.2.7	USB D+/D- Signal Requirements (Normative)		N/A
	The USB D+/D- lines of the USB Type-C to USB Type-C passive cable assembly shall meet the requirements defined in Table 3-27.		N/A
3.7.2.8	VBUS DC Voltage Tolerance (Normative)		N/A
	A USB Type-C to USB Type-C cable assembly shall tolerate a VBUS voltage of 21 V DC at the cable rated current (i.e. 3 A or 5 A) applied for one hour as a pre-condition of the testing of the electrical aspects of the cable assembly.		N/A
3.7.3	<b>Mated Connector (Informative – USB 3.2 Gen2 and USB4 Gen2)</b>		N/A
	The mated connector as defined in this specification for USB Type-C consists of a receptacle mounted on a PCB, representing		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
	how the receptacle is used in a product, and a test plug also mounted on a PCB (paddle card) without cable. This is illustrated in Figure 3-57. Note that the test plug is used in host/device TX/RX testing also.		
3.7.3.1	Differential Impedance (Informative)		N/A
	The mated connector impedance target is specified to minimize reflection from the connector. The differential impedance of a mated connector should be within $85\ \Omega \pm 9\ \Omega$ , as seen from a 40 ps (20% – 80%) rise time. The impedance profile of a mated connector should fall within the limits shown in Figure 3-58.		N/A
	The PCB stack up, lead geometry, and solder pad geometry should be modeled in 3D fieldsolver to optimize electrical performance. Example ground voids under signal pads are shown in Figure 3-59 based on pad geometry, mounting type, and PCB stack-up shown.		N/A
3.7.3.2	Mated Connector Recommended Differential S-Parameter and Signal Integrity Characteristics (Informative)		N/A
	The recommended signal integrity characteristics of USB Type-C mated connector pair are listed in Table 3-28.		N/A
<b>3.7.4</b>	<b>Receptacle Connector SI Requirements and Testing (Normative – USB4 Gen3)</b>		N/A
	The USB Type-C receptacle connector requirements for USB4 Gen3 are normative and listed in Table 3-29. Unless otherwise specified, the items to be specified are identical to what is defined in Section 3.7.3 and the parameters used to calculate the integrated parameters are the same as defined in Section 3.7.2.4 for the USB4 Gen3 cable assembly.		N/A
	The requirements defined in this section do not apply to the USB Type-C plug connector, as the limits Table 3-29 factor in the electrical characteristics of test fixture that includes a USB Type-C plug connector specifically selected for testing of the USB Type-C receptacle. The USB Type-C plug connector does not have a set of requirements defined at the mated connector level as there are tradeoffs allowed to achieve acceptable performance at the finished cable assembly level.		N/A
<b>3.7.5</b>	<b>USB Type-C to Legacy Cable Assemblies (Normative)</b>		N/A
	The USB Type-C to legacy cable assemblies may support USB 2.0 only or USB 3.2 Gen2; USB 3.2 Gen1-only Type-C to legacy cable assemblies are not allowed.		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
3.7.5.1	USB 2.0-only Cable Assemblies (Normative)		N/A
	The USB 2.0-only Type-C to legacy USB cable assemblies include:		N/A
	USB Type-C plug to USB 2.0 Standard-A plug		N/A
	USB Type-C plug to USB 2.0 Standard-B plug		N/A
	USB Type-C plug to USB 2.0 Micro-B plug		N/A
	USB Type-C plug to USB 2.0 Mini-B plug		N/A
3.7.5.2	USB 3.1 Gen2 Cable Assemblies (Normative)		N/A
	The USB Type-C to USB 3.1 Gen2 legacy cable assemblies include:		N/A
	USB Type-C plug to USB 3.1 Standard-A plug		N/A
	USB Type-C plug to USB 3.1 Standard-B plug		N/A
	USB Type-C plug to USB 3.1 Micro-B plug		N/A
3.7.5.3	Compliant USB Legacy Plugs used in USB Type-C to Legacy Cable Assemblies		N/A
	The following requirements are incremental to the existing requirements for legacy connectors when used in compliant USB Type-C to legacy cable assemblies.		N/A
3.7.5.3.1	Contact Material Requirements for USB Type-C to USB Micro-B Assemblies		N/A
	For USB Type-C to USB Micro-B assemblies, change the contact material in the USB Micro-B connector to achieve the following Low-Level Contact Resistance (EIA 364-23B):		N/A
	20 milliohms (Max) initial for VBUS and GND contacts,		N/A
	Maximum change (delta) of +10 milliohms after environmental stresses.		N/A
3.7.5.3.2	Contact Current Ratings for USB Standard-A, USB Standard-B and USB Micro-B Connector Mated Pairs (EIA 364-70, Method 2)		N/A
	When a current of 3 A is applied to the VBUS pin and its corresponding GND pin (i.e., pins 1 and 4 in a USB Standard-A or USB Standard-B connector or pins 1 and 5 in a USB Micro-B connector), the delta temperature shall not exceed +30° C at any point on the connectors under test, when measured at an ambient temperature of 25° C.		N/A
3.7.6	<b>USB Type-C to USB Legacy Adapter Assemblies (Normative)</b>		N/A
	Only the following standard legacy adapter assemblies are defined:		N/A
	USB 2.0 Type-C plug to USB 2.0 Micro-B receptacle		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	USB Full-Featured Type-C plug to USB 3.1 Standard-A receptacle		N/A
3.7.6.1	USB 2.0 Type-C Plug to USB 2.0 Micro-B Receptacle Adapter Assembly (Normative)		N/A
	This adapter assembly supports only the USB 2.0 signaling. It shall not exceed 150 mm total length, measured from end to end. Table 3-33 defines the electrical requirements.		N/A
3.7.6.2	USB Full-Featured Type-C Plug to USB 3.1 Standard-A Receptacle Adapter Assembly (Normative)		N/A
	The USB Full-Featured Type-C plug to USB 3.1 Standard-A receptacle adapter assembly is intended to be used with a direct-attach device (e.g., USB thumb drive). A system is not guaranteed to function when using an adapter assembly together with a Standard USB cable assembly.		N/A
	To minimize the impact of the adapter assembly to system signal integrity, the adapter assembly should meet the informative design targets in Table 3-34.		N/A
3.7.6.3	Compliant USB Legacy Receptacles used in USB Type-C to Legacy Adapter Assemblies		N/A
3.7.6.3.1	Contact Material Requirements		N/A
	Refer to Section 3.7.5.3.1 for contact material requirements as these apply to legacy USB Standard-A and USB Micro-B receptacles used in USB Type-C to Legacy Adapter Assemblies.		N/A
3.7.6.3.2	Contact Current Ratings		N/A
	Refer to Section 3.7.5.3.2 for contact current rating requirements as these apply to legacy USB Standard-A and USB Micro-B receptacles used in USB Type-C to Legacy Adapter Assemblies.		N/A
3.7.7	<b>Shielding Effectiveness Requirements (Normative)</b>		N/A
	The cable assembly shielding effectiveness (SE) test measures the EMI and RFI levels from the cable assembly. To perform the measurement, the cable assembly shall be installed in the cable SE test fixture as shown in Figure 3-64. The coupling factors from the cable to the fixture are characterized with a VNA.		N/A
	All USB Type-C cable assemblies shall pass the shielding effectiveness test for compliance. Figure 3-65 shows the pass/fail criteria for (a) USB Type-C to USB Type-C cable assemblies, (b) USB Type-C to legacy USB cable assemblies, and (c) the USB Type-C to USB 3.1 Standard-A Receptacle Adapter assembly. Note that the shielding effectiveness for the frequency band from 4 GHz to 5 GHz is not		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	specified since there is no antenna operating in this frequency range.		
<b>3.7.8</b>	<b>DC Electrical Requirements (Normative)</b>		N/A
	Unless otherwise stated, the tests in this section are performed on mated connector pairs.		N/A
3.7.8.1	Low Level Contact Resistance (EIA 364-23B)		N/A
	The low-level contact resistance (LLCR) measurement is made across the plug and receptacle mated contacts and does not include any internal paddle cards or substrates of the plug or receptacle. See Figure 3-66. The following apply to the power and signal contacts:		N/A
	40 mΩ (Max) initial for VBUS, GND and all other contacts.		N/A
	50 mΩ (Max) after environmental stresses.		N/A
	Measure at 20 mV (Max) open circuit at 100 mA.		N/A
	Refer to Section 3.8 for environmental requirements and test sequences.		N/A
3.7.8.2	Dielectric Strength (EIA 364-20)		N/A
	No breakdown shall occur when 100 Volts AC (RMS) is applied between adjacent contacts of unmated and mated connectors.		N/A
3.7.8.3	Insulation Resistance (EIA 364-21)		N/A
	A minimum of 100 MΩ insulation resistance is required between adjacent contacts of unmated and mated connectors.		N/A
3.7.8.4	Contact Current Rating		N/A
	The current rating testing for the USB Type-C connector (plug and receptacle) shall be conducted per the following set up and procedures:		N/A
	A current of 5 A shall be applied collectively to VBUS pins (i.e., pins A4, A9, B4, and B9) and 1.25 A shall be applied to the VCONN pin (i.e., B5) as applicable, terminated through the corresponding GND pins (i.e., pins A1, A12, B1, and B12). A minimum current of 0.25 A shall also be applied individually to all the other contacts, as applicable. When current is applied to the contacts, the temperature of the connector pair shall be allowed to stabilize. The temperature rise of the outside shell surface of the mated pair above the VBUS and GND contacts shall not exceed 30 °C above the ambient temperature. Figure 3-67 provides an illustration of the measurement location.		N/A
	The measurement shall be done in still air.		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	The connectors shall be oriented such that the accessible outer shell surface is on top and horizontal to the ground.		N/A
	The plug and receptacle may require modification to access solder tails or cable attachment points.		N/A
	Either thermocouple or thermo-imaging (preferred) method may be used for temperature measurement		N/A
	For certification, the connector manufacturer shall provide the receptacle and plug samples under test mounted on a current rating test PCB with no copper planes. A cable plug may use short wires to attach the cable attachment points together rather than using a current rating test PCB.		N/A
	The current rating test PCBs shall be of a 2-layer construction. If 2-layer construction is not possible due to the solder tail configuration, VBUS and ground traces shall be located on the outer layers with the inner layers reserved for signal traces, as required; VCONN traces may be routed either on internal or external layers. Table 3-36 defines the requirements for the test PCB thickness and traces. The trace length applies to each PCB (receptacle PCB and plug PCB) and is from the contact terminal to the current source tie point. Figure 3-68 provides an informative partial trace illustration of the current rating test PCB.		N/A
	If short wires are used instead of a current rating test PCB, the wire length shall not exceed 70 mm, measured from the plug contact solder point to the other end of the wire. There shall be no paddle card or overmold included in the test set-up. Each plug solder tail shall be attached with a wire with the wire gauge of AWG 36 for signals, AWG 32 for power (VBUS and VCONN), and AWG 30 for ground.		N/A
3.7.8.5	DC Resistance of D+ and D-		N/A
	The DC Resistance of the D+ and D- in USB 2.0 High-Speed capable USB Type-C devices and USB 2.0 High-Speed capable USB Type-C Captive devices shall be equal or less than the maximum value specified in Table 3-37. The D+ and D- DC Resistance is the series combination of any resistance in switches, multiplexers, and the USB PHY.		N/A
	A USB Type-C Host operating in USB 2.0 High-Speed mode shall implement a disconnect threshold voltage (VHSDSC) level as defined in the USB 2.0 DCR ECN.		N/A
<b>3.8</b>	<b>Mechanical and Environmental</b>		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
	<b>Requirements (Normative)</b>		
	The requirements in this section apply to all USB Type-C connectors and/or cable assemblies unless otherwise specified. For USB Type-C plug connectors and cable assemblies, the test methods are based on an assumption that the cable exits the overmold in line with mating direction to a USB Type-C receptacle (i.e., straight out the back of the overmold). For USB Type-C plug connectors and cable assemblies with the cable exiting the overmold in a different direction than straight out the back (e.g., right angle to the mating direction), test fixtures and procedures shall be modified as required to accomplish the measurement.		N/A
<b>3.8.1</b>	<b>Mechanical Requirements</b>		N/A
3.8.1.1	Insertion Force (EIA 364-13)		N/A
	The initial connector insertion force shall be within the range from 5 N to 20 N at a maximum rate of 12.5 mm (0.492") per minute. This requirement does not apply when the connectors are used in a docking application.		N/A
	It is recommended to use a non-silicone-based lubricant on the latching mechanism to reduce wear. The effects of lubricants should be restricted to insertion and extraction characteristics and should not increase the resistance of the mated connection.		N/A
3.8.1.2	Extraction Force (EIA 364-13)		N/A
	The initial connector extraction force shall be within the range of 8 N to 20 N, measured after a preconditioning of five insertion/extraction cycles (i.e., the sixth extraction). After an additional twenty-five insertion/extraction cycles, the extraction force shall be measured again (i.e., the thirty-second extraction) and the extraction force shall be:		N/A
	a. within 33% of the initial reading, and		N/A
	b. within the range of 8 N to 20 N.		N/A
	The extraction force shall be within the range of 6 N to 20 N after 10,000 insertion/ extraction cycles. The extraction force measurement shall be performed at a maximum speed of 12.5 mm (0.492") per minute. The extraction force requirement does not apply when the connectors are used in a mechanical docking application.		N/A
	It is recommended to use a non-silicone-based lubricant on the latching mechanism to reduce wear. The effects of lubricants should be restricted to insertion and extraction characteristics and should not increase the		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	resistance of the mated connection.		
3.8.1.3	Durability or Insertion/Extraction Cycles (EIA 364-09)		N/A
	The durability rating shall be 10,000 cycles minimum for the USB Type-C connector family. The durability test shall be done at a rate of 500 $\pm$ 50 cycles per hour and no physical damage to any part of the connector and cable assembly shall occur.		N/A
3.8.1.4	Cable Flexing (EIA 364-41, Condition 1)		N/A
	No physical damage or discontinuity over 1ms during flexing shall occur to the cable assembly with Dimension X = 3.7 times the cable diameter and 500 cycles in each of two planes.		N/A
3.8.1.5	Cable Pull-Out (EIA 364-38, Method A)		N/A
	No physical damage to the cable assembly shall occur when it is subjected to a 40 N axial load for a minimum of 1 minute while clamping one end of the cable plug.		N/A
3.8.1.6	Cable Pull-Out (EIA 364-38, Method A)		N/A
	The USB Type-C connector family shall be tested for continuity under stress using a test fixture shown in Figure 3-69 or equivalent.		N/A
	Plugs shall be supplied with a representative overmold or mounted on a 2-layer printed circuit board (PCB) between 0.8 mm and 1.0 mm thickness as applicable. A USB Type-C receptacle shall be mounted on a 2-layer PCB between 0.8 mm and 1.0 mm thickness. The PCB shall be clamped on three sides of the receptacle no further than 5 mm away from the receptacle outline. The receptacle PCB shall initially be placed in a horizontal plane, and a perpendicular moment shall be applied to the plug with a 5 mm ball tipped probe for a period of at least 10 seconds at a distance of 15 mm from the mating edge of the receptacle shell in a downward direction, perpendicular to the axis of insertion. See Table 3-38 for the force and moment to be applied. Any configuration of non-conductive shell receptacles shall be tested at the values specified for the vertical receptacle configuration.		N/A
	The continuity across each contact shall be measured throughout the application of the tensile force. Each non-ground contact shall also be tested to confirm that it does not short to the shell during the stresses. The PCB shall then be rotated 90 degrees such that the cable is still inserted horizontally and the tensile force in Table 3-38 shall be applied again in the downward direction and continuity measured as before. This test is repeated for 180 degree and 270 degree rotations. Passing parts shall not		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	exhibit any discontinuities or shorting to the shell greater than 1 $\mu$ s duration in any of the four orientations.		
	One method for measuring the continuity through the contacts is to short all the wires at the end of the cable pigtail and apply a voltage through a pull-up to each of VBUS, USB D+, USB D-, SBU, CC, and TX/RX pins, with the GND pins connected to ground.		N/A
	Alternate methods are allowed to verify continuity through all pins.		N/A
3.8.1.7	Wrenching Strength		N/A
	USB Type-C plugs on cable assemblies and fixture plugs without overmold (including PCBmount USB Type-C plugs) shall be tested using the mechanical wrenching test fixture defined in the Universal Serial Bus Type-C Connectors and Cable Assemblies Compliance Document. For plug without overmold, the supplier shall provide a plug test fixture that conforms to the specified plug overmold dimensions for the USB Type-C plug (see Figure 3-70). The fixture may be metal or other suitable material. Perpendicular moments are applied to the plug with a 5 mm ball tipped probe for a period of at least 10 seconds when inserted in the test fixture to achieve the defined moments in four directions of up or down (i.e., perpendicular to the long axis of the plug opening) and left or right (i.e., in the plane of the plug opening). Compliant connectors shall meet the following force thresholds:		N/A
	A moment of 0-0.75 Nm (e.g., 50 N at 15 mm from the edge of the receptacle) is applied to a plug inserted in the test fixture in each of the four directions. A single plug shall be used for this test. Some mechanical deformation may occur. The plug shall be mated with the continuity test fixture after the test forces have been applied to verify no damage has occurred that causes discontinuity or shorting. The continuity test fixture shall provide a planar surface on the mating side located $6.20 \pm 0.20$ mm from the receptacle Datum A, perpendicular to the direction of insertion. No moment forces are applied to the plug during this continuity test. Figure 3-71 illustrates an example continuity test fixture to perform the continuity test. The Dielectric Withstanding Voltage test shall be conducted after the continuity test to verify plug compliance.		N/A
	The plug shall disengage from the test fixture or demonstrate mechanical failure (i.e., the force applied during the test procedure peaks and		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
	drops off) when a moment of 2.0 Nm is applied to the plug in the up and down directions and a moment 3.5 Nm is applied to the plug in the left and right directions. A new plug is required for each of the four test directions. An example of the mechanical failure point and an illustration of the wrenching test fixture are shown in Figure 3-72 and Figure 3-73, respectively.		
3.8.1.8	Restriction of Hazardous Substances		N/A
	It is recommended that components be RoHS compliant.		N/A
<b>3.8.2</b>	<b>Environmental Requirements</b>		N/A
	The connector interface environmental tests shall follow EIA 364-1000.01, Environmental Test Methodology for Assessing the Performance of Electrical Connectors and Sockets Used in Business Office Applications.		N/A
	Since the connector defined has more than 0.127 mm wipe length, Test Group 6 in EIA 364- 1000.01 is not required. The temperature life test duration and the mixed flowing gas test duration values are derived from EIA 364-1000.01 based on the field temperature per the following.		N/A
	The pass/fail criterion for the low-level contact resistance (LLCR) is as defined in Section 3.7.8.1. The durability ratings are defined in Section 3.8.1.3.		N/A
3.8.2.1	Reference Materials (Informative)		N/A
	This specification does not specify materials for connectors and cables. Connector and cable manufacturers should select appropriate materials based on performance requirements. The information below is provided for reference only.		N/A
	Option I		N/A
	Receptacle		N/A
	Contact area: (Min) 0.05 $\mu\text{m}$ Au + (Min) 0.75 $\mu\text{m}$ Ni-Pd on top of (Min) 2.0 $\mu\text{m}$ Ni		N/A
	Plug		N/A
	Contact area: (Min) 0.05 $\mu\text{m}$ Au + (Min) 0.75 $\mu\text{m}$ Ni-Pd on top of (Min) 2.0 $\mu\text{m}$ Ni		N/A
	Option II		N/A
	Receptacle		N/A
	Contact area: (Min) 0.75 $\mu\text{m}$ Au on top of (Min) 2.0 $\mu\text{m}$ Ni		N/A
	Plug		N/A
	Contact area: (Min) 0.75 $\mu\text{m}$ Au on top of (Min) 2.0 $\mu\text{m}$ Ni		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	Other reference materials that connector and cable manufacturers select based on performance parameters listed in Table 3-40 are for reference only.		N/A
<b>3.9</b>	<b>Docking Applications (Informative)</b>		N/A
	In this specification, docking refers to plugging a device directly into a dock without using a cable assembly. The USB Type-C connector is defined to support such applications.		N/A
	The connector is only part of a docking solution. A complete docking solution at the system level may also include retention or locking mechanisms, alignment mechanisms, docking plug mounting solutions, and protocols supported through the connector. This specification does not attempt to standardize system docking solutions, therefore there is no interoperability requirement for docking solutions.		N/A
	The following list includes the requirements and guidelines when using the USB Type-C connector for docking:		N/A
	1. The USB Type-C plug used for docking shall work with compliant USB Type-C receptacle. It shall comply with all dimensional, electrical and mechanical requirements.		N/A
	2. If the plug on the dock does not include the side latches, then the dock should provide a retention or locking mechanism to secure the device to the plug. The retention latches also serve as one of the ground return paths for EMC. The docking design should ensure adequate EMC performance without the side latches if they are not present.		N/A
	3. The internal EMC fingers are not required for the docking plug as long as the receptacle and plug shells have adequate electrical connection.		N/A
	4. Alignment is critical for docking. Depending on system design, standard USB Type-C connectors alone may not provide adequate alignment for mating. System level alignment is highly recommended. Alignment solutions are implementation-specific.		N/A
	5. Fine alignment is provided by the connector. The receptacle front face may have lead-in features for fine alignment. Figure 3-74 shows an example of a USB Type-C receptacle with a lead-in flange compared to a receptacle without the flange.		N/A
<b>3.10</b>	<b>Implementation Notes and Design Guides</b>		N/A
	This section discusses a few implementation notes and design guides to help users design and use the USB Type-C connectors and cables.		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
<b>3.10.1</b>	<b>EMC Management (Informative)</b>		N/A
	Connector and cable assembly designers, as well as system implementers should pay attention to receptacle and cable assembly shielding to ensure a low-impedance grounding path. The following are guidelines for EMC management:		N/A
	The quality of raw cables should be ensured. The intra-pair skew or the differential to common mode conversion of the TX/RX pairs has a significant impact on cable EMC and should be controlled within the limits of this specification.		N/A
	The cable external braid should be physically connected to the plug metal shell as close to 360° as possible to control EMC. Without appropriate shielding termination, even a perfect cable with zero intra-pair skew may not meet EMC requirements. Copper tape may be needed to shield off the braid termination area.		N/A
	The wire termination contributes to common-mode noise. The breakout distance for the wire termination should be kept as small as possible to optimize EMC and signal integrity performance. If possible, symmetry should be maintained for the two lines within a differential pair.		N/A
	Besides the mechanical function, the side latches on the plug and the mid-plate in the receptacle also play a role for EMC. This is illustrated in Figure 3-75:		N/A
	1. The side latch should have electrical connection to the receptacle mid-plate (a docking plug may not have side latches).		N/A
	2. The side latches should be terminated to the paddle card GND plane inside the plug.		N/A
	3. The mid-plate should be directly connected to system PCB GND plane with three or more solder leads/tails.		N/A
	The EMC fingers inside the plug mates with the EMC pad in the receptacle. It is important for the EMC pad to have adequate connections to the receptacle shell. As illustrated in Figure 3-77, there are multiple laser welding points between the EMC pads and the receptacle shell, top and bottom.		N/A
	The receptacle shell should have sufficient connection points to the system PCB GND plane with apertures as small as possible. Figure 3-77 illustrates an example with multiple solder tails to connect the receptacle shell to system PCB GND.		N/A
<b>3.10.2</b>	<b>Stacked and Side-by-Side Connector Physical Spacing (Informative)</b>		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	Stacked and side-by-side USB connectors are commonly used in PC systems. Figure 3-79 illustrates the recommended spacing between connectors for stacked and side-by-side configurations.		N/A
<b>3.10.3</b>	<b>Cable Mating Considerations (Informative)</b>		N/A
	The receptacle mounting location, exterior product surfaces, cable overmold, and plug mating length need to be considered to ensure the USB Type-C plug is allowed to fully engage the USB Type-C receptacle. Figure 3-80 illustrates the recommended minimum plug overmold clearance to allow the cable plug to fully seat in the product receptacle.		N/A
	Figure 3-81 illustrates special considerations required when external walls are angled. For such applications, the USB Type-C receptacle shell may not provide as much mechanical alignment protection to the receptacle tongue as in the full shell design. Design options to allow the receptacle to pass mechanical test requirements include relief in the exterior wall surface to allow use of a full shell receptacle or use of a receptacle specifically designed for the application.		N/A
<b>3.11</b>	<b>Extended Power Range (EPR) Cables</b>		N/A
<b>3.11.1</b>	<b>Electrical Requirements</b>		N/A
	Extended Power Range cables have additional requirements to assure that these cables can deliver the full defined voltage and current range for USB PD EPR operation.		N/A
	EPR cables shall functionally support a reported 50 V and 5 A operation. The minimum functional voltage that a cable shall support is 53.65 V. The electrical components potentially in the path of VBUS in an EPR cable, e.g. bypass capacitors, should be minimally rated for 63V.		N/A
	To control the impact of inductive kickback and ringing that can increase the chance of arcing between a USB Type-C plug and receptacle when a cable is removed while power is still applied, an EPR cable may include a snubber capacitor within the plug at each end of the cable. See Appendix H for more information.		N/A
<b>3.11.2</b>	<b>EPR Cable Identification Requirements</b>		N/A
	All EPR cables shall be Electronically Marked and include EPR-specific information in the eMarker as defined by the USB PD specification. As defined in the USB PD specification, EPR cables are marked as 50 V and 5 A capable.		N/A
	All EPR cables shall be visibly identified with EPR cable identification icons as defined by the		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	USB-IF. This is required so that end users will be able to confirm visually that the cable supports up to as high of PDP = 240W as defined in the USB PD specification.		
<b>4</b>	<b>Functional</b>		P
	This chapter covers the functional requirements for the signaling across the USB Type-C® cables and connectors. This includes functional signal definition, discovery and configuration processes, and power delivery.		P
<b>4.1</b>	<b>Signal Summary</b>		P
<b>4.2</b>	<b>Signal Pin Descriptions</b>		N/A
<b>4.2.1</b>	<b>SuperSpeed USB Pins</b>		N/A
<b>4.2.2</b>	<b>USB 2.0 Pins</b>		N/A
<b>4.2.3</b>	<b>Auxiliary Signal Pins</b>		N/A
<b>4.2.4</b>	<b>Power and Ground Pins</b>		N/A
<b>4.2.5</b>	<b>Configuration Pins</b>		N/A
<b>4.3</b>	<b>Sideband Use (SBU)</b>		N/A
	The Sideband Use pins (SBU1 and SBU2) are limited to the uses as defined by this specification and additional functionality defined in the USB4 Specification. See Appendix E and Appendix A for use of the SBU pins in Alternate Modes and Audio Adapter Accessory Mode.		N/A
	The SBU pins on a port shall either be open circuit or have a weak pull-down to ground no stronger than zSBU Termination when in USB 3.2 or USB 2.0.		N/A
	These pins are pre-wired in the standard USB Full-Featured Type-C cable as individual single-ended wires (SBU_A and SBU_B). Note that SBU1 and SBU2 are cross-connected in the cable.		N/A
	When operating in USB4, these pins are used as the USB4 Sideband Channel with SBU1 mapping to SBTX and SBU2 mapping to SBRX. SBTX and SBRX functional requirements are as defined in the USB4 Specification. When a port determines that the locally-inserted plug is flipped (i.e. CC1 is open, CC2 is terminated), the USB4 Specification (reference Sideband Channel Lane Reversal) dictates that the port flip the SBTX and SBRX mappings to SBU1 and SBU2 in order to assure proper sideband transmit-to-receive end-to-end operation.		N/A
<b>4.4</b>	<b>Power and Ground</b>		N/A
<b>4.4.1</b>	<b>IR Drop</b>		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	The maximum allowable cable IR drop for ground (including ground on a captive cable) shall be 250 mV and for VBUS shall be 500 mV through the cable to the cable's maximum rated VBUS current capacity. When VCONN is being sourced, the IR drop for the ground shall still be met considering any additional VCONN return current.		N/A
<b>4.4.2</b>	<b>VBUS</b>		N/A
	The allowable default range for VBUS as measured at the Source receptacle shall be as defined by the USB 2.0 Specification and USB 3.2 Specification. For USB4, the USB 3.2 Specification is used for this requirement. NOTE that due to higher currents allowed, legacy devices may experience a higher voltage (up to 5.5V maximum) at light loads.		N/A
	The Source's USB Type-C receptacle VBUS pin shall remain unpowered and shall limit the capacitance between VBUS and GND as specified in Table 4-2 until a Sink is attached. The VBUS pin shall return to the unpowered state when the Sink is detached. See Table 4-29 for VBUS timing values. Legacy hosts/chargers that by default source VBUS when connected using any legacy USB connector (Standard-A, Micro-B, etc.) to USB Type-C cable or adapter are exempted from these two requirements.		N/A
	A DRP or Source (or device with Accessory Support) implementing an Rp pull-up as its method of connection detection shall provide an impedance between VBUS and GND on its receptacle pins as specified in Table 4-2 when not sourcing power on VBUS (i.e., when in states Unattached. SRC or Unattached. Accessory).		N/A
<b>4.4.3</b>	<b>VCONN</b>		N/A
	VCONN is provided by the Source to power cables with electronics in the plug. VCONN is provided over the CC pin that is determined not to be connected to the CC wire of the cable.		N/A
	Initially, VCONN shall be sourced on all Source USB Type-C receptacles that utilize the TX and RX pins during specific connection states as described in Section 4.5.2.2. Subsequently, if VCONN is not explicitly required by the cable or device as indicated in its eMarker, VCONN may be removed as described in Table 4-4. VCONN may also be sourced by USB Type-C receptacles that do not utilize the TX and RX pins as described in Section 4.5.2.2. USB PD VCONN_Swap command also provides the Source a means to request that the attached Sink source VCONN.		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
	To aid in reducing the power associated with supplying VCONN, a Source is allowed to either not source VCONN or turn off VCONN under any of the following conditions:		N/A
	Ra is not detected on the CC pin after tCCDebounce when the other CC pin is in the SRC.Rd state, or		N/A
	if there is no GoodCRC response to USB PD Discover Identity messages sent to SOP'.		N/A
	If the power source used to supply VCONN power is a shared power source for other USB VCONN and VBUS outputs, it must be bypassed with capacitance identical to the VBUS capacitance requirements of USB 3.2 Section 11.4.4 – Dynamic Attach and Detach. Any VCONN power source bypass capacitance must be isolated from the CC pins when VCONN is not being provided.		N/A
	The cable shall remove or weaken Ra according to the state diagram behavior in 4.5.2.5. The cable shall reapply Ra according to the state diagram behavior in 4.5.2.5. The cable shall discharge VCONN to below vVCONNDischarge on a cable disconnect. The cable shall control Ra at each of its ends independently based on the VCONN on that end.		N/A
	Implementation Note: Increasing Ra to 20KΩ will meet both the power dissipation for electronically marked passive cables and discharge 10μF to less than vVCONNDischarge in tvVCONNDischarge.		N/A
	The VPA shall remove or weaken Ra within tRaWeaken (as defined in Table 4-7) after VCONN enters the valid voltage range (vVCONNValid).		N/A
	The VPA shall reapply Ra when VCONN falls below vRaReconnect as defined in Table 4-7. The VPA shall discharge VCONN to below vVCONNDischarge within tvVCONNDischarge on a cable disconnect. The VPA shall consider the VCONN capacitance present in the accessory when discharging VCONN.		N/A
	The maximum power consumption while in an Alternate Mode is defined by the specification specific to the Alternate Mode being used.		N/A
	The VPD shall remove or weaken Ra within tRaWeaken (as defined in Table 4-8) after VCONN enters the valid voltage range (vVCONNValid).		N/A
	The VPD shall reapply Ra when VCONN falls below vRaReconnect as defined in Table 4-8. The VPD shall discharge VCONN to below vVCONNDischarge within tvVCONNDischarge on a cable disconnect. The VPD shall consider the VCONN capacitance present in the device		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	when discharging VCONN.		
<b>4.5</b>	<b>Configuration Channel (CC)</b>		N/A
<b>4.5.1</b>	<b>Architectural Overview</b>		N/A
	For the USB Type-C solution, two pins on the connector, CC1 and CC2, are used to establish and manage the Source-to-Sink connection. When the device is connected through a hub, the connection between a Sink (UFP) on the hub and the Source (host port) and the connection between the Sink (device port) and a Source (DFP on the hub), are treated as separate connections. Functionally, the configuration channel is used to serve the following purposes.		N/A
	Detect attach of USB ports, e.g. a Source to a Sink		N/A
	Resolve cable orientation and twist connections to establish USB data bus routing		N/A
	Establish data roles between two attached ports		N/A
	Discover and configure VBUS: USB Type-C Current modes or USB Power Delivery		N/A
	Configure VCONN		N/A
	Discover and configure optional Alternate and Accessory modes		N/A
4.5.1.1	USB Data Bus Interface and USB Type-C Plug Flip-ability		N/A
	Since the USB Type-C plug can be inserted in either right-side-up or upside-down position, the hosts and devices that support USB data bus functionality must operate on the signal pins that are actually connected end-to-end. In the case of USB 2.0, this is done by shorting together the two D+ signal pins and the two D- signal pins in the host and device receptacles. In the case of USB 3.2 SuperSpeed USB or USB4 TX/RX signals in a single-lane implementation, it requires the functional equivalent of a switch in both the host and device to appropriately route the TX and RX signal pairs to the connected path through the cable. For a USB 3.2 SuperSpeed USB or USB4 dual-lane implementation, the host and/or device resolves the lane ordering.		N/A
	To establish the proper routing of the active USB data bus from host to device, the standard USB Type-C cable is wired such that a single CC wire is position aligned with the first TX/RX signal pairs (TXp1/TXn1 and RXp1/RXn1) – in this way, the CC wire and TX/RX data bus wires that are used for single-lane operational signaling within the cable track with regard to		N/A



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	the orientation and twist of the cable. By being able to detect which of the CC pins (CC1 or CC2) at the receptacle is terminated by the device, the host is able to determine which TX/RX signals are to be used for the single-lane connection and the host can use this to control the functional switch for routing the TX/RX signal pairs. Similarly in the device, detecting which of the CC pins at the receptacle is terminated by the host allows the device to control the functional switch that routes its TX/RX signal pairs.		
	For a dual-lane implementation, the TX/RX signal pairs in the cable/plug aligned with the CC wire/pin is Lane 0 and in reference to USB 3.2, shall be identified as the Configuration Lane. The second TX/RX signal pairs (TXp2/TXn2 and RXp2/RXn2) in the cable/plug is Lane 1 of a dual-lane configuration.		N/A
	The functional requirements for implementing TX/RX data bus routing for the USB Type-C receptacle are not included in the scope of this specification. There are multiple host, device and hub architectures that can be used to accomplish this which could include either discrete or integrated switching, and could include merging this functionality with other USB 3.2 or USB4 design elements, e.g. a bus repeater.		N/A
	The functional requirements for addressing SBU1 and SBU2 routing is not included in the scope of this specification. For USB4, where SBTX and SBRX are mapped to SBU1 and SBU2, the adjustment to the mapping of these signals based on the connection state (flipped and/or twisted) of the cable is defined by the USB4 Specification (reference Sideband Channel Lane Reversal).		N/A
4.5.1.2	Connecting Sources and Sinks		N/A
	Given that the USB Type-C receptacle and plug no longer differentiate host and device roles based on connector shape, e.g., as was the case with USB Type-A and Type-B connectors, any two ports that have USB Type-C receptacles can be connected together with a standard USB Type-C cable. Table 4-9 summarizes the expected results when interconnecting Source, Sink and DRP ports.		N/A
	In the cases where no function results, neither port shall be harmed by this connection. The user has to independently realize the invalid combination and take appropriate action to resolve. While these two invalid combinations mimic traditional USB where host-to-host and device-to-device connections are not intended to work, the non-keyed USB Type-C solution		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	does not prevent the user from attempting such interconnects. VBUS and VCONN shall not be applied by a Source (host) in these cases.		
	The typical flow for the configuration of the interface in the general USB case of a Source (Host) to a Sink (Device) is as follows:		N/A
	1. Detect a valid connection between the ports (including determining cable orientation, Source/Sink and DFP/UFP relationship)		N/A
	2. Optionally discover the cable's capabilities		N/A
	3. Optionally establish alternatives to traditional USB power (See Section 4.6.2)		N/A
	a. USB PD communication over CC for advanced power delivery negotiation		N/A
	b. USB Type-C Current modes		N/A
	c. USB BC 1.2		N/A
	4. USB Device Enumeration		N/A
	For cases of Dual-Role-Power (DRP) ports connecting to either Source-only, Sink-only or another DRP, the process is essentially the same except that during the detecting a valid connection step, the DRP alternates between operating as a Source for detecting an attached Sink and presenting as a Sink to be detected by an attached Source. Ultimately this results in a Source-to-Sink connection.		N/A
4.5.1.2.1	Detecting a Valid Source-to-Sink Connection		N/A
	The general concept for setting up a valid connection between a Source and Sink is based on being able to detect terminations residing in the product being attached.		N/A
	To aid in defining the functional behavior of CC, a pull-up (Rp) and pull-down (Rd) termination model is used – actual implementation in hosts and devices may vary, for example, the pullup termination could be replaced by a current source. Figure 4-5 and Figure 4-6 illustrates two models, the first based on a pull-up resistor in the Source and the second replacing this with a current source.		N/A
	Initially, a Source exposes independent Rp terminations on its CC1 and CC2 pins, and a Sink exposes independent Rd terminations on its CC1 and CC2 pins, the Source-to-Sink combination of this circuit configuration represents a valid connection. To detect this, the Source monitors CC1 and CC2 for a voltage lower than its unterminated voltage – the choice of Rp is a function of the pull-up termination voltage and the Source's detection circuit. This indicates that either a Sink, a powered cable, or a Sink connected via a		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	powered cable has been attached.		
	Prior to application of VCONN, a powered cable exposes Ra on its VCONN pin. Ra represents the load on VCONN plus any resistive elements to ground. In some cable plugs it might be a pure resistance and in others it may be simply the load.		N/A
	The Source has to be able to differentiate between the presence of Rd and Ra to know whether there is a Sink attached and where to apply VCONN. The Source is not required to source VCONN unless Ra is detected.		N/A
	Two special termination combinations on the CC pins as seen by a Source are defined for directly attached Accessory Modes: Ra/Ra for Audio Adapter Accessory Mode (Appendix A) and Rd/Rd for Debug Accessory Mode (Appendix B).		N/A
	The Source uses de-bounce timers to reliably detect states on the CC pins to de-bounce the connection (tCCDebounce), and hide USB PD BMC communications (tPDDebounce).		N/A
	Once the Sink is powered, the Sink monitors CC1 and CC2 for a voltage greater than its local ground. The CC pin that is at a higher voltage (i.e. pulled up by Rp in the Source) indicates the orientation of the plug.		N/A
	Figure 4-3 shows how the inserted plug orientation is detected at the Source's receptacle by noting on which of the two CC pins in the receptacle an Rd termination is sensed. Now that the Source (Host) has recognized that a Sink (Device) is attached and the plug orientation is determined, it configures the TX/RX data bus routing to the receptacle.		N/A
	The Source (Host) then turns on VBUS. For the CC pin that does not connect Source-to-Sink through the cable, the Source supplies VCONN and may remove the termination. With the Sink (Device) now powered, it configures the USB data path. This completes the Host-to-Device connection.		N/A
	The Source monitors the CC wire for the loss of pull-down termination to detect detach. If the Sink is removed, the Source port removes any voltage applied to VBUS and VCONN, resets its interface configuration and resumes looking for a new Sink attach.		N/A
	Once a valid Source-to-Sink connection is established, alternatives to traditional USB power (VBUS as defined by either USB 2.0 or USB 3.2 specifications) may be available depending on the capabilities of the host and device. These include USB Type-C Current, USB Power Delivery, and USB Battery Charging 1.2.		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	In the case where USB PD PR_Swap is used to swap the Source and Sink of VBUS, the supplier of VCONN remains unchanged during and after the VBUS power swap. The new Source monitors the CC wire and the new Sink monitors VBUS to detect detach. When a detach event is detected, any voltages applied to VBUS and VCONN are removed, each port resets its interface configuration and resumes looking for an attach event.		N/A
	In the case where USB PD DR_Swap is used to swap the data roles (DFP and UFP), the source of VBUS and VCONN do not change after the data role swap.		N/A
	In the case where USB PD VCONN Swap is used to swap the VCONN source, the VBUS Source/Sink and DFP/UFP roles are maintained during and after the VCONN swap.		N/A
	The last step in the normal USB Type-C connect process is for the USB device to be attached and enumerated per standard USB 2.0 and USB 3.2 processes.		N/A
4.5.1.3	Configuration Channel Functional Models		N/A
	The functional models for the configuration channel behavior based on the CC1 and CC2 pins are described in this section for each port type: Source, Sink and Dual-Role-Power (DRP).		N/A
	The figures in the following sections illustrate the CC1 and CC2 routing after the CC detection process is complete. In these figures, VBUS and VCONN may or may not actually be available.		N/A
4.5.1.3.1	Source Configuration Channel Functional Model		N/A
	Referring to Figure 4-7, a port that behaves as a Source has the following functional characteristics:		N/A
	1. The Source uses a FET to enable/disable power delivery across VBUS and initially the Source has VBUS disabled.		N/A
	2. The Source supplies pull-up resistors (Rp) on CC1 and CC2 and monitors both to detect a Sink. The presence of an Rd pull-down resistor on either pin indicates that a Sink is being attached. The value of Rp indicates the initial USB Type-C Current level supported by the host.		N/A
	3. The Source can optionally clamp the voltage on either of its CC pins. The minimum clamping voltage shall be vCC-Clamp. The clamp is intended to protect the Source circuitry associated with CC functionality.		N/A
	4. The Source uses the CC pin pull-down characteristic to detect and establish the		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	correct routing for the SuperSpeed USB data path and determine which CC pin is intended for supplying VCONN.		
	5. Once a Sink is detected, the Source enables VBUS and VCONN.		N/A
	6. The Source can dynamically adjust the value of Rp to indicate a change in available USB Type-C Current to a Sink.		N/A
	7. The Source monitors the continued presence of Rd to detect Sink detach. When a detach event is detected, the Source removes, if supplied, VBUS and VCONN, and returns to step 2.		N/A
	8. If the Source supports advanced functions (USB Power Delivery and/or Alternate Modes), USB PD communication is required.		N/A
4.5.1.3.2	Sink Configuration Channel Functional Model		N/A
	Referring to Figure 4-9, a port that behaves as a Sink has the following functional characteristics:		N/A
	1. The Sink terminates both CC1 and CC2 to GND using pull-down resistors.		N/A
	2. The Sink determines that a Source is attached by the presence of power on VBUS.		N/A
	3. The Sink uses the CC pin pull-up characteristic to detect and establish the correct routing for the SuperSpeed USB data path.		N/A
	4. The Sink can optionally monitor CC to detect an available higher USB Type-C Current from the Source. The Sink shall manage its load to stay within the detected Source current limit.		N/A
	5. The Sink can optionally clamp the voltage on either of its CC pins. The minimum clamping voltage shall be vCC-Clamp. The clamp is intended to protect the Sink circuitry associated with CC functionality.		N/A
	6. If the Sink supports advanced functions (USB Power Delivery and/or Alternate Modes), USB PD communication is required.		N/A
4.5.1.3.3	Dual-Role-Power (DRP) Configuration Channel Functional Model		N/A
	Referring to Figure 4-11, a port that can alternate between DFP and UFP behaviors has the following functional characteristics:		N/A
	1. The DRP uses a FET to enable/disable power delivery across VBUS and initially when in Source mode has VBUS disabled.		N/A
	2. The DRP uses switches for presenting as a Source or Sink.		N/A
	3. The DRP has logic used during initial attach to toggle between Source and Sink operation:		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
	a. Until a specific stable state is established, the DRP alternates between exposing itself as a Source and Sink. The timing of this process is dictated by a period (tDRP), percentage of time that a DRP exposes Rp (dcSRC. DRP) and role transition time (tDRPTransition).		N/A
	b. When the DRP is presenting as a Source, it follows Source operation to detect an attached Sink – if a Sink is detected, it applies VBUS, VCONN, and continues to operate as a Source (e.g., cease alternating).		N/A
	c. When the DRP is presenting as a Sink, it monitors VBUS to detect that it is attached to a Source – if a Source is detected, it continues to operate as a Sink (cease alternating).		N/A
	4. If the DRP supports advanced functions (USB Power Delivery and/or Alternate Modes), USB PD communication is required.		N/A
4.5.1.4	USB Type-C Port Power Roles and Role Swapping Mechanisms		N/A
	USB Type-C ports on products (USB hosts, USB devices, USB chargers, etc.) can be generally characterized as implementing one of seven power role behavioral models:		N/A
	Source-only		N/A
	Source (Default) – strong preference toward being a Source but subsequently capable of becoming a Sink using USB PD swap mechanisms.		N/A
	Sink-only		N/A
	Sink (Default) – strong preference toward being a Sink but subsequently capable of becoming a Source using USB PD swap mechanisms.		N/A
	DRP: Toggling (Source/Sink)		N/A
	DRP: Sourcing Device		N/A
	DRP: Sinking Host		N/A
	Two independent sets of swapping mechanisms are defined for USB Type-C port implementations, one based on role swapping within the initial state machine connection process and the other based on subsequent use of USB PD-based swapping mechanisms.		N/A
4.5.1.4.1	USB Type-C State-Machine-Based Role Swapping		N/A
	During the initial USB Type-C state machine connection process, the products being connected end up in one of the two following roles associated with the termination of its port:		N/A
	Rp - VBUS and VCONN source and behaving as a downstream facing port (USB Host)		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
	Rd - VBUS sink and behaving as an upstream facing port (USB Device)		N/A
	A USB Type-C DRP-based product may incorporate either or both the Try.SRC and Try.SNK swap mechanisms to affect the resulting role. Try.SRC allows a DRP that has a policy-based preference to be a Source when connecting to another DRP to affect a transition from a destined Sink role to the Source role. Alternately, Try.SNK allows a DRP that has a policybased preference to be a Sink when connecting to another DRP to effect a transition from a destined Source role to the Sink role. Connection timing and other factors are involved in this process as defined in the USB Type-C state machine operation (see Section 4.5.2). It is important to note that these mechanisms, Try.SRC and Try.SNK, can only be used once as part of the initial connection process.		N/A
	Try.SRC and Try.SNK are intended to ensure more predictable power roles when initially connecting two DRPs, especially if the port partner does not support USB PD. For example, a small mobile device may want to implement Try.SNK, so that when attaching to a DRP laptop, the mobile device will always initially be the power sink. Similarly, a laptop or Power Bank may wish to implement Try.SRC to ensure it always sources power to attached DRPs. Selfpowered devices such as AMAs or those whose primary function is a data UFP may also consider implementing Try.SNK to ensure they can properly expose their functionality. If both sides support USB PD, the appropriate roles may then be further refined or swapped as per the USB PD specification.		N/A
4.5.1.4.2	USB PD-based Power Role, Data Role and VCONN Swapping		N/A
	Following the completion of the initial USB Type-C state machine connection process, products may use USB PD-based swapping mechanisms to command a change power roles, data roles and which end of the cable will supply VCONN. These mechanisms are:		N/A
	USB PD PR Swap : swaps Source (Rp) and Sink (Rd)		N/A
	USB PD DR Swap : swaps DFP (host data) and UFP (device data) roles		N/A
	USB PD VCONN Swap : swaps which port supplies VCONN		N/A
4.5.1.4.3	Power Role Behavioral Model Summary		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
<b>4.5.2</b>	<b>CC Functional and Behavioral Requirements</b>		N/A
	This section provides the functional and behavioral requirements for implementing CC. The first sub-section provides connection state diagrams that are the basis for the remaining subsections.		N/A
	The terms Source (SRC) and Sink (SNK) used in this section refer to the port's power role while the terms DFP and UFP refer to the port's data role. A DRP (Dual-Role-Power) port is capable of acting as either a Source or Sink. Typically, Sources are found on hosts and supply VBUS while a Sink is found on a device and consumes power from VBUS. When a connection is initially made, the port's initial power state and data role are established. USB PD introduces three swap commands that may alter a port's power or data role:		N/A
	The PR_Swap command changes the port's power state as reflected in the following state machines. PR_Swap does not change the port sourcing VCONN.		N/A
	The DR_Swap command has no effect on the following state machines or VCONN as it only changes the port's data role.		N/A
	VCONN_Swap command changes the port sourcing VCONN. The PR_Swap command and DR_Swap command have no effect on the port sourcing VCONN.		N/A
	The connection state diagrams and CC behavior descriptions in this section describe the behavior of receptacle-based ports. The plug on a direct connect device or a device with a captive cable shall behave as a plug on a cable that is attached at its other end in normal orientation to a receptacle. These devices shall apply and sense CC voltage levels on pin A5 only and pin B5 shall have an impedance above zOPEN, unless it is a VCONN-Powered Accessory, in which case B5 shall have an impedance Ra.		N/A
4.5.2.1	Connection State Diagrams		N/A
	This section provides reference connection state diagrams for CC-based behaviors.		N/A
	Refer to Section 4.5.2.2 for the specific state transition requirements related to each state shown in the diagrams.		N/A
	Refer to Section 4.5.2.4 for a description of which states are mandatory for each port type, and a list of states where USB PD communication is permitted.		N/A
4.5.2.2	Connection State Machine Requirements		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	Entry into any unattached state when “directed from any state” shall not be used to override tDRP toggle.		N/A
	A DRP or a Sink may consume default power from VBUS in any state where it is not required to provide VBUS.		N/A
	The following two tables define the electrical states for a CC pin in both a Source and a Sink. Every port has CC1 and CC2 pins, each with its own individual CC pin state. The combination of a port's CC1 and CC2 pin states are be used to define the conditions under which a port transitions from one state to another.		N/A
4.5.2.2.1	Disabled State		N/A
	The Disabled state is where the port prevents connection from occurring by removing all terminations from the CC pins.		N/A
	The port should transition to the Disabled state from any other state when directed. When the port transitions to the Disabled state from Attached.SNK, it shall keep all terminations on the CC pins removed for a minimum of tErrorRecovery.		N/A
	A port may choose not to support the Disabled state. If the Disabled state is not supported, the port shall be directed to either the Unattached.SNK or Unattached.SRC states after power-on.		N/A
4.5.2.2.1.1	Disabled State Requirements		N/A
	The port shall not drive VBUS or VCONN, and shall present a high-impedance to ground (above zOPEN) on its CC1 and CC2 pins.		N/A
4.5.2.2.1.2	Exiting from Disabled State		N/A
	A Sink shall transition to Unattached.SNK when directed.		N/A
	A Source shall transition to Unattached.SRC when directed.		N/A
	A DRP shall transition to either Unattached.SNK or Unattached.SRC when directed.		N/A
4.5.2.2.2	ErrorRecovery Stat		N/A
	The ErrorRecovery state is where the port removes the terminations from the CC1 and CC2 pins for tErrorRecovery followed by transitioning to the appropriate Unattached.SNK or Unattached.SRC state based on port type. This is the equivalent of forcing a detach event and looking for a new attach.		N/A
	Ports that support USB Power Delivery shall support the ErrorRecovery state.		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	Ports that support the ErrorRecovery state shall transition to the ErrorRecovery state from any other state when directed.		N/A
	does not support USB Power Delivery may choose not to support the ErrorRecovery state. If the ErrorRecovery state is not supported, the port shall be directed to the Disabled state if supported. If the Disabled state is not supported, the port shall be directed to either the Unattached.SNK or Unattached.SRC states.		N/A
4.5.2.2.2.1	ErrorRecovery State Requirements		N/A
	The port shall not drive VBUS or VCONN, and shall present a high-impedance to ground (above zOPEN) on its CC1 and CC2 pins.		N/A
4.5.2.2.2.2	Exiting from ErrorRecovery State		N/A
	A Sink shall transition to Unattached.SNK after tErrorRecovery.		N/A
	A Source shall transition to Unattached.SRC after tErrorRecovery.		N/A
	A DRP (Figure 4-15) and a DRP with Accessory and Try.SNK Support (Figure 4-17) shall transition to Unattached.SNK after tErrorRecovery.		N/A
	A DRP with Accessory and Try.SRC Support (Figure 4-16) shall transition to Unattached.SRC after tErrorRecovery.		N/A
4.5.2.2.3	Unattached.SNK State		N/A
	When in the Unattached.SNK state, the port is waiting to detect the presence of a Source.		N/A
	A port with a dead battery shall enter this state while unpowered.		N/A
4.5.2.2.3.1	Unattached.SNK Requirements		N/A
	The port shall not drive VBUS or VCONN.		N/A
	Both CC1 and CC2 pins shall be independently terminated to ground through Rd.		N/A
	A Charge-Through VCONN-Powered USB Device shall isolate its Host-side port from its Charge-Through port, including CCs and VBUS, and independently terminate its Charge-Through port's CC1 and CC2 pins and Host-side port's CC pin to ground through Rd.		N/A
4.5.2.2.3.2	Exiting from Unattached.SNK State		N/A
	If the port supports USB PD or accessories, the port shall transition to AttachWait.SNK when the SNK.Rp state is present on at least one of its CC pins.		N/A
	The maximum times that a Port shall take to transition to AttachWait.SNK are the following:		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	tNoToggleConnect when neither Port Partner is toggling		N/A
	tOnePortToggleConnect when one Port Partner only is toggling		N/A
	When both Port Partners are toggling, a Port should transition to AttachWait.SNK within tTwoPortToggleConnect. Note that when both Port Partners are DRPs it is indeterminate whether the local port will transition to AttachWait.SRC or AttachWait.SNK.		N/A
	A USB 2.0 only Sink that doesn't support accessories and is self-powered or requires only default power and does not support USB PD may transition directly to Attached.SNK when VBUS is detected.		N/A
	A DRP shall transition to Unattached.SRC within tDRPTransition after the state of both CC pins is SNK.Open for tDRP – dcSRC.DRP · tDRP, or if directed.		N/A
	A Sink with Accessory support shall transition to Unattached.Accessory within tDRPTransition after the state of both the CC1 and CC2 pins is SNK.Open for tDRP – dcSRC.DRP · tDRP, or if directed.		N/A
	A Charge-Through VCONN-Powered USB Device shall transition to Unattached.SRC within tDRPTransition after the state of the Host-side port's CC pin is SNK.Open for tDRP – dcSRC.DRP · tDRP and both of the following is detected on the Charge-Through port.		N/A
	SNK.Rp state is detected on exactly one of the CC1 or CC2 pins for at least tCCDebounce		N/A
	VBUS is detected		N/A
	A Charge-Through VCONN-Powered USB Device shall transition to Attached.SNK when a Source connection is detected, as indicated by the SNK.Rp state on its Host-side port's CC pin.		N/A
4.5.2.2.4	AttachWait.SNK State		N/A
	When in the AttachWait.SNK state, the port has detected the SNK.Rp state on at least one of its CC pins and is waiting for VBUS.		N/A
	When in the AttachWait.SNK state, the Charge-Through VCONN-Powered USB Device has detected the SNK.Rp state on its Host-side port's CC pin and is waiting for host-side VBUS.		N/A
4.5.2.2.4.1	AttachWait.SNK Requirements		N/A
	The port shall not drive VBUS or VCONN.		N/A
	Both the CC1 and CC2 pins shall be independently terminated to ground through Rd.		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
	A Charge-Through VCONN-Powered USB Device shall isolate its Host-side port from its Charge-Through port, including CCs and VBUS, and independently terminate its Charge-Through port's CC1 and CC2 pins and Host-side port's CC pin to ground through Rd.		N/A
	It is strongly recommended that a USB 3.2 SuperSpeed device hold off VBUS detection to the device controller until the Attached.SNK state or the DebugAccessory.SNK state is reached, i.e. at least one CC pin is in the SNK.Rp state. Otherwise, it may connect as USB 2.0 when attached to a legacy host or hub's DFP.		N/A
4.5.2.2.4.2	Exiting from AttachWait. SNK State		N/A
	A Sink shall transition to Unattached.SNK when the state of both the CC1 and CC2 pins is SNK.Open for at least tPDDebounce.		N/A
	A DRP shall transition to Unattached.SRC when the state of both the CC1 and CC2 pins is SNK.Open for at least tPDDebounce.		N/A
	The port shall transition to Attached.SNK after the state of only one of the CC1 or CC2 pins is SNK.Rp for at least tCCDebounce and VBUS is detected. Note the Source may initiate USB PD communications which will cause brief periods of the SNK.Open state on one of the CC pins with the state of the other CC pin remaining SNK.Open, but this event will not exceed tPDDebounce.		N/A
	If the port is a VCONN-Powered Accessory or a VCONN-Powered USB Device, the port shall transition to Attached.SNK when either VCONN or VBUS is detected. The port may transition without waiting tCCDebounce on CC.		N/A
	If the port supports Debug Accessory Mode, the port shall transition to DebugAccessory.SNK if the state of both the CC1 and CC2 pins is SNK.Rp for at least tCCDebounce and VBUS is detected. Note the DAM Source may initiate USB PD communications which will cause brief periods of the SNK.Open state on one of the CC pins with the state of the other CC pin remaining SNK.Rp, but this event will not exceed tPDDebounce.		N/A
	A Charge-Through VCONN-Powered USB Device shall transition to Attached.SNK after the state of the Host-side port's CC pin is SNK.Rp for at least tCCDebounce and either host-side VCONN or VBUS is detected.		N/A
	A DRP that strongly prefers the Source role may optionally transition to Try.SRC instead of Attached.SNK when the state of only one CC pin has been SNK.Rp for at least tCCDebounce and VBUS is detected.		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
4.5.2.2.5	Attached.SNK State		N/A
	When in the Attached.SNK state, the port is attached and operating as a Sink. When the port initially enters this state it is also operating as a UFP. The power and data roles can be changed using USB PD commands.		N/A
	A port that entered this state directly from Unattached.SNK due to detecting VBUS shall not determine orientation or availability of higher than Default USB Power and shall not use USB PD.		N/A
4.5.2.2.5.1	Attached.SNK Requirements		N/A
	If the port needs to determine the orientation of the connector, it shall do so only upon entry to this state by detecting which of the CC1 or CC2 pins is connected through the cable (i.e., the CC pin that is in the SNK.Rp state).		N/A
	If the port supports signaling on SuperSpeed USB pairs, it shall functionally connect the SuperSpeed USB pairs and maintain the connection during and after a USB PD PR_Swap.		N/A
	If the port has entered the Attached.SNK state from the AttachWait.SNK or TryWait.SNK states, only one the CC1 or CC2 pins will be in the SNK.Rp state. The port shall continue to terminate this CC pin to ground through Rd.		N/A
	If the port has entered the Attached.SNK state from the Attached.SRC state following a USB PD PR_Swap, the port shall terminate the connected CC pin to ground through Rd.		N/A
	The port shall meet the Sink Power Sub-State requirements specified in Section 4.5.2.2.22.		N/A
	If the port is a VCONN-Powered USB Device, it shall respond to USB PD cable identity queries on SOP'. It shall not send or respond to messages on SOP. It shall ensure there is sufficient capacitance on CC to meet cReceiver as defined in USB PD.		N/A
	A Charge-Through VCONN-Powered USB Device shall isolate its Host-side port from its Charge-Through port, including CCs and VBUS, present a high-impedance to ground (above zOPEN) on its Charge-Through port's CC1 and CC2 pins and terminate its Host-side port's CC pin to ground through Rd.		N/A
	A Charge-Through VCONN-Powered USB Device shall start a Charge-Through Support Timer when it enters the Attached.SNK state. If a Charge-Through VCONN-Powered USB Device fails to exit the Attached.SNK state before the Charge-Through Support Timer exceeds tAMETimeout, it shall present a USB Billboard Device Class interface indicating that		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	it does not support Charge-Through.		
	A Charge-Through VCONN-Powered USB Device shall reset the Charge-Through Support Timer when it first receives any USB PD Structured VDM Command it supports. If a Charge-Through VCONN-Powered USB Device receives a Structured VDM Command multiple times, it shall only reset the Charge-Through Support Timer once. This ensures a Charge-Through VCONN-Powered USB Device will present a USB Billboard Device Class interface if it fails to exit Attached.SNK while receiving repeated or continuous Structured VDM Commands (e.g., Discover Identity).		N/A
	A Charge-Through VCONN-Powered USB Device shall reset the Charge-Through Support Timer when it receives any Data Message it supports. A Charge-Through VCONN-Powered USB Device shall hold the Charge-Through Support Timer in reset while it is in any USB PD BIST mode.		N/A
	Except for a VCONN-Powered USB Device or Charge-Through VCONN-Powered USB Device, the port may negotiate a USB PD PR_Swap, DR_Swap or VCONN_Swap.		N/A
	If the port supports Charge-Through VCONN-Powered USB Device, and an explicit USB PD contract has failed to be negotiated, the port shall query the identity of the cable via USB PD on SOP'.		N/A
	If the port supports Charge-Through VCONN-Powered USB Device, and an explicit USB PD contract has failed to be negotiated, the port shall query the identity of the cable via USB PD on SOP'.		N/A
	The port may negotiate a USB PD VCONN_Swap. When the port successfully executes USB PD VCONN_Swap operation and was not sourcing VCONN, it shall start sourcing VCONN within tVCONNON. The port shall execute the VCONN_Swap in a make-before-break sequence in order to keep active USB Type-C to USB Type-C cables powered. When the port successfully executes USB PD VCONN_Swap operation and was sourcing VCONN, it shall stop sourcing VCONN within tVCONNOFF.		N/A
4.5.2.2.5.2	Exiting from Attached.SNK State		N/A
	A port that is not a VCONN-Powered USB Device and is not in the process of a USB PD PR_Swap or a USB PD Hard Reset or a USB PD FR_Swap shall transition to Unattached.SNK within tSinkDisconnect when VBUS falls below vSinkDisconnect for VBUS		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	operating at or below 5 V or below vSinkDisconnectPD when negotiated by USB PD to operate above 5 V.		
	A VCONN-Powered USB Device shall return to Unattached.SNK when VBUS has fallen below vSinkDisconnect and VCONN has fallen below vVCONNDisconnect.		N/A
	A port that has entered into USB PD communications with the Source and has seen the CC voltage exceed vRd-USB may monitor the CC pin to detect cable disconnect in addition to monitoring VBUS.		N/A
	A port that is monitoring the CC voltage for disconnect (but is not in the process of a USB PD PR_Swap or USB PD FR_Swap) shall transition to Unattached.SNK within tSinkDisconnect after the CC voltage remains below vRd-USB for tPDDebounce.		N/A
	If supplying VCONN, the port shall cease to supply it within tVCONNOff of exiting Attached.SNK.		N/A
	A Charge-Through VCONN-Powered USB Device shall transition to CTUnattached.VPD if VCONN is present and the state of its Host-side port's CC pin is SNK.Open for tVPDCTDD.		N/A
	A port that via SOP' has detected an attached Charge-Through VCONN-Powered USB Device shall transition to TryWait.SRC if implemented, or transition to Unattached.SRC or Unattached.Accessory if TryWait.SRC is not supported. This transition may be delayed until the device has sufficient battery charge needed to remain powered until it reaches the CTAttached.SNK state.		N/A
	After receiving a USB PD PS_RDY from the original Source during a USB PD PR_Swap, the port shall transition directly to the Attached.SRC state (i.e., remove Rd from CC, assert Rp on CC and supply VBUS), but shall maintain its VCONN supply state, whether off or on, and its data role/connections.		N/A
4.5.2.2.6	UnattachedWait.SRC State		N/A
	When in the UnattachedWait.SRC state, the port is discharging the CC pin that was providing VCONN in the previous Attached.SRC state.		N/A
4.5.2.2.6.1	UnattachedWait.SRC Requirements		N/A
	The port shall not enable VBUS or VCONN.		N/A
	The port shall complete the VCONN turn off initiated when leaving the previous Attached.SRC state.		N/A
	The port shall continue to provide an Rp termination, as specified in Table 4-24, on the CC pin not being discharged.		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	The port shall not provide an Rp termination on the CC pin being discharged.		N/A
	The port shall not provide an Rp termination on the CC pin being discharged.		N/A
	The port shall discharge the CC pin being discharged below vVCONNDIScharge.		N/A
4.5.2.2.6.2	Exiting from UnattachedWait.SRC State		N/A
	The port shall transition to Unattached.SRC when VCONN is below vVCONNDIScharge. The port may delay this transition to allow the cable plug more time to reapply Ra.		N/A
4.5.2.2.7	Unattached.SRC State		N/A
	When in the Unattached.SRC state, the port is waiting to detect the presence of a Sink or an Accessory.		N/A
	When in the Unattached.SRC state, the Charge-Through VCONN-Powered USB Device has detected a Source on its Charge-Through port and is independently monitoring its Host-side port to detect the presence of a Sink.		N/A
4.5.2.2.7.1	Unattached.SRC Requirements		N/A
	The port shall not drive VBUS or VCONN.		N/A
	The port shall source current on both the CC1 and CC2 pins independently.		N/A
	The port shall provide a separate Rp termination on the CC1 and CC2 pins as specified in Table 4-24. Note: A Source with a captive cable or just a plug presents a single Rp termination on its CC pin (A5).		N/A
	The Charge-Through VCONN-Powered USB Device shall isolate its Host-side port from its Charge-Through port, including CCs and VBUS. The Charge-Through VCONN-Powered USB Device shall ensure that it is powered by VBUS from the Charge-Through port.		N/A
	Upon entry into this state, the Charge-Through VCONN-Powered USB Device shall remove its Rd termination to ground on the Host-side port CC and provide an Rp termination instead advertising Default USB Power, as specified in Table 4-24, and continue to independently terminate its Charge-Through port's CC1 and CC2 pins to ground through Rd.		N/A
4.5.2.2.7.2	Exiting from Unattached.SRC State		N/A
	The port shall transition to AttachWait.SRC when:		N/A
	The SRC.Rd state is present on either the CC1 or CC2 pin or		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	The SRC.Ra state is present on both the CC1 and CC2 pins.		N/A
	The maximum times that a Port shall take to transition to AttachWait.SRC are the following:		N/A
	tNoToggleConnect when neither Port Partner is toggling		N/A
	tOnePortToggleConnect when one Port Partner only is toggling		N/A
	When both Port Partners are toggling, a Port should transition to AttachWait.SRC within tTwoPortToggleConnect. Note that when both Port Partners are DRPs it is indeterminate whether the local port will transition to AttachWait.SRC or AttachWait.SNK.		N/A
	The Charge-Through VCONN-Powered USB Device shall transition to AttachWait.SRC when host-side VBUS is vSafe0V and SRC.Rd state is detected on the Host-side port's CC pin.		N/A
	A DRP shall transition to Unattached.SNK within tDRPTransition after dcSRC.DRP · tDRP, or if directed.		N/A
	A Charge-Through VCONN-Powered USB Device shall transition to Unattached.SNK within tDRPTransition after dcSRC.DRP · tDRP, or if Charge-Through VBUS is removed.		N/A
4.5.2.2.8	AttachWait.SRC State		N/A
	The AttachWait.SRC state is used to ensure that the state of both of the CC1 and CC2 pins is stable after a Sink is connected.		N/A
	When in the AttachWait.SRC state, the Charge-Through VCONN-Powered USB Device ensures that the state of Host-side port's CC pin is stable after a Sink is connected.		N/A
4.5.2.2.8.1	AttachWait.SRC Requirements		N/A
	The requirements for this state are identical to Unattached.SRC.		N/A
4.5.2.2.8.2	Exiting from AttachWait.SRC State		N/A
	The port shall transition to Attached.SRC when VBUS is at vSafe0V and the SRC.Rd state is detected on exactly one of the CC1 or CC2 pins for at least tCCDebounce.		N/A
	The Charge-Through VCONN-Powered USB Device shall transition to Try.SNK when the hostside VBUS is at vSafe0V and the SRC.Rd state is on the Host-side port's CC pin for at least tCCDebounce.		N/A
	If the port supports Audio Adapter Accessory Mode, it shall transition to AudioAccessory when the SRC.Ra state is detected on both the CC1 and CC2 pins for at least tCCDebounce.		N/A
	If the port supports Debug Accessory Mode, it		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
	shall transition to UnorientedDebugAccessory. SRC when VBUS is at vSafe0V and the SRC.Rd state is detected on both the CC1 and CC2 pins for at least tCCDebounce.		
	A Source shall transition to Unattached.SRC and a DRP to Unattached.SNK when the SRC.Open state is detected on both the CC1 and CC2 pins. The Source shall detect the SRC.Open state within tSRCDisconnect, but should detect it as quickly as possible.		N/A
	A Source shall transition to Unattached.SRC and a DRP to Unattached.SNK when the SRC.Open state is detected on either the CC1 or CC2 pin and the other CC pin is SRC.Ra. The Source shall detect the SRC.Open state within tSRCDisconnect, but should detect it as quickly as possible.		N/A
	A Charge-Through VCONN-Powered USB Device shall transition to Unattached.SNK when the SRC.Open state is detected on the Host-side port's CC or if Charge-Through VBUS falls below vSinkDisconnect. The Charge-Through VCONN-Powered USB Device shall detect the SRC.Open state within tSRCDisconnect, but should detect it as quickly as possible.		N/A
	A DRP that strongly prefers the Sink role may optionally transition to Try.SNK instead of Attached.SRC when VBUS is at vSafe0V and the SRC.Rd state is detected on exactly one of the CC1 or CC2 pins for at least tCCDebounce.		N/A
4.5.2.2.9	Attached.SRC State		N/A
	When in the Attached.SRC state, the port is attached and operating as a Source. When the port initially enters this state it is also operating as a DFP. Subsequently, the initial power and data roles can be changed using USB PD commands.		N/A
	When in the Attached.SRC state, the Charge-Through VCONN-Powered USB Device has detected a Sink on its Host-side port and has connected the Charge-Through port VBUS to the Host-side port VBUS.		N/A
4.5.2.2.9.1	Attached.SRC Requirements		N/A
	If the port needs to determine the orientation of the connector, it shall do so only upon entry to the Attached.SRC state by detecting which of the CC1 or CC2 pins is connected through the cable, i.e., which CC pin is in the SRC.Rd state.		N/A
	If the port has entered this state from the AttachWait.SRC state or the Try.SRC state, the SRC.Rd state will be on only one of the CC1 or CC2 pins. The port shall source current on this CC pin and monitor its state.		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
	If the port has entered this state from the Attached.SNK state as the result of a USB PD PR_Swap, the port shall source current on the connected CC pin and monitor its state.		N/A
	The port shall provide an Rp as specified in Table 4-24.		N/A
	The port shall supply VBUS current at the level it advertises on Rp.		N/A
	The port shall supply VBUS within tVBUSON of entering this state, and for as long as it is operating as a power source.		N/A
	The port shall not initiate any USB PD communications until VBUS reaches vSafe5V.		N/A
	If the port supports signaling on SuperSpeed USB pairs, it shall:		N/A
	Functionally connect the SuperSpeed USB pairs		N/A
	For VCONN, do one of two things:		N/A
	Supply VCONN unconditionally to the CC pin not in the SRC.Rd state, or		N/A
	Supply VCONN to the CC pin in the SRC.Ra state.		N/A
	A port that does not support signaling on SuperSpeed USB pairs may supply VCONN in the same manner described above.		N/A
	The port may negotiate a USB PD PR_Swap, DR_Swap or VCONN_Swap.		N/A
	If the port supplies VCONN, it shall do so within tVCONNON.		N/A
	The port may query the identity of the cable via USB PD on SOP'. If it detects that it is connected to a VCONN-Powered USB Device, the port may remove VBUS and discharge it to vSafe0V, while continuing to remain in this state with VCONN applied. The port may also initiate other SOP' communication.		N/A
	The port shall not supply VCONN if it has entered this state as a result of a USB PD PR_Swap and was not previously supplying VCONN. A USB PD DR_Swap has no effect on which port sources VCONN.		N/A
	The port may negotiate a USB PD VCONN_Swap. When the port successfully executes USB PD VCONN_Swap operation and was sourcing VCONN, it shall stop sourcing VCONN within tVCONNOFF. The port shall execute the VCONN_Swap in a make-before-break sequence in order to keep active USB Type-C to USB Type-C cables powered. When the port successfully executes USB PD		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	VCONN_Swap operation and was not sourcing VCONN, it shall start sourcing VCONN within tVCONNON.		
	The Charge-Through VCONN-Powered USB Device shall continue to isolate its Host-side port's CC pin from its Charge-Through CC pins.		N/A
	The Charge-Through VCONN-Powered USB Device shall maintain its Rp termination advertising Default USB Power on the Host-side port's CC pin, and continue to independently terminate its Charge-Through port's CC1 and CC2 pins to ground through Rd.		N/A
	The Charge-Through VCONN-Powered USB Device shall immediately connect the Charge-Through port's VBUS through to the Host-side port's VBUS.		N/A
	The Charge-Through VCONN-Powered USB Device shall ensure that it is powered entirely by VBUS.		N/A
	The Charge-Through VCONN-Powered USB Device shall only respond to USB PD Discover Identity queries on SOP' on its Host-side port and complete any active queries prior to exiting this state. It shall ensure there is sufficient capacitance on the Host-side port CC to meet cReceiver as defined in USB PD.		N/A
4.5.2.2.9.2	Exiting from Attached.SRC State		N/A
	A Source that is supplying VCONN or has yielded VCONN source responsibility to the Sink through USB PD VCONN_Swap messaging shall transition to UnattachedWait.SRC when the SRC.Open state is detected on the monitored CC pin. The Source shall detect the SRC.Open state within tSRCDisconnect, but should detect it as quickly as possible.		N/A
	A Source that is not supplying VCONN and has not yielded VCONN responsibility to the Sink through USB PD VCONN_Swap messaging shall transition to Unattached.SRC when the SRC.Open state is detected on the monitored CC pin. The Source shall detect the SRC.Open state within tSRCDisconnect, but should detect it as quickly as possible.		N/A
	When the SRC.Open state is detected on the monitored CC pin, a DRP shall transition to Unattached.SNK unless it strongly prefers the Source role. In that case, it shall transition to TryWait.SNK. This transition to TryWait.SNK is needed so that two devices that both prefer the Source role do not loop endlessly between Source and Sink. In other words, a DRP that would enter Try.SRC from AttachWait.SNK shall enter TryWait.SNK for a Sink detach from Attached.SRC.		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	A DRP that supports Charge-Through VCONN-Powered USB Device shall transition to CTUnattached.SNK if the connected device identifies itself as a Charge-Through VCONNPowered USB Device in its Discover Identity Command response. The DRP may delay this transition in order to perform further SOP' communication.		N/A
	A port shall cease to supply VBUS within tVBUSOFF of exiting Attached.SRC.		N/A
	A port that is supplying VCONN shall cease to supply it within tVCONNOFF of exiting Attached.SRC, unless it is exiting as a result of a USB PD PR_Swap or is transitioning into the CTUnattached.SNK state.		N/A
	After a USB PD PR_Swap is accepted (i.e., either an Accept message is received or acknowledged), a DRP shall transition directly to the Attached.SNK state (i.e., remove Rp from CC, assert Rd on CC and stop supplying VBUS) and maintain its current data role, connection and VCONN supply state.		N/A
	A Charge-Through VCONN-Powered USB Device shall transition to Unattached.SNK when VBUS falls below vSinkDisconnect or the Host-side port's CC pin is SRC.Open. The Charge- Through VCONN-Powered USB Device shall detect the SRC.Open state within tSRCDDisconnect, but should detect it as quickly as possible.		N/A
4.5.2.2.10	Try.SRC State		N/A
	When in the Try.SRC state, the port is querying to determine if the port partner supports the Sink role.		N/A
4.5.2.2.10.1	Try.SRC Requirements		N/A
	The port shall not drive VBUS or VCONN.		N/A
	The port shall source current on both the CC1 and CC2 pins independently.		N/A
	The port shall provide an Rp as specified in Table 4-24.		N/A
4.5.2.2.10.2	Exiting from Try.SRC State		N/A
	The port shall transition to Attached.SRC when the SRC.Rd state is detected on exactly one of the CC1 or CC2 pins for at least tTryCCDebounce.		N/A
	The port shall transition to TryWait.SNK after tDRPTry and the SRC.Rd state has not been detected and VBUS is within vSafe0V, or after tTryTimeout and the SRC.Rd state has not been detected.		N/A
4.5.2.2.11	TryWait.SNK State		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	When in the TryWait.SNK state, the port has failed to become a Source and is waiting to attach as a Sink. Alternatively the port is responding to the Sink being removed while in the Attached.SRC state.		N/A
4.5.2.2.11.1	TryWait.SNK Requirements		N/A
	The port shall not drive VBUS or VCONN.		N/A
	Both the CC1 and CC2 pins shall be independently terminated to ground through Rd.		N/A
4.5.2.2.11.2	Exiting from TryWait.SNK State		N/A
	The port shall transition to Attached.SNK after tCCDebounce if or when VBUS is detected. Note the Source may initiate USB PD communications which will cause brief periods of the SNK.Open state on both the CC1 and CC2 pins, but this event will not exceed tPDDebounce.		N/A
	The port shall transition to Unattached.SNK when the state of both of the CC1 and CC2 pins is SNK.Open for at least tPDDebounce.		N/A
4.5.2.2.12	Try.SNK State		N/A
	When in the Try.SNK state, the port is querying to determine if the port partner supports the Source role.		N/A
	When in the Try.SNK state, the Charge-Through VCONN-Powered USB Device is querying to determine if the port partner on the Host-side port supports the Source role.		N/A
4.5.2.2.12.1	Try.SNK Requirements		N/A
	The port shall not drive VBUS or VCONN.		N/A
	Both the CC1 and CC2 pins shall be independently terminated to ground through Rd.		N/A
	The Charge-Through VCONN-Powered USB Device shall isolate its Host-side port from its Charge-Through port, including CCs and VBUS. The Charge-Through VCONN-Powered USB Device shall ensure that it is powered by VBUS from the Charge-Through port.		N/A
	The Charge-Through VCONN-Powered USB Device shall remove its Rp termination (Default USB Power advertisement) on the Host-side port CC and provide an Rd termination to ground instead, as specified in Table 4-24 and remain to independently terminate its Charge-Through port's CC1 and CC2 pins to ground through Rd.		N/A
4.5.2.2.12.2	Exiting from Try.SNK State		N/A
	The port shall wait for tDRPtry and only then begin monitoring the CC1 and CC2 pins for the		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	SNK.Rp state.		
	The port shall then transition to Attached.SNK when the SNK.Rp state is detected on exactly one of the CC1 or CC2 pins for at least tTryCCDebounce and VBUS is detected.		N/A
	Alternatively, the port shall transition to TryWait.SRC if SNK.Rp state is not detected for tTryCCDebounce.		N/A
	The Charge-Through VCONN-Powered USB Device shall wait for tDRPTry and only then begin monitoring the Host-side port's CC pin for the SNK.Rp state.		N/A
	The Charge-Through VCONN-Powered USB Device shall wait for tDRPTry and only then begin monitoring the Host-side port's CC pin for the SNK.Rp state.		N/A
	Alternatively, the Charge-Through VCONN-Powered USB Device shall transition to TryWait.SRC if Host-side SNK.Rp state is not detected for tTryCCDebounce.		N/A
	A Sink with Accessory Support shall transition to Unsupported.Accessory if SNK.Rp state is not detected for tDRPTryWait.		N/A
4.5.2.2.13	TryWait.SRC State		N/A
	When in the TryWait.SRC state, the port has failed to become a Sink and is waiting to attach as a Source.		N/A
	When in the TryWait.SRC state, the Charge-Through VCONN-Powered USB Device has failed to become a Sink on its Host-side port and is waiting to attach as a Source on its Host-side port.		N/A
4.5.2.2.13.1	TryWait.SRC Requirements		N/A
	The requirements for this state are identical to Unattached.SRC.		N/A
4.5.2.2.13.2	Exiting from TryWait.SRC State		N/A
	The port shall transition to Attached.SRC when VBUS is at vSafe0V and the SRC.Rd state is detected on exactly one of the CC pins for at least tTryCCDebounce.		N/A
	The Charge-Through VCONN-Powered USB Device shall transition to Attached.SRC when host-side VBUS is at vSafe0V and the SRC.Rd state is detected on the Host-side port's CC pin for at least tTryCCDebounce.		N/A
	The port shall transition to Unattached.SNK after tDRPTry if neither of the CC1 or CC2 pins are in the SRC.Rd state.		N/A
	The Charge-Through VCONN-Powered USB Device shall transition to Unattached.SNK after tDRPTry if the Host-side port's CC pin is not in the SRC.Rd state.		N/A
4.5.2.2.14	Unattached.Accessory State		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
	The Unattached.Accessory state allows accessory-supporting Sinks to connect to audio or VCONN-Powered Accessories.		N/A
	This state is functionally equivalent to the Unattached.SRC state in a DRP, except that Attached.SRC is not supported.		N/A
4.5.2.2.14.1	Unattached.Accessory Requirements		N/A
	The port shall not drive VBUS or VCONN.		N/A
	The port shall source current on both the CC1 and CC2 pins independently.		N/A
	The port shall provide an Rp as specified in Table 4-24.		N/A
4.5.2.2.14.2	Exiting from Unattached.Accessory State		N/A
	A port that supports Audio Adapter Accessory Mode shall transition to AttachWait.Accessory when the state of both CC pins is SRC.Ra.		N/A
	A port that supports VCONN-Powered Accessories also shall transition to AttachWait.Accessory when the state of either CC1 or CC2 pin is SRC.Ra and the other CC pin is SRC.Rd.		N/A
	The maximum time the local port shall take to transition from Unattached.Accessory to the AttachWait.Accessory state when an Audio Adapter Accessory or VCONN-Powered Accessory is present is tOnePortToggleConnect.		N/A
	Otherwise, the port shall transition to Unattached.SNK within tDRPTransition after dcSRC.DRP · tDRP, or if directed.		N/A
4.5.2.2.15	AttachWait.Accessory State		N/A
	The AttachWait.Accessory state is used to ensure that the state of both of the CC1 and CC2 pins is stable after a cable is plugged in.		N/A
4.5.2.2.15.1	AttachWait.Accessory Requirements		N/A
	The requirements for this state are identical to Unattached.Accessory.		N/A
4.5.2.2.15.2	Exiting from AttachWait.Accessory State		N/A
	If the port supports Audio Adapter Accessory Mode, it shall transition to AudioAccessory when the state of both the CC1 and CC2 pins is SRC.Ra for at least tCCDebounce.		N/A
	The port shall transition to Unattached.SNK when the state of either the CC1 or CC2 pin is SRC.Open for at least tCCDebounce.		N/A
	If the port supports VCONN-Powered Accessories, it shall transition to PoweredAccessory state if the state of either the CC1 or CC2 pin is SRC.Rd and the other CC pin is SRC.Ra concurrently for at least		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
	tCCDebounce.		
4.5.2.2.16	AudioAccessory State		N/A
	The AudioAccessory state is used for the Audio Adapter Accessory Mode specified in Appendix A.		N/A
4.5.2.2.16.1	AudioAccessory Requirements		N/A
	The port shall reconfigure its pins as detailed in Appendix A.		N/A
	The port shall not drive VBUS or VCONN. A port that sinks current from the audio accessory over VBUS shall not draw more than 500 mA.		N/A
	The port shall provide an Rp as specified in Table 4-24.		N/A
	The port shall source current on at least one of the CC1 or CC2 pins and monitor to detect when the state is no longer SRC.Ra. If the port sources and monitors only one of CC1 or CC2, then it shall ensure that the termination on the unmonitored CC pin does not affect the monitored signal when the port is connected to an Audio Accessory that may short both CC1 and CC2 pins together.		N/A
4.5.2.2.16.2	Exiting from AudioAccessory State		N/A
	If the port is a Sink, the port shall transition to Unattached.SNK when the state of the monitored CC1 or CC2 pin(s) is SRC.Open for at least tCCDebounce.		N/A
	If the port is a Source or DRP, the port shall transition to Unattached.SRC when the state of the monitored CC1 or CC2 pin(s) is SRC.Open for at least tCCDebounce.		N/A
4.5.2.2.17	UnorientedDebugAccessory.SRC		N/A
	The UnorientedDebugAccessory.SRC state is used for the Debug Accessory Mode specified in Appendix B.		N/A
4.5.2.2.17.1	UnorientedDebugAccessory.SRC Requirements		N/A
	This mode is for debug only and shall not be used for communicating with commercial products.		N/A
	The port shall provide an Rp as specified in Table 4-24 on both the CC1 and CC2 pins and monitor to detect when the state of either is SRC.Open.		N/A
	The port shall supply VBUS current at the level it advertises on Rp. The port shall not drive VCONN.		N/A
	The port may connect any non-orientation specific debug signals for Debug Accessory Mode operation only after entry to this state.		N/A
4.5.2.2.17.2	Exiting from UnorientedDebugAccessory.SRC		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	State		
	If the port is a Source, the port shall transition to Unattached.SRC when the SRC.Open state is detected on either the CC1 or CC2 pin.		N/A
	If the port is a DRP, the port shall transition to Unattached.SNK when the SRC.Open state is detected on either the CC1 or CC2 pin.		N/A
	The port shall transition to OrientedDebugAccessory.SRC state if orientation is required and detected as described in Section B.2.6.1.2.		N/A
4.5.2.2.18	OrientedDebugAccessory.SRC State		N/A
	The OrientedDebugAccessory.SRC state is used for the Debug Accessory Mode specified in Appendix B.		N/A
4.5.2.2.18.1	OrientedDebugAccessory.SRC State Requirements		N/A
	This mode is for debug only and shall not be used for communicating with commercial products.		N/A
	The port shall provide an Rp as specified in Table 4-24 on both the CC1 and CC2 pins and monitor to detect when the state of either is SRC.Open.		N/A
	The port shall supply VBUS current at the level it advertises on Rp. The port shall not drive VCONN.		N/A
	The port shall connect any orientation specific debug signals for Debug Accessory Mode operation only after entry to this state. Any non-orientation specific debug signals for Debug Accessory Mode operation shall be connected or remain connected in this state.		N/A
	If the port needs to establish USB PD communications, it shall do so only after entry to this state. The port shall not initiate any USB PD communications until VBUS reaches vSafe5V. In this state, the port takes on the initial USB PD role of DFP/Source.		N/A
4.5.2.2.18.2	Exiting from OrientedDebugAccessory.SRC State		N/A
	If the port is a Source, the port shall transition to Unattached.SRC when the SRC.Open state is detected on either the CC1 or CC2 pin.		N/A
	If the port is a DRP, the port shall transition to Unattached.SNK when the SRC.Open state is detected on either the CC1 or CC2 pin.		N/A
4.5.2.2.19	DebugAccessory.SNK		N/A
	The DebugAccessory.SNK state is used for the Debug Accessory Mode specified in Appendix B.		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
4.5.2.2.19.1	DebugAccessory.SNK Requirements		N/A
	This mode is for debug only and shall not be used for communicating with commercial products.		N/A
	The port shall not drive VBUS or VCONN.		N/A
	The port shall provide an Rd as specified in Table 4-25 on both the CC1 and CC2 pins and monitor to detect when the state of either is SRC. Open.		N/A
	If supported, orientation is determined as outlined in Section B.2.6.1.1. The port shall connect any debug signals for Debug Accessory Mode operation only after entry to this state.		N/A
4.5.2.2.19.2	Exiting from DebugAccessory.SNK State		N/A
	The port shall transition to Unattached.SNK when VBUS is no longer present.		N/A
4.5.2.2.20	PoweredAccessory State		N/A
	When in the PoweredAccessory state, the port is powering a VCONN-Powered Accessory or VCONN-Powered USB Device.		N/A
4.5.2.2.20.1	PoweredAccessory Requirements		N/A
	If the port needs to determine the orientation of the connector, it shall do so only upon entry to the PoweredAccessory state by detecting which of the CC1 or CC2 pins is connected through the cable (i.e., which CC pin is in the SRC.Rd state).		N/A
	The SRC.Rd state is detected on only one of the CC1 or CC2 pins. The port shall advertise either 1.5 A or 3.0 A (see Table 4-24) on this CC pin and monitor its state.		N/A
	The port shall supply VCONN on the unused CC pin within tVconnON-PA of entering the PoweredAccessory state.		N/A
	The port shall not drive VBUS.		N/A
	When the port initially enters the PoweredAccessory state it shall operate as a USB Power Delivery Source with a DFP data role. In addition, the port shall support at least one of the following:		N/A
	Use USB PD to establish an explicit contract and then use Structured Vendor Defined Messages (Structured VDMs) to identify a VCONN-Powered Accessory and enter an Alternate Mode.		N/A
	Use USB PD to query the identity of a VCONN-Powered USB Device (that operates as a cable plug responding to SOP').		N/A
4.5.2.2.20.2	Exiting from PoweredAccessory State		N/A
	The port shall transition to Unattached.SNK		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	when the SRC. Open state is detected on the monitored CC pin.		
	The port shall transition to Try.SNK if the attached device is not a VCONN-Powered Accessory or VCONN-Powered USB Device. For example, the attached device does not support USB PD or does not respond to USB PD commands required for a VCONN-Powered Accessory (e.g., Discover SVIDs, Discover Modes, etc.) or is a Sink or DRP attached through a Powered Cable.		N/A
	The port shall transition to Unsupported.Accessory if the attached device is a VCONN-Powered Accessory but the port has not successfully entered an Alternate Mode within tAMETimeout (see Appendix E).		N/A
	A port that supports Charge-Through VCONN-Powered USB Device shall transition to CTUnattached.SNK if the connected device identifies itself as a Charge-Through VCONNPowered USB Device in its Discover Identity Command response. The port may delay this transition in order to perform further SOP' communication.		N/A
	The port shall cease to supply VCONN within tVCONNOff of exiting the PoweredAccessory state unless it is transitioning into the CTUnattached.SNK state.		N/A
4.5.2.2.21	Unsupported.Accessory State		N/A
	If a VCONN-Powered Accessory does not enter an Alternate Mode, the Unsupported.Accessory state is used to wait until the accessory is unplugged before continuing.		N/A
4.5.2.2.21.1	Unsupported.Accessory Requirements		N/A
	Only one of the CC1 or CC2 pins shall be in the SRC.Rd state. The port shall advertise Default USB Power (see Table 4-24) on this CC pin and monitor its voltage.		N/A
	The port shall not drive VBUS or VCONN.		N/A
	A Sink with either VCONN-Powered Accessory or VCONN-Powered USB Device support shall provide user notification that it does not recognize or support the attached accessory or device.		N/A
4.5.2.2.21.2	Exiting from Unsupported.Accessory		N/A
	The port shall transition to Unattached.SNK when the SRC. Open state is detected on the monitored CC pin.		N/A
4.5.2.2.22	CTUnattached.VPD State		N/A
	When in the CTUnattached.VPD state, the Charge-Through VCONN-Powered USB Device has detected SNK.Open on its host port		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	for tVPDCTDD, indicating that it is connected to a Charge-Through capable Source, and is independently monitoring its Charge-Through port for the presence of a pass-through Power Source.		
	This state may also have been entered through detach of a Power Source on the Charge-Through port or detach of a sink from the CTVPD's Charge-through port.		N/A
4.5.2.2.22.1	CTUnattached.VPD Requirements		N/A
	The Charge-Through VCONN-Powered USB Device shall isolate its Host-side port from its Charge-Through port, including CCs and VBUS. The Charge-Through VCONN-Powered USB Device shall ensure that it is powered by VCONN, does not consume more than ICCS (USB 3.2) / ICCSH (USB 2.0) from VBUS for monitoring, and is sufficiently isolated from VBUS to tolerate high voltages during Charge-Through operation.		N/A
	Upon entry into this state, the device shall remove its Rd termination to ground (if present) on the Host-side port CC and provide an Rp termination advertising 3.0 A instead, as specified in Table 4-24. Note that because VBUS is not provided, the Rp termination signals continued connection to the port partner but does not carry with it any current advertisement.		N/A
	The Charge-Through VCONN-Powered USB Device shall only respond to USB PD Discover Identity queries on SOP' on its Host-side port. It shall ensure there is sufficient capacitance on the Host-side port CC to meet cReceiver as defined in USB PD.		N/A
	The Charge-Through VCONN-Powered USB Device shall independently terminate both the Charge-Through port's CC1 and CC2 pins to ground through Rd.		N/A
	The Charge-Through VCONN-Powered USB Device shall provide a bypass capacitance of CCTB on the Charge-Through Port's VBUS pins.		N/A
4.5.2.2.22.2	Exiting from CTUnattached.VPD		N/A
	The Charge-Through VCONN-Powered USB Device shall transition to CTAttachWait.VPD when a Source connection is detected on the Charge-Through port, as indicated by the SNK.Rp state on exactly one of the Charge-Through port's CC pins.		N/A
	Debug accessories are not supported on the Charge-Through port.		N/A
	The Charge-Through VCONN-Powered USB Device shall transition to Unattached.SNK if		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
	VCONN falls below vVCONNDisconnect.		
	The Charge-Through VCONN-Powered USB Device shall transition to CTUnattached. Unsupported within tDRPTransition after the state of both the Charge-Through port's CC1 and CC2 pins is SNK.Open for tDRP – dcSRC.DRP · tDRP, or if directed.		N/A
4.5.2.2.23	CTAttachWait.VPD State		N/A
	When in the CTAttachWait.VPD state, the device has detected the SNK.Rp state on exactly one of its Charge-Through port's CC pins and is waiting for VBUS on the Charge-Through port.		N/A
4.5.2.2.23.1	CTAttachWait.VPD Requirements		N/A
	The Charge-Through VCONN-Powered USB Device shall isolate its Host-side port from its Charge-Through port, including CCs and VBUS. The Charge-Through VCONN-Powered USB Device shall ensure that it is powered by VCONN, does not consume more than ICCS (USB 3.2) / ICCSH (USB 2.0) from VBUS for monitoring, and is sufficiently isolated from VBUS to tolerate high voltages during Charge-Through operation.		N/A
	The Charge-Through VCONN-Powered USB Device shall maintain its Rp termination advertising 3.0 A on the Host-side port's CC pin, as well as the independent terminations to ground through Rd on the Charge-Through port's CC1 and CC2 pins.		N/A
	The Charge-Through VCONN-Powered USB Device shall only respond to USB PD Discover Identity queries on SOP' on its Host-side port, and complete any active queries prior to exiting this state. It shall ensure there is sufficient capacitance on the Host-side port CC to meet cReceiver as defined in USB PD.		N/A
4.5.2.2.23.2	Exiting from CTAttachWait.VPD		N/A
	The Charge-Through VCONN-Powered USB Device shall transition to CTUnattached.VPD when the state of both the Charge-Through port's CC1 and CC2 pins are SNK.Open for at least tPDDebounce.		N/A
	The Charge-Through VCONN-Powered USB Device shall transition to CTAttached.VPD after the state of only one of the Charge-Through port's CC1 or CC2 pins is SNK.Rp for at least tCCDebounce and VBUS on the Charge-Through port is detected.		N/A
	Note the Charge-Through Source may initiate USB PD communications which will cause brief periods of the SNK.Open state on one of the Charge-Through port's CC pins with the state of the Charge-Through port's other CC pin		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
	remaining SNK.Open, but this event will not exceed tPDDebounce.		
	The Charge-Through VCONN-Powered USB Device shall transition to CTDisabled.VPD if VCONN falls below vVCONNDisconnect.		N/A
4.5.2.2.24	CTAttached.VPD State		N/A
	When in the CTAttached.VPD state, the Charge-Through VCONN-Powered USB Device has detected a Power Source on its Charge-Through port and has connected the Charge-Through port's CC and VBUS pins directly to the Host-side port's CC and VBUS pins. Hence all power delivery, negotiation and USB PD communication are performed directly between the unit on Host-side port and the Power Source connected to the Charge-Through port.		N/A
4.5.2.2.24.1	CTAttached.VPD Requirements		N/A
	Upon entry to this state, the Charge-Through VCONN-Powered USB Device shall detect which of the Charge-Through port's CC1 or CC2 pins is connected through the cable (i.e., the CC pin that is in the SNK.Rp state). The device shall then immediately, in the following order:		N/A
	1. Remove or reduce any additional capacitance on the Host-side CC port that was introduced in order to meet cReceiver as defined in USB PD to present on CC a value equal to or less than two times the maximum value for cCablePlug_CC.		N/A
	2. Disable the Rp termination advertising 3.0 A on the host port's CC pin.		N/A
	3. Passively multiplex the detected Charge-Through port's CC pin through to the host port's CC pin with an impedance of less than RccCON.		N/A
	4. Disable the Rd on the Charge-Through port's CC1 and CC2 pins.		N/A
	5. Connect the Charge-Through port's VBUS through to the host port's VBUS.		N/A
	These steps shall be completed within tVPDDetach minimum of entering this state.		N/A
	The Charge-Through VCONN-Powered USB Device shall ensure that it is powered by VCONN, does not consume more than ICCS (USB 3.2) / ICCSH (USB 2.0) from VBUS for monitoring, and is sufficiently isolated from VBUS to tolerate high voltages during Charge-Through operation.		N/A
	The Charge-Through VCONN-Powered USB Device shall not respond to any USB PD communication on any CC pin in this state. Any		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	active queries on SOP' shall have been completed prior to entering this state.		
4.5.2.2.24.2	Exiting from CTAttached.VP		N/A
	The Charge-Through VCONN-Powered USB Device shall transition to CTUnattached.VPD when VBUS falls below vSinkDisconnect and the state of the passed-through CC pin is SNK. Open for tVPDCTDD.		N/A
	The Charge-Through VCONN-Powered USB Device shall transition to CTDIsabled. VPD if VCONN falls below vVCONNDISconnect.		N/A
4.5.2.2.25	CTDisabled.VPD State		N/A
	When in the CTDIsabled.VPD state, the Charge-Through VCONN-Powered USB Device has detected the detach on its Host-side port but may still potentially be connected to a Power Source on the Charge-Through port, and is thus ensuring that the VBUS from the Power Source is removed.		N/A
4.5.2.2.25.1	CTDisabled.VPD Requirements		N/A
	The Charge-Through VCONN-Powered USB Device shall isolate its Host-side port from its Charge-Through port, including CCs and VBUS.		N/A
	The device shall present a high-impedance to ground (above zOPEN) on the Host-side port's CC pin and on the Charge-Through port CC1 and CC2 pins.		N/A
	The Charge-Through VCONN-Powered USB Device shall ensure that it is powered entirely by VBUS.		N/A
4.5.2.2.25.2	Exiting from CTDIsabled.VPD		N/A
	The Charge-Through VCONN-Powered USB Device shall transition to Unattached.SNK after tVPDDisable.		N/A
4.5.2.2.26	CTUnattached.SNK State		N/A
	When in the CTUnattached.SNK state, the port has detected that it is attached to a Charge-Through VCONN-Powered USB Device and is ready if a Power Source is attached to the Charge-Through VCONN-Powered USB Device.		N/A
	This state may also have been entered through detach of a Charge-Through Power Source.		N/A
4.5.2.2.26.1	CTUnattached.SNK Requirements		N/A
	Upon entry to this state, the port shall remove its Rp termination (if present) and terminate CC to ground through Rd.		N/A
	The port shall continue to supply VCONN.		N/A
	The port shall stop sourcing or sinking VBUS and discharge it.		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	In USB PD Version 2.0, the port shall initiate PD messages.		N/A
	The port may query the state of the attached VCONN-Powered USB Device by sending SOP' messages on USB PD to read the VPD's eMarker.		N/A
4.5.2.2.26.2	Exiting from CTUnattached.SNK		N/A
	The port shall transition to CTAttached.SNK when VBUS is detected. Note that by this point, the VCONN-Powered USB Device has already de-bounced the passed-through CC pin.		N/A
	The port shall transition to Unattached.SNK if the state of the CC pin is SNK. Open for tVPDDetach after VBUS is vSafe0V.		N/A
4.5.2.2.27	CTAttached.SNK State		N/A
	When in the CTAttached.SNK state, the port is connected to a Charge-Through VCONN-Powered USB Device, which in turn is passing through the connection to a Power Source.		N/A
4.5.2.2.27.1	CTAttached.SNK Requirements		N/A
	The port shall continue to terminate CC to ground through Rd. Since there is now a Power Source connected through to VBUS and CC, the port shall operate in one of the Sink Power Sub-States shown in Figure 4-19, and remain within the Sink Power Sub-States, until either VBUS is removed or a USB PD contract is established with the source.		N/A
	The port shall not negotiate a voltage on VBUS higher than the maximum voltage specified in the Charge-Through VCONN-Powered USB Device's Discover Identity Command response.		N/A
	The port shall continue to supply VCONN.		N/A
	The port shall reject a VCONN swap request.		N/A
	The port shall not perform USB BC 1.2 primary detection, as that will interfere with VPD functionality.		N/A
	In USB PD Version 2.0, the port shall not initiate USB PD messages, although it remains a DFP for USB data.		N/A
	The port shall neither initiate nor respond to any SOP' communication.		N/A
	The port shall meet the Sink Power Sub-State requirements specified in Section 4.5.2.2.29.		N/A
	The port shall meet the additional maximum current constraints described in Section 4.6.2.5.		N/A
	The port shall follow the restrictions on USB PD messages described in Section 4.10.2.		N/A
	The port shall alter its advertised capabilities to UFP role/sink only role as described in Section		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	4.10.2.		
4.5.2.2.27.2	Exiting from CTAttached.SNK		N/A
	A port that is not in the process of a USB PD Hard Reset shall transition to CTUnattached.SNK within tSinkDisconnect when VBUS falls below vSinkDisconnect for VBUS operating at or below 5 V or below vSinkDisconnectPD when negotiated by USB PD to operate above 5 V.		N/A
	A port that has entered into USB PD communications with the Source and has seen the CC voltage exceed vRd-USB may monitor the CC pin to detect cable disconnect in addition to monitoring VBUS.		N/A
	A port that is monitoring the CC voltage for disconnect shall transition to CTUnattached.SNK within tSinkDisconnect after the CC voltage remains below vRd-USB for tPDDebounce.		N/A
4.5.2.2.28	CTUnattached.Unsupported State		N/A
	When in the CTUnattached.Unsupported state, the Charge-Through VCONN-Powered USB Device has previously detected SNK. Open on its host port for tVPDCTDD, indicating that it is connected to a Charge-Through Capable Source, and is now monitoring its Charge-Through port for the presence of an unsupported sink.		N/A
	A Charge-Through VCONN-Powered USB Device does not support Sinks, Debug Accessory Mode, or Audio Adapter Accessory Mode.		N/A
4.5.2.2.28.1	CTUnattached.Unsupported Requirements		N/A
	The Charge-Through VCONN-Powered USB Device shall isolate its Host-side port from its Charge-Through port, including CCs and VBUS. The Charge-Through VCONN-Powered USB Device shall ensure that it is powered by VCONN, does not consume more than ICCS (USB 3.2) / ICCSH (USB 2.0) from VBUS for monitoring, and is sufficiently isolated from VBUS to tolerate high voltages during Charge-Through operation.		N/A
	Upon entry into this state, the Charge-Through VCONN-Powered USB Device shall maintain its Rp termination advertising 3.0 A on the Host-side port's CC pin, remove its Rd terminations to ground on the Charge-Through port's CC1 and CC2 pins, and provide a Rp termination advertising Default USB Power instead.		N/A
	The Charge-Through VCONN-Powered USB Device shall only respond to USB PD Discover Identity queries on SOP' on its Host-side port. It shall ensure there is sufficient capacitance on		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	the Host-side port CC to meet cReceiver as defined in USB PD.		
4.5.2.2.28.2	Exiting from CTUnattached.Unsupported		N/A
	The Charge-Through VCONN-Powered USB Device shall transition to CTAttachWait.Unsupported when a Sink connection is detected on the Charge-Through port, as indicated by the SRC.Rd state on at least one of the Charge-Through port's CC pins or SRC.Ra state on both the CC1 and CC2 pins.		N/A
	The Charge-Through VCONN-Powered USB Device shall transition to Unattached.SNK if VCONN falls below vVCONNDDisconnect.		N/A
	Otherwise, a Charge-Through VCONN-Powered USB Device shall transition to CTUnattached.VPD within tDRPTransition after dcSRC.DRP · tDRP, or if directed.		N/A
4.5.2.2.29	CTAttachWait.Unsupported State		N/A
	The CTAttachWait.Unsupported state is used to ensure that the state of both the Charge-Through Port's CC1 and CC2 pins are stable for at least tCCDebounce.		N/A
4.5.2.2.29.1	CTAttachWait.Unsupported Requirements		N/A
	The requirements for this state are identical to CTUnattached.Unsupported state.		N/A
4.5.2.2.29.2	Exiting from CTAttachWait.Unsupported		N/A
	The Charge-Through VCONN-Powered USB Device shall transition to CTTry.SNK if the state of at least one of the Charge-Through port's CC pins is SRC.Rd, or if the state of both the CC1 and CC2 pins is SRC.Ra for at least tCCDebounce.		N/A
	The Charge-Through VCONN-Powered USB Device shall transition to CTUnattached.VPD when the state of either the Charge-Through Port's CC1 or CC2 pin is SRC.Open for at least tCCDebounce.		N/A
	The Charge-Through VCONN-Powered USB Device shall transition to Unattached.SNK if VCONN falls below vVCONNDDisconnect.		N/A
4.5.2.2.30	CTTry.SNK State		N/A
	When in the CTTry.SNK state, the Charge-Through VCONN-Powered USB Device is querying to determine if the port partner on the Charge-Through port supports the source role.		N/A
4.5.2.2.30.1	CTTry.SNK Requirements		N/A
	The requirements for this state are identical to CTUnattached.VPD state.		N/A
4.5.2.2.30.2	Exiting from CTTry.SNK		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
	The Charge-Through VCONN-Powered USB Device shall wait for tDRPTry and only then begin monitoring the Charge-Through port's CC pins for the SNK.Rp state.		N/A
	The Charge-Through VCONN-Powered USB Device shall then transition to CTAttached.VPD when the SNK.Rp state is detected on the Charge-Through port's CC pins for at least tTryCCDebounce and VBUS is detected on Charge-Through port.		N/A
	A Charge-Through VCONN-Powered USB Device shall transition to CTAttached. Unsupported if SNK.Rp state is not detected for tDRPTryWait.		N/A
	The Charge-Through VCONN-Powered USB Device shall transition to Unattached.SNK if VCONN falls below vVCONNDisconnect.		N/A
4.5.2.2.31	CTAttached.Unsupported State		N/A
	If the port partner to the Charge-Through VCONN-Powered USB Device's Charge-Through port either does not support the source power role, or failed to negotiate the source role, the CTAttached.Unsupported state is used to wait until that device is unplugged before continuing.		N/A
4.5.2.2.31.1	CTAttached.Unsupported Requirements		N/A
	The Charge-Through VCONN-Powered USB Device shall isolate its Host-side port from its Charge-Through port, including CCs and VBUS. The Charge-Through VCONN-Powered USB Device shall ensure that it is powered by VCONN, does not consume more than ICCS (USB 3.2) / ICCSH (USB 2.0) from VBUS for monitoring, and is sufficiently isolated from VBUS to tolerate high voltages during Charge-Through operation.		N/A
	Upon entry into this state, the Charge-Through VCONN-Powered USB Device shall maintain its Rp termination advertising 3.0 A on the Host-side port's CC pin, remove its Rd terminations to ground on the Charge-Through port's CC1 and CC2 pins, and provide a Rp termination advertising Default USB Power instead.		N/A
	At least one of the CC1 or CC2 pins will be in the SRC.Rd state or both will be in the SRC.Ra state. The Charge-Through port shall advertise Default USB Power (see Table 4-24) on its CC pins and monitor their voltage.		N/A
	The Charge-Through VCONN-Powered USB Device shall present a USB Billboard Device Class interface indicating that it does not recognize or support the attached accessory or device.		N/A
4.5.2.2.31.2	Exiting from CTAttached. Unsupported		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
	The Charge-Through VCONN-Powered USB Device shall transition to CTUnattached.VPD when SRC. Open state is detected on both the Charge-Through port's CC pins or the SRC. Open state is detected on one CC pin and SRC.Ra is detected on the other CC pin.		N/A
4.5.2.3	Sink Power Sub-State Requirements		N/A
	When in the Attached.SNK or CTAttached.SNK states and the Source is supplying default VBUS, the port shall operate in one of the sub-states shown in Figure 4-19. The initial Sink Power Sub-State is PowerDefault.SNK. Subsequently, the Sink Power Sub-State is determined by Source's USB Type-C current advertisement. The port in Attached.SNK shall remain within the Sink Power Sub-States until either VBUS is removed or a USB PD contract is established with the Source.		N/A
	The Sink is only required to implement Sink Power Sub-State transitions if the Sink wants to consume more than default USB current.		N/A
	Note that for the CTAttached.SNK state, there are further limitations on maximum current (see Section 4.6.2.5).		N/A
4.5.2.3.1	PowerDefault.SNK Sub-State		N/A
	This sub-state supports Sinks consuming current within the lowest range (default) of Sourcesupplied current.		N/A
4.5.2.3.1.1	PowerDefault.SNK Requirements		N/A
	The port shall draw no more than the default USB power from VBUS. See Section 4.6.2.1.		N/A
	If the port wants to consume more than the default USB power, it shall monitor vRd to determine if more current is available from the Source.		N/A
4.5.2.3.1.2	Exiting from PowerDefault.SNK		N/A
	For any change in vRd indicating a change in allowable power, the port shall not transition until the new vRd has been stable for at least tRpValueChange.		N/A
	For a vRd in the vRd-1.5 range, the port shall transition to the Power1.5.SNK Sub-State.		N/A
	For a vRd in the vRd-3.0 range, the port shall transition to the Power3.0.SNK Sub-State.		N/A
4.5.2.3.2	Power1.5.SNK Sub-State		N/A
	This sub-state supports Sinks consuming current within the two lower ranges (default and 1.5 A) of Source-supplied current.		N/A
4.5.2.3.2.1	Power1.5.SNK Requirements		N/A
	The port shall draw no more than 1.5 A from		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	VBUS.		
	The port shall monitor vRd while it is in this sub-state.		N/A
4.5.2.3.2.2	Exiting from Power1.5.SNK		N/A
	For any change in vRd indicating a change in allowable power, the port shall not transition until the new vRd has been stable for at least tRpValueChange.		N/A
	For a vRd in the vRd-USB range, the port shall transition to the PowerDefault.SNK Sub-State and reduce its power consumption to the new range within tSinkAdj.		N/A
	For a vRd in the vRd-3.0 range, the port shall transition to the Power3.0.SNK Sub-State.		N/A
4.5.2.3.3	Power3.0.SNK Sub-State		N/A
	This sub-state supports Sinks consuming current within all three ranges (default, 1.5 A and 3.0 A) of Source-supplied current.		N/A
4.5.2.3.3.1	Power3.0.SNK Requirements		N/A
	The port shall draw no more than 3.0 A from VBUS.		N/A
	The port shall monitor vRd while it is in this sub-state.		N/A
4.5.2.3.3.2	Exiting from Power3.0.SNK		N/A
	For any change in vRd indicating a change in allowable power, the port shall not transition until the new vRd has been stable for at least tRpValueChange.		N/A
	For a vRd in the vRd-USB range, the port shall transition to the PowerDefault.SNK Sub-State and reduce its power consumption to the new range within tSinkAdj.		N/A
	For a vRd in the vRd-1.5 range, the port shall transition to the Power1.5.SNK Sub-State and reduce its power consumption to the new range within tSinkAdj.		N/A
4.5.2.4	Cable eMarker State Machine Requirements		N/A
4.5.2.4.1	Cable Power On State		N/A
4.5.2.4.1.1	Cable Power On State Requirements		N/A
	Each eMarker in the cable shall power on.		N/A
	The cable shall not respond to SOP' and SOP" commands in this state.		N/A
4.5.2.4.1.2	Exiting from Cable Power On State		N/A
	Each eMarker in a passive or active cable shall transition to Assign Cable SOP* when it has completed its boot process. Each eMarker shall transition to Assign Cable SOP* within tVCONNStable.		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
4.5.2.4.2	Respond to SOP'/' State		N/A
	A passive cable has only one eMarker powered at a time. This cable eMarker in a passive cable shall respond to SOP' in this state.		N/A
	Each cable eMarker in an active cable shall respond to a pre-set SOP' or SOP''. If only one eMarker exists in the cable, it shall only respond to SOP'.		N/A
	Cable designers shall ensure that the eMarker works correctly in the presence of ground and VCONN maximum IR drop.		N/A
4.5.2.4.2.1	Respond to SOP' /'' State Requirements		N/A
	Each eMarker in the passive or active cable shall be able to respond to any USB PD communication sent to its pre-set SOP' or SOP''. For a passive cable, only one eMarker should be powered at a time and shall respond to SOP' only. If two eMarkers exist in a passive or active cable and are powered at the same time, then only one shall respond to SOP' and the other shall respond to SOP''. The assignment of SOP' and SOP'' is fixed for each eMarker in a cable and shall not be dynamically set when power is applied to VCONN.		N/A
4.5.2.4.2.2	Exiting from Respond to SOP' /'' State		N/A
	Each eMarker in the cable shall transition to Cable Power On upon sensing VCONN less than vVconnDisconnect or upon a Power On Reset event.		N/A
	Each eMarker in the cable shall transition to Cable Power On upon sensing a Hard Reset or Cable Reset.		N/A
4.5.2.5	Cable Ra Management State Machine Requirements		N/A
4.5.2.5.1	Ra Applied State		N/A
	This state appears in Figure 4-22. This is the initial state at power on for each eMarker in the cable.		N/A
4.5.2.5.1.1	Ra Applied State Requirements		N/A
	Each eMarker in the cable shall apply Ra to VCONN within tRaReconnect.		N/A
4.5.2.5.1.2	Exiting from Ra Applied State		N/A
	Each eMarker in a passive or active cable shall transition to the Ra Weakened state when VCONN is greater than vVCONNDISCONNECT for tRaWeaken.		N/A
4.5.2.5.2	Ra Weakened State		N/A
4.5.2.5.2.1	Ra Weakened State Requirements		N/A
	The eMarker in the cable shall remove or weaken Ra.		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	Passive cables shall meet the Power for electronically marked passive cables defined in Table 4-6. Active cables shall meet the Power for Active Cables in Table 4-6.		N/A
4.5.2.5.2.2	Exiting from Ra Weakened State		N/A
	Each eMarker in a passive or active cable shall transition to the Ra Applied state when VCONN is below vVCONNDisconnect.		N/A
4.5.2.6	Connection States Summary		N/A
<b>4.5.3</b>	<b>USB Port Interoperability Behavior</b>		N/A
	This section describes interoperability behavior between USB Type-C to USB Type-C ports and between USB Type-C to legacy USB ports.		N/A
4.5.3.1	USB Type-C Port to USB Type-C Port Interoperability Behaviors		N/A
	The following sub-sections describe typical port-to-port interoperability behaviors for the various combinations of USB Type-C Source, Sink and DRPs as presented in Table 4-9. In all of the described behaviors, the impact of USB PD-based swaps (PR_Swap, DR_Swap or VCONN_Swap) are not considered.		N/A
	The figures in the following sections illustrate the CC1 and CC2 routing after the CC detection process is complete.		N/A
4.5.3.1.1	Source to Sink Behavior		N/A
	Figure 4-23 illustrates the functional model for a Source connected to a Sink. The single CC wire that is in a standard cable is only shown in one of the four possible connection routes, CC1 to CC1.		N/A
	The following describes the behavior when a Source is connected to a Sink.		N/A
	1. Source and Sink in the unattached state		N/A
	2. Source transitions from Unattached.SRC to Attached.SRC through AttachWait.SRC		N/A
	Source detects the Sink's pull-down on CC and enters Attached.SRC through AttachWait.SRC		N/A
	Source turns on VBUS and VCONN		N/A
	3. Sink transitions from Unattached.SNK to Attached.SNK through AttachWait.SNK. Sink may skip AttachWait.SNK if it is USB 2.0 only and does not support accessories.		N/A
	Sink detects VBUS and enters Attached.SNK through AttachWait.SNK		N/A
	4. While the Source and Sink are in the attached state:		N/A
	Source adjusts Rp as needed to limit the current the Sink may draw		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	Sink detects and monitors vRd for available current on VBUS		N/A
	Source monitors CC for detach and when detected, enters Unattached.SRC		N/A
	Sink monitors VBUS for detach and when detected, enters Unattached.SNK		N/A
4.5.3.1.2	Source to DRP Behavior		N/A
	Figure 4-24 illustrates the functional model for a Source connected to a DRP. The single CC wire that is in a standard cable is only shown in one of the four possible connection routes, CC1 to CC1.		N/A
	The following describes the behavior when a Source is connected to a DRP.		N/A
	1. Source and DRP in the unattached state		N/A
	DRP alternates between Unattached.SRC and Unattached.SNK		N/A
	2. Source transitions from Unattached.SRC to Attached.SRC through AttachWait.SRC		N/A
	Source detects the DRP's pull-down on CC and enters AttachWait.SRC. After tCCDebounce it then enters Attached.SRC.		N/A
	Source turns on VBUS and VCONN		N/A
	3. DRP transitions from Unattached.SNK to Attached.SNK through AttachWait.SNK		N/A
	DRP in Unattached.SNK detects pull up on CC and enters AttachWait.SNK. After that state persists for tCCDebounce and it detects VBUS, it enters Attached.SNK.		N/A
	4. While the Source and DRP are in their respective attached states:		N/A
	Source adjusts Rp as needed to limit the current the DRP (as Sink) may draw		N/A
	DRP (as Sink) detects and monitors vRd for available current on VBUS		N/A
	Source monitors CC for detach and when detected, enters Unattached.SRC		N/A
	DRP (as Sink) monitors VBUS for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)		N/A
4.5.3.1.3	DRP to Sink Behavior		N/A
	Figure 4-25 illustrates the functional model for a DRP connected to a Sink. The single CC wire that is in a standard cable is only shown in one of the four possible connection routes, CC1 to CC1.		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	The following describes the behavior when a DRP is connected to a Sink.		N/A
	1. DRP and Sink in the unattached state		N/A
	DRP alternates between Unattached.SRC and Unattached.SNK		N/A
	2. DRP transitions from Unattached.SRC to AttachWait.SRC to Attached.SRC		N/A
	DRP in Unattached.SRC detects one of the CC pull-downs of Sink which is in Unattached.SNK and DRP enters AttachWait.SRC		N/A
	DRP in AttachWait.SRC detects that pull down on CC persists for tCCDebounce. It then enters Attached.SRC and turns on VBUS and VCONN		N/A
	3. Sink transitions from Unattached.SNK to Attached.SNK through AttachWait.SNK if required.		N/A
	Sink detects VBUS and enters Attached.SNK		N/A
	4. While the DRP and Sink are in their respective attached states:		N/A
	DRP (as Source) adjusts Rp as needed to limit the current the Sink may draw		N/A
	Sink detects and monitors vRd for available current on VBUS		N/A
	DRP (as Source) monitors CC for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)		N/A
	Sink monitors VBUS for detach and when detected, enters Unattached.SNK		N/A
4.5.3.1.4	DRP to DRP Behavior		N/A
	Two behavior descriptions based on the connection state diagrams are provided below. In the first case, the two DRPs accept the resulting Source-to-Sink relationship achieved randomly whereas in the second case the DRP #2 chooses to drive the random result to the opposite result using the Try.SRC mechanism.		N/A
	Figure 4-26 illustrates the functional model for a DRP connected to a DRP in the first case described. The single CC wire that is in a standard cable is only shown in one of the four possible connection routes, CC1 to CC1. Port numbers have been arbitrarily assigned in the diagram to assist the reader to understand the process description.		N/A
	CASE 1: The following describes the behavior when a DRP is connected to another DRP. In this flow, the two DRPs accept the resulting Source-to-Sink relationship achieved randomly.		N/A
	1. Both DRPs in the unattached state		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
	DRP #1 and DRP #2 alternate between Unattached.SRC and Unattached.SNK		N/A
	2. DRP #1 transitions from Unattached.SRC to AttachWait.SRC		N/A
	DRP #1 in Unattached.SRC detects a CC pull down of DRP #2 in Unattached.SNK and enters AttachWait.SRC		N/A
	3. DRP #2 transitions from Unattached.SNK to AttachWait.SNK		N/A
	DRP #2 in Unattached.SNK detects pull up on a CC and enters AttachWait.SNK		N/A
	4. DRP #1 transitions from AttachWait.SRC to Attached.SRC		N/A
	DRP #1 in AttachWait.SRC continues to see CC pull down of DRP #2 for tCCDebounce, enters Attached.SRC and turns on VBUS and VCONN		N/A
	5. DRP #2 transitions from AttachWait.SNK to Attached.SNK.		N/A
	DRP #2 after having been in AttachWait.SNK for tCCDebounce and having detected VBUS, enters Attached.SNK		N/A
	6. While the DRPs are in their respective attached states:		N/A
	DRP #1 (as Source) adjusts Rp as needed to limit the current DRP #2 (as Sink) may draw		N/A
	DRP #2 (as Sink) detects and monitors vRd for available current on VBUS		N/A
	DRP #1 (as Source) monitors CC for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)		N/A
	DRP #2 (as Sink) monitors VBUS for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)		N/A
	Figure 4-27 illustrates the functional model for a DRP connected to a DRP in the second case described.		N/A
	CASE 2: The following describes the behavior when a DRP is connected to another DRP. In this flow, the DRP #2 chooses to drive the random result to the opposite result using the Try.SRC mechanism.		N/A
	1. Both DRPs in the unattached state		N/A
	DRP #1 and DRP #2 alternate between Unattached.SRC and Unattached.SNK		N/A
	2. DRP #1 transitions from Unattached.SRC to AttachWait.SRC		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	DRP #1 in Unattached.SRC detects a CC pull down of DRP #2 in Unattached.SNK and enters AttachWait.SRC		N/A
	3. DRP #2 transitions from Unattached.SNK to AttachWait.SNK		N/A
	DRP #2 in Unattached.SNK detects pull up on a CC and enters AttachWait.SNK		N/A
	4. DRP #1 transitions from AttachWait.SRC to Attached.SRC		N/A
	DRP #1 in AttachWait.SRC continues to see CC pull down of DRP #2 for tCCDebounce, enters Attached.SRC and turns on VBUS and VCONN		N/A
	5. DRP #2 transitions from AttachWait.SNK to Try.SRC.		N/A
	DRP #2 in AttachWait.SNK has been in this state for tCCDebounce and detects VBUS but strongly prefers the Source role, so transitions to Try.SRC		N/A
	DRP #2 in Try.SRC asserts a pull-up on CC and waits		N/A
	6. DRP #1 transitions from Attached.SRC to Unattached.SNK to AttachWait.SNK		N/A
	DRP #1 in Attached.SRC no longer detects DRP #2's pull-down on CC and transitions to Unattached.SNK.		N/A
	DRP #1 in Unattached.SNK turns off VBUS and VCONN and applies a pull-down on CC		N/A
	DRP #1 in Unattached.SNK detects pull up on a CC and enters AttachWait.SNK		N/A
	7. DRP #2 transitions from Try.SRC to Attached.SRC		N/A
	DRP #2 in Try.SRC detects the DRP #1 in Unattached.SNK's pull-down on CC and enters Attached.SRC		N/A
	DRP #2 in Attached.SRC turns on VBUS and VCONN		N/A
	8. DRP #1 transitions from AttachWait.SNK to Attached.SNK		N/A
	DRP #1 in AttachWait.SNK after tCCDebounce and detecting VBUS, enters Attached.SNK		N/A
	9. While the DRPs are in their respective attached states:		N/A
	DRP #2 (as Source) adjusts Rp as needed to limit the current DRP #1 (as Sink) may draw		N/A
	DRP #1 (as Sink) detects and monitors vRd for available current on VBUS		N/A
	DRP #2 (as Source) monitors CC for detach and when detected, enters Unattached.SNK		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	(and resumes toggling between Unattached.SNK and Unattached.SRC)		
	DRP #1 (as Sink) monitors VBUS for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)		N/A
	CASE 3: The following describes the behavior when a DRP is connected to another DRP. In this flow, the DRP #1 chooses to drive the random result to the opposite result using the Try.SNK mechanism.		N/A
	1. Both DRPs in the unattached state		N/A
	DRP #1 and DRP #2 alternate between Unattached.SRC and Unattached.SNK		N/A
	2. DRP #1 transitions from Unattached.SRC to AttachWait.SRC		N/A
	DRP #1 in Unattached.SRC detects a CC pull down of DRP #2 in Unattached.SNK and enters AttachWait.SRC		N/A
	3. DRP #2 transitions from Unattached.SNK to AttachWait.SNK		N/A
	DRP #2 in Unattached.SNK detects pull up on a CC and enters AttachWait.SNK		N/A
	4. DRP #1 transitions from AttachWait.SRC to Try.SNK		N/A
	DRP #1 in AttachWait.SRC has been in this state for tCCDebounce and detects DRP #2's pull-down on CC but strongly prefers the Sink role, so transitions to Try.SNK		N/A
	DRP #1 in Try.SNK asserts a pull down on CC and waits		N/A
	5. DRP #2 transitions from AttachWait.SNK to Unattached.SRC to AttachWait.SRC.		N/A
	DRP #2 in AttachWait.SNK no longer detects DRP #1's pull up on CC and transitions to Unattached.SRC		N/A
	DRP #2 in Unattached.SRC applies a pull up on CC		N/A
	DRP #2 in Unattached.SRC detects a pull down on a CC pin and enters AttachWait.SRC		N/A
	DRP #1 detects DRP #2's pull up on CC and remains in Try.SNK		N/A
	6. DRP #2 transitions from AttachWait.SRC to Attached.SRC		N/A
	DRP #2 in AttachWait.SRC times out (tCCDebounce) and transitions to Attached.SRC		N/A
	DRP #2 in Attached.SRC turns on VBUS and VCONN		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	7. DRP #1 transitions from Try.SNK to Attached.SNK		N/A
	DRP #1 in Try.SNK after detecting VBUS, enters Attached.SNK		N/A
	8. While the DRPs are in their respective attached states:		N/A
	DRP #2 (as Source) adjusts Rp as needed to limit the current DRP #1 (as Sink) may draw		N/A
	DRP #1 (as Sink) detects and monitors vRd for available current on VBUS		N/A
	DRP #2 (as Source) monitors CC for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)		N/A
	DRP #1 (as Sink) monitors VBUS for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)		N/A
4.5.3.1.5	Source to Source Behavior		N/A
	Figure 4-28 illustrates the functional model for a Source connected to a Source. The single CC wire that is in a standard cable is only shown in one of the four possible connection routes, CC1 to CC1. Port numbers have been arbitrarily assigned in the diagram to assist the reader to understand the process description.		N/A
	The following describes the behavior when a Source is connected to another Source.		N/A
	1. Both Sources in the unattached state		N/A
	Source #1 fails to detect a Sink's pull-down on CC and remains in Unattached.SRC		N/A
	Source #2 fails to detect a Sink's pull-down on CC and remains in Unattached.SRC		N/A
4.5.3.1.6	Sink to Sink Behavior		N/A
	Figure 4-29 illustrates the functional model for a Sink connected to a Sink. The single CC wire that is in a standard cable is only shown in one of the four possible connection routes, CC1 to CC1. Port numbers have been arbitrarily assigned in the diagram to assist the reader to understand the process description.		N/A
	The following describes the behavior when a Sink is connected to another Sink.		N/A
	1. Both Sinks in the unattached state		N/A
	Sink #1 fails to detect pull up on CC or VBUS supplied by a Source and remains in Unattached.SNK		N/A
	Sink #2 fails to detect pull up on CC or VBUS supplied by a Source and remains in Unattached.SNK		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
4.5.3.1.7	DRP to VCONN-Powered USB Device (VPD) Behavior		N/A
	Figure 4-30 illustrates the functional model for a DRP connected to a VCONN-Powered USB Device that does not feature charge-through functionality.		N/A
	The following describes the behavior when a DRP that supports VPDs is connected to a VPD.		N/A
	1. DRP and VPD in the unattached state		N/A
	DRP alternates between Unattached.SRC and Unattached.SNK		N/A
	2. DRP transitions from Unattached.SRC to Attached.SRC through AttachWait.SRC		N/A
	DRP in Unattached.SRC detects the CC pull-down of VPD which is in Unattached.SNK and DRP enters AttachWait.SRC		N/A
	DRP in AttachWait.SRC detects that pull-down on CC persists for tCCDebounce. It then enters Attached.SRC and turns on VBUS and VCONN		N/A
	3. VPD transitions from Unattached.SNK to Attached.SNK through AttachWait.SNK		N/A
	VPD detects VCONN and enters Attached.SNK		N/A
	4. While DRP and VPD are in their respective attached states, DRP discovers the VPD and removes VBUS		N/A
	DRP (as Source) queries the cable identity via USB PD on SOP'.		N/A
	VPD responds on SOP', advertising that it is a VCONN-Powered USB Device that does not support charge-through		N/A
	DRP (as Source) removes VBUS		N/A
	DRP (as Source) maintains its Rp		N/A
	5. DRP and VPD for detach		N/A
	DRP (as Source) monitors CC for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)		N/A
	VPD monitors VCONN for detach and when detected, enters Unattached.SNK		N/A
4.5.3.1.8	DRP to Charge-Through VCONN-Powered USB Device (CTVPD) Behavior		N/A
	Figure 4-31 illustrates the functional model for a DRP connected to a Charge-Through VCONNPowered USB Device, with a Source attached to the Charge-Through port on the VCONNPowered USB Device.		N/A
	CASE 1: The following describes the behavior when a DRP is connected to a Charge-Through		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	VCONN-Powered USB Device (abbreviated CTVPD), with no Power Source attached to the Charge-Through port on the CTVPD.		
	1. DRP and CTVPD are both in the unattached state		N/A
	a. DRP alternates between Unattached.SRC and Unattached.SNK		N/A
	b. CTVPD has applied Rd on its Charge-Through port's CC1 and CC2 pins and Rd on the Host-side port's CC pin		N/A
	2. DRP transitions from Unattached.SRC to Attached.SRC through AttachWait.SRC		N/A
	a. DRP in Unattached.SRC detects a CC pull down of CTVPD which is in Unattached.SNK and DRP enters AttachWait.SRC		N/A
	b. DRP in AttachWait.SRC detects that pull down on CC persists for tCCDebounce, enters Attached.SRC and turns on VBUS and VCONN		N/A
	3. CTVPD transitions from Unattached.SNK to Attached.SNK through AttachWait.SNK		N/A
	a. CTVPD detects the host-side CC pull-up of the DRP and CTVPD enters AttachWait.SNK		N/A
	b. CTVPD in AttachWait.SNK detects that pull up on the Host-side port's CC persists for tCCDebounce, VCONN present and enters Attached.SNK		N/A
	c. CTVPD present a high-impedance to ground (above zOPEN) on its Charge-Through port's CC1 and CC2 pins		N/A
	4. While DRP and CTVPD are in their respective attached states, DRP discovers the CTVPD and transitions to CTUnattached.SNK		N/A
	a. DRP (as Source) queries the device identity via USB PD (Device Identity Command) on SOP'		N/A
	b. CTVPD responds on SOP', advertising that it is a Charge-Through VCONN Powered USB Device		N/A
	c. DRP (as Source) removes VBUS		N/A
	d. DRP (as Source) changes its Rp to a Rd		N/A
	e. DRP (as Sink) continues to provide VCONN and enters CTUnattached.SNK		N/A
	5. CTVPD transitions to CTUnattached.VPD		N/A
	a. CTVPD detects VBUS removal, VCONN presence, the low Host-side CC pin and enters CTUnattached.VPD		N/A
	b. CTVPD changes its host-side Rd to a Rp advertising 3.0 A		N/A
	c. CTVPD isolates itself from VBUS		N/A
	d. CTVPD apply Rd on its Charge-Through		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
	port's CC1 and CC2 pins		
	6. While the CTVPD in CTUnattached.VPD state and the DRP in CTUnattached.SNK state:		N/A
	a. CTVPD monitors Charge-Through CC pins for a source or sink; when a Power Source attach is detected, enters CTAttachWait.VPD; when a sink is detected, enters CTAttachWait.Unsupported		N/A
	b. CTVPD monitors VCONN for Host detach and when detected, enters Unattached.SNK		N/A
	c. DRP monitors VBUS and CC for CTVPD detach for tVPDDetach and when detected, enters Unattached.SNK		N/A
	d. DRP monitors VBUS for Power Source attach and when detected, enters CTAttached.SNK		N/A
	CASE 2: The following describes the behavior when a Power Source is connected to a Charge-Through VCONN-Powered USB Device (abbreviated CTVPD), with a Host already attached to the Host-side port on the CTVPD.		N/A
	1. DRP is in CTUnattached.SNK state, CTVPD in CTUnattached.VPD, and Power Source in the unattached state		N/A
	a. CTVPD has applied Rd on the Charge-Through port's CC1 and CC2 pins and Rp termination advertising 3.0 A on the Host-side port's CC pin		N/A
	2. Power Source transitions from Unattached.SRC to Attached.SRC through AttachWait.SRC		N/A
	a. Power Source detects the CC pull-down of the CTVPD and enters AttachWait.SRC		N/A
	b. Power Source in AttachWait.SRC detects that pull down on CC persists for tCCDebounce, enters Attached.SRC and turns on VBUS		N/A
	3. CTVPD transitions from CTUnattached.VPD through CTAttachWait.VPD to CTAttached.VPD		N/A
	a. CTVPD detects the Source's Rp on one of its Charge-Through CC pins, and transitions to CTAttachWait.VPD		N/A
	b. CTVPD finishes any active USB PD communication on SOP' and ceases to respond to SOP' queries		N/A
	c. CTVPD in CTAttachWait.VPD detects that the pull up on Charge-Through CC pin persists for tCCDebounce, detects VBUS and enters CTAttached.VPD		N/A
	d. CTVPD connects the active Charge-Through CC pin to the Host-side port's CC pin		N/A
	e. CTVPD disables its Rp termination advertising 3.0 A on the Host-side port's CC pin		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	f. CTVPD disables its Rd on the Charge-Through CC pins		N/A
	g. CTVPD connects VBUS from the Charge-Through side to the Host side		N/A
	4. DRP (as Sink) transitions to CTAttached.SNK		N/A
	a. DRP (as Sink) detects VBUS, monitors vRd for available current and enter CTAttached.SNK		N/A
	5. While the devices are all in their respective attached states:		N/A
	a. CTVPD monitors VCONN for DRP detach and when detected, enters CTDisabled.VPD		N/A
	b. CTVPD monitors VBUS and CC for Power Source detach and when detected, enters CTUnattached.VPD within tVPDCTDD		N/A
	c. DRP (as Sink) monitors VBUS for Charge-Through Power Source detach and when detected, enters CTUnattached.SNK		N/A
	d. DRP (as Sink) monitors VBUS and CC for CTVPD detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)		N/A
	e. Power Source monitors CC for CTVPD detach and when detected, enters Unattached.SRC		N/A
	CASE 3: The following describes the behavior when a Power Source is connected to a Charge-Through VCONN-Powered USB Device (abbreviated CTVPD), with no Host attached to the Host-side port on the CTVPD.		N/A
	1. CTVPD and Power Source are both in the unattached state		N/A
	a. CTVPD has applied Rd on the Charge-Through port's CC1 and CC2 pins and Rd on the Host-side port's CC pin		N/A
	2. Power Source transitions from Unattached.SRC to Attached.SRC through AttachWait.SRC		N/A
	a. Power Source detects the CC pull-down of the CTVPD and enters AttachWait.SRC		N/A
	b. Power Source in AttachWait.SRC detects that pull down on CC persists for tCCDebounce, enters Attached.SRC and turns on VBUS		N/A
	3. CTVPD alternates between Unattached.SNK and Unattached.SRC		N/A
	a. CTVPD detects the Source's Rp on one of its Charge-Through CC pins, detects VBUS for tCCDebounce and starts alternating between Unattached.SRC and Unattached.SNK		N/A
	4. While the CTVPD alternates between		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	Unattached.SRC and Unattached.SNK state and the Power Source in Attached.SRC state:		
	a. CTVPD monitors the Host-side port's CC pin for device attach and when detected, enters AttachWait.SRC		N/A
	b. CTVPD monitors VBUS for Power Source detach and when detected, enters Unattached.SNK		N/A
	c. Power Source monitors CC for CTVPD detach and when detected, enters Unattached.SRC		N/A
	CASE 4: The following describes the behavior when a DRP is connected to a Charge-Through VCONN-Powered USB Device (abbreviated CTVPD), with a Power Source already attached to the Charge-Through side on the CTVPD.		N/A
	1. DRP and CTVPD are in unattached state and Power Source in Attached.SRC state		N/A
	a. DRP alternates between Unattached.SRC and Unattached.SNK		N/A
	b. CTVPD alternates between Unattached.SRC and Unattached.SNK		N/A
	c. CTVPD has applied Rd on its Charge-Through port's CC1 and CC2 pins		N/A
	d. Power Source has applied VBUS		N/A
	2. DRP transitions from Unattached.SNK to AttachWait.SNK		N/A
	a. DRP in Unattached.SNK detects the CC pull-up of CTVPD which is in Unattached.SRC and DRP enters AttachWait.SNK		N/A
	3. CTVPD transitions from Unattached.SRC to Try.SNK through AttachWait.SRC		N/A
	a. CTVPD in Unattached.SRC detects the CC pull-down of DRP which is in Unattached.SNK and CTVPD enters AttachWait.SRC		N/A
	b. CTVPD in AttachWait.SRC detects that pull down on CC persists for tCCDebounce and enters Try.SNK		N/A
	c. CTVPD disables Rp termination advertising Default USB Power on the Hostside port's CC pin		N/A
	d. CTVPD enables Rd on the Host-side port's CC pin		N/A
	4. DRP transitions from AttachWait.SNK to Attached.SRC through Unattached.SRC and AttachWait.SRC		N/A
	a. DRP in AttachWait.SNK detects the CC pull-up removal of CTVPD which is in Try.SNK and DRP enters Unattached.SRC		N/A
	b. DRP in Unattached.SRC detects the CC pull-down of CTVPD which is in Try.SNK and DRP		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	enters AttachWait.SRC		
	c. DRP in AttachWait.SRC detects that pull down on CC persists for tCCDebounce. It then enters Attached.SRC and enable VBUS and VCONN		N/A
	5. CTVPD transitions from Try.SNK to Attached.SNK		N/A
	a. CTVPD detects the CC pull-up of the DRP persists for tTryCCDebounce		N/A
	b. CTVPD detects VBUS on the Host-side port and enters Attached.SNK		N/A
	6. While DRP and CTVPD are in their respective attached states, DRP discovers the Charge-Through CTVPD and transitions to CTUnattached.SNK		N/A
	a. DRP (as Source) queries the device identity via USB PD (Discover Identity Command) on SOP'		N/A
	b. CTVPD responds on SOP', advertising that it is a Charge-Through VCONNPowered USB Device		N/A
	c. DRP (as Source) removes VBUS		N/A
	d. DRP (as Source) changes its Rp into an Rd		N/A
	e. DRP (as Sink) continues to provide VCONN and enters CTUnattached.SNK		N/A
	7. CTVPD transitions to CTUnattached.VPD		N/A
	a. CTVPD detects VBUS removal, VCONN presence, and the low CC pin on its host port and enters CTUnattached.VPD		N/A
	b. CTVPD changes its host-side Rd into an Rp termination advertising 3.0 A		N/A
	c. CTVPD isolates itself from VBUS		N/A
	8. CTVPD transitions from CTUnattached.VPD through CTAttachWait.VPD to CTAttached.VPD		N/A
	a. CTVPD detects the Source's Rp on one of its Charge-Through CC pins, and transitions to CTAttachWait.VPD		N/A
	b. CTVPD in CTAttachWait.VPD detects that the pull up on Charge-Through CC pin persists for tCCDebounce, detects VBUS and enters CTAttached.VPD		N/A
	c. CTVPD finishes any active USB PD communication on SOP' and ceases to respond to SOP' queries		N/A
	d. CTVPD connects the active Charge-Through CC pin to the Host-side port's CC pin		N/A
	e. CTVPD disables its Rp termination advertising 3.0 A on the Host-side port's CC pin		N/A
	f. CTVPD disables its Rd on the Charge-Through CC pins		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	g. CTVPD connects VBUS from the Charge-Through side to the Host side		N/A
	9. DRP (as Sink) transitions to CTAttached.SNK		N/A
	a. DRP (as Sink) detects VBUS and monitors vRd for available current and enter CTAttached.SNK		N/A
	10. While the devices are all in their respective attached states:		N/A
	a. CTVPD monitors VCONN for DRP detach and when detected, enters CTDisabled.VPD		N/A
	b. CTVPD monitors VBUS and CC for Power Source detach and when detected, enters CTUnattached.VPD within tVPDCTDD		N/A
	c. DRP (as Sink) monitors VBUS for Charge-Through Power Source detach and when detected, enters CTUnattached.SNK		N/A
	d. DRP (as Sink) monitors VBUS and CC for CTVPD detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)		N/A
	e. Power Source monitors CC for CTVPD detach and when detected, enters Unattached.SRC		N/A
	CASE 5: The following describes the behavior when a Power Source is connected to a Charge-Through VCONN-Powered USB Device (abbreviated CTVPD), with a DRP (with dead battery) attached to the Host-side port on the CTVPD.		N/A
	1. DRP, CTVPD and Power Source are all in the unattached state		N/A
	a. DRP apply dead battery Rd		N/A
	b. CTVPD apply Rd on the Charge-Through port's CC1 and CC2 pins and Rd on the Host-side port's CC pin		N/A
	2. Power Source transitions from Unattached.SRC to Attached.SRC through AttachWait.SRC		N/A
	a. Power Source detects the CC pull-down of the CTVPD and enters AttachWait.SRC		N/A
	b. Power Source in AttachWait.SRC detects that pull down on CC persists for tCCDebounce, enters Attached.SRC and turns on VBUS		N/A
	3. CTVPD alternates between Unattached.SNK and Unattached.SRC		N/A
	a. CTVPD detects the Source's Rp on one of its Charge-Through CC pins, detects VBUS for tCCDebounce and starts alternating between Unattached.SRC and Unattached.SNK		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
	4. CTVPD transitions from Unattached.SRC to Try.SNK through AttachWait.SRC		N/A
	a. CTVPD in Unattached.SRC detects the CC pull-down of DRP which is in Unattached.SNK and CTVPD enters AttachWait.SRC		N/A
	b. CTVPD in AttachWait.SRC detects that pull down on CC persists for tCCDebounce and enters Try.SNK		N/A
	d. CTVPD enables Rd on the Host-side port's CC pin		N/A
	5. DRP in dead battery condition remains in Unattached.SNK		N/A
	6. CTVPD transitions from Try.SNK to Attached.SRC through TryWait.SRC		N/A
	a. CTVPD didn't detect the CC pull-up of the DRP for tTryCCDebounce after tDRPTry and enters TryWait.SRC		N/A
	b. CTVPD disables Rp on the Host-side port's CC pin		N/A
	c. CTVPD enables Rp termination advertising Default USB Power on the Hostside port's CC pin		N/A
	d. CTVPD detects the CC pull-down of the DRP for tTryCCDebounce and enters Attached.SRC		N/A
	e. CTVPD connects VBUS from the Charge-Through side to the Host side		N/A
	7. DRP transitions from Unattached.SNK to Attached.SNK through AttachWait.SNK		N/A
	a. DRP in Unattached.SNK detects the CC pull-up of CTVPD which is in Attached.SRC and DRP enters AttachWait.SNK		N/A
	b. DRP in AttachWait.SNK detects that pull up on CC persists for tCCDebounce, VBUS present and enters Attached.SNK		N/A
	8. While the devices are all in their respective attached states:		N/A
	a. CTVPD monitors the Host-side port's CC pin for device attach and when detected, enters Unattached.SNK		N/A
	b. CTVPD monitors VBUS for Power Source detach and when detected, enters Unattached.SNK		N/A
	c. Power Source monitors CC for CTVPD detach and when detected, enters Unattached.SRC		N/A
	d. DRP monitors VBUS for CTVPD detach and when detected, enters Unattached.SNK		N/A
	e. Additionally, the DRP may query the identity of the cable via USB PD on SOP' when it has sufficient battery power and when a Charge-Through VPD is identified enters TryWait.SRC		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
	if implemented, or enters Unattached.SRC if TryWait.SRC is not supported		
	CASE 6: The following describes the behavior when a DRP is connected to a Charge-Through VCONN-Powered USB Device (abbreviated CTVPD) and a Sink is attached to the Charge-Through port on the CTVPD.		N/A
	1. DRP, CTVPD and Sink are all in the unattached state		N/A
	a. DRP alternates between Unattached.SRC and Unattached.SNK		N/A
	b. CTVPD has applied Rd on its Charge-Through port's CC1 and CC2 pins and Rd on the Host-side port's CC pin		N/A
	2. DRP transitions from Unattached.SRC to Attached.SRC through AttachWait.SRC		N/A
	a. DRP in Unattached.SRC detects the CC pull-down of CTVPD which is in Unattached.SNK and DRP enters AttachWait.SRC		N/A
	b. DRP in AttachWait.SRC detects that pull down on CC persists for tCCDebounce. It then enters Attached.SRC and enable VBUS and VCONN		N/A
	3. CTVPD transitions from Unattached.SNK to Attached.SNK through AttachWait.SNK		N/A
	a. CTVPD detects the host-side CC pull-up of the DRP and CTVPD enters AttachWait.SNK		N/A
	b. CTVPD in AttachWait.SNK detects that pull up on the Host-side port's CC persists for tCCDebounce, VCONN present and enters Attached.SNK		N/A
	c. CTVPD present a high-impedance to ground (above zOPEN) on its Charge-Through port's CC1 and CC2 pins		N/A
	4. While DRP and CTVPD are in their respective attached states, DRP discovers the Charge-Through CTVPD and transitions to CTUnattached.SNK		N/A
	a. DRP (as Source) queries the device identity via USB PD (Discover Identity Command) on SOP'		N/A
	b. CTVPD responds on SOP', advertising that it is a Charge-Through VCONNPowered USB Device		N/A
	c. DRP (as Source) removes VBUS		N/A
	d. DRP (as Source) changes its Rp into an Rd		N/A
	e. DRP (as Sink) continues to provide VCONN and enters CTUnattached.SNK		N/A
	5. CTVPD transitions to CTUnattached.VPD		N/A
	a. CTVPD detects VBUS removal, VCONN presence, and the low CC pin on its host port		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	and enters CTUnattached.VPD		
	b. CTVPD changes its host-side Rd into an Rp termination advertising 3.0 A		N/A
	c. CTVPD isolates itself from VBUS		N/A
	d. CTVPD apply Rd on its Charge-Through port's CC1 and CC2 pins		N/A
	6. CTVPD alternates between CTUnattached.VPD and CTUnattached.Unsupported		N/A
	a. CTVPD detects SRC.Open on its Charge-Through CC pins and starts alternating between CTUnattached.VPD and CTUnattached.Unsupported		N/A
	7. CTVPD transitions from CTUnattached.Unsupported to CTTry.SNK through CTAttachWait.Unsupported		N/A
	a. CTVPD in CTUnattached.Unsupported detects the CC pull-down of the Sink which is in Unattached.SNK and CTVPD enters CTAttachWait.Unsupported		N/A
	b. CTVPD in CTAttachWait.Unsupported detects that pull down on CC persists for tCCDebounce and enters CTTry.SNK		N/A
	c. CTVPD disables Rp termination advertising Default USB Power on the Charge-Through port's CC pins		N/A
	d. CTVPD enables Rd on the Charge-Through port's CC pins		N/A
	8. CTVPD transitions from CTTry.SNK to CTAttached.Unsupported		N/A
	a. CTVPD didn't detect the CC pull-up of the potential Source for tDRPTryWait after tDRPTry and enters CTAttached.Unsupported		N/A
	9. While the CTVPD in CTAttached.Unsupported state, the DRP in CTUnattached.SNK state and the Sink in Unattached.SNK state:		N/A
	a. CTVPD disables the Rd termination on the Charge-Through port's CC pins and applies Rp termination advertising Default USB Power		N/A
	b. CTVPD exposes a USB Billboard Device Class to the DRP indicating that it is connected to an unsupported device on its Charge Through port		N/A
	c. CTVPD monitors Charge-Through CC pins for Sink detach and when detected, enters CTUnattached.VPD		N/A
	d. CTVPD monitors VCONN for Host detach and when detected, enters Unattached.SNK		N/A
	e. DRP monitors CC for CTVPD detach for tVPDDetach and when detected, enters Unattached.SNK		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	f. DRP monitors VBUS for CTVPD Charge-Through source attach and, when detected, enters CTAttached.SNK		N/A
4.5.3.2	USB Type-C port to Legacy Port Interoperability Behaviors		N/A
	The following sub-sections describe port-to-port interoperability behaviors for the various combinations of USB Type-C Source, Sink and DRPs and legacy USB ports.		N/A
4.5.3.2.1	Source to Legacy Device Port Behavior		N/A
	Figure 4-32 illustrates the functional model for a Source connected to a legacy device port. This model is based on having an adapter present as a Sink to the Source. This adapter has a USB Type-C plug on one end plugged into the Source and either a USB Standard-B plug, USB Micro-B plug, USB Mini-B plug, or a USB Standard-A receptacle on the other end.		N/A
	The following describes the behavior when a Source is connected to a legacy device adapter that has an Rd to ground so as to mimic the behavior of a Sink.		N/A
	1. Source in the unattached state		N/A
	2. Source transitions from Unattached.SRC to Attached.SRC through AttachWait.SRC		N/A
	Source detects the Sink's pull-down on CC and enters AttachWait.SRC. After tCCDebounce, it enters Attached.SRC.		N/A
	Source turns on VBUS and VCONN		N/A
	3. While the Source is in the attached state:		N/A
	Source monitors CC for detach and when detected, enters Unattached.SRC		N/A
4.5.3.2.2	Legacy Host Port to Sink Behavior		N/A
	Figure 4-33 illustrates the functional model for a legacy host port connected to a Sink. This model is based on having an adapter that presents itself as a Source to the Sink, this adapter is either a USB Standard-A legacy plug or a USB Micro-B legacy receptacle on one end and the USB Type-C plug on the other end plugged into a Sink.		N/A
	The following describes the behavior when a legacy host adapter that has an Rp to VBUS so as to mimic the behavior of a Source that is connected to a Sink. The value of Rp shall indicate an advertisement of Default USB Power (See Table 4-24), even though the cable itself can carry 3 A. This is because the cable has no knowledge of the capabilities of the power source, and any higher current is negotiated via USB BC 1.2.		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	1. Sink in the unattached state		N/A
	2. Sink transitions from Unattached.SNK to Attached.SNK through AttachWait.SNK if needed.		N/A
	While in Unattached.SNK, if device is not USB 2.0 only, supports accessories or requires more than default power, it enters AttachWait.SNK when it detects a pull up on CC and ignores VBUS. Otherwise, it may enter Attached.SNK directly when VBUS is detected.		N/A
	Sink detects VBUS and enters Attached.SNK		N/A
	3. While the Sink is in the attached state:		N/A
	Sink monitors VBUS for detach and when detected, enters Unattached.SNK		N/A
4.5.3.2.3	DRP to Legacy Device Port Behavior		N/A
	Figure 4-34 illustrates the functional model for a DRP connected to a legacy device port. This model is based on having an adapter present as a Sink (Device) to the DRP. This adapter has a USB Type-C plug on one end plugged into a DRP and either a USB Standard-B plug, USB Micro-B plug, USB Mini-B plug, or a USB Standard-A receptacle on the other end.		N/A
	The following describes the behavior when a DRP is connected to a legacy device adapter that has an Rd to ground so as to mimic the behavior of a Sink.		N/A
	1. DRP in the unattached state		N/A
	DRP alternates between Unattached.SRC and Unattached.SNK		N/A
	2. DRP transitions from Unattached.SRC to Attached.SRC		N/A
	DRP in Unattached.SRC detects the adapter's pull-down on CC and enters AttachWait.SRC		N/A
	DRP in AttachWait.SRC times out (tCCDebounce) and transitions to Attached.SRC		N/A
	DRP in Attached.SRC turns on VBUS and VCONN		N/A
	DRP in AttachWait.SRC may support Try.SNK and if so, may transition through Try.SNK and TryWait.SRC prior to entering Attached.SRC		N/A
	3. While the DRP is in the attached state:		N/A
	DRP monitors CC for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)		N/A
4.5.3.2.4	Legacy Host Port to DRP Behavior		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	Figure 4-35 illustrates the functional model for a legacy host port connected to a DRP operating as a Sink. This model is based on having an adapter that presents itself as a Source (Host) to the DRP operating as a Sink, this adapter is either a USB Standard-A legacy plug or a USB Micro-B legacy receptacle on one end and the USB Type-C plug on the other end plugged into a DRP.		N/A
	The following describes the behavior when a legacy host adapter that has an Rp to VBUS so as to mimic the behavior of a Source is connected to a DRP. The value of Rp shall indicate an advertisement of Default USB Power (See Table 4-24), even though the cable itself can carry 3 A. This is because the cable has no knowledge of the capabilities of the power source, and any higher current is negotiated via USB BC 1.2.		N/A
	1. DRP in the unattached state		N/A
	DRP alternates between Unattached.SRC and Unattached.SNK		N/A
	2. DRP transitions from Unattached.SNK to AttachWait.SNK to Attached.SNK		N/A
	DRP in Unattached.SNK detects pull up on CC and enters AttachWait.SNK.		N/A
	DRP in AttachWait.SNK detects VBUS and enters Attached.SNK		N/A
	DRP in AttachWait.SNK may support Try.SRC and if so, may transition through Try.SRC and TryWait.SNK prior to entering Attached.SNK		N/A
	3. While the DRP is in the attached state:		N/A
	DRP monitors VBUS for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)		N/A
<b>4.6</b>	<b>Power</b>		N/A
	Power delivery over the USB Type-C connector takes advantage of the existing USB methods as defined by: the USB 2.0 and USB 3.2 specifications, the USB BC 1.2 specification and the USB Power Delivery specification. Power for USB4 operation requires a USB PD explicit contract as defined in Section 5.3 and the USB Power Delivery specification. Prior to entering a USB PD explicit contract, a USB4 port operates as a USB 3.2 port regarding power.		N/A
	The USB Type-C Current mechanism allows the Source to offer more current than defined by the USB BC 1.2 specification. A USB power source shall not provide more than 20 V		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
	nominal on VBUS. USB PD power sources that deliver power over a USB Type-C connector shall follow the power rules as defined in Section 10 of the USB Power Delivery specification.		
	All USB Type-C-based devices shall support USB Type-C Current and may support other USB-defined methods for power. The following order of precedence of power negotiation shall be followed: USB BC 1.2 supersedes the USB 2.0 and USB 3.2 specifications, USB Type-C Current at 1.5 A and 3.0 A supersedes USB BC 1.2, and USB Power Delivery supersedes USB Type-C Current. Table 4-17 summarizes this order of precedence of power source usage.		N/A
	For example, once the PD mode (e.g. a power contract has been negotiated) has been entered, the device shall abide by that power contract ignoring any other previously made or offered by the USB Type-C Current, USB BC 1.2 or USB 2.0 and USB 3.2 specifications. When the PD mode is exited, the device shall fallback in order to the USB Type-C Current, USB BC 1.2 or USB 2.0 and USB 3.2 specification power levels.		N/A
	All USB Type-C ports shall tolerate being connected to USB power source supplying default USB power, e.g. a host being connected to a legacy USB charger that always supplies VBUS.		N/A
<b>4.6.1</b>	<b>Power Requirements during USB Suspend</b>		N/A
	USB Type-C implementations with USB Type-C Current, USB PD and VCONN, along with active cables, requires the need to expand the traditional USB suspend definition.		N/A
4.6.1.1	VBUS Requirements during USB Suspend		N/A
	The USB 2.0 and USB 3.2 specifications define the amount of current a Sink is allowed to consume during suspend.		N/A
	USB suspend power rules shall apply when the USB Type-C Current is at the Default USB Power level or when USB PD is being used and the Suspend bit is set appropriately.		N/A
	When USB Type-C Current is set at 1.5 A or 3.0 A, the Sink is allowed to continue to draw current from VBUS during USB suspend. During USB suspend, the Sink's requirement to track and meet the USB Type-C Current advertisement remains in force (See Section 4.5.2.3).		N/A
	USB PD provides a method for the Source to communicate to the Sink whether or not the Sink has to follow the USB power rules for suspend.		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
4.6.1.2	VCONN Requirements during USB Suspend		N/A
	If the Source supplies VBUS power during USB suspend, it shall also supply VCONN and meet the requirements defined in Table 4-5.		N/A
	Electronically Marked Cables shall meet the requirements in Table 4-6 during USB suspend.		N/A
	VCONN powered accessories shall meet the requirements defined in Table 4-7 during USB suspend.		N/A
<b>4.6.2</b>	<b>VBUS Power Provided Over a USB Type-C Cable</b>		N/A
	The minimum requirement for VBUS power supplied over the USB Type-C cable assembly matches the existing requirement for VBUS supplied over existing legacy USB cable assemblies.		N/A
	USB Power Delivery in Standard Power Range (SPR) operation is intended to work over unmodified USB Type-C to USB Type-C cables, therefore any USB Type-C cable assembly that incorporates electrical components or electronics shall ensure that it tolerate, or be protected from, a VBUS voltage of 21 V.		N/A
	USB Power Delivery in Extended Power Range (EPR) operation requires EPR-compatible USB Type-C to USB Type-C cables. Any USB Type-C cable assembly that incorporates electrical components or electronics that may be powered by VBUS shall ensure that it can functionally tolerate, or be protected from, a VBUS voltage of up to 53.65 V (51 V + 5% + 100mV).		N/A
4.6.2.1	USB Type-C Current		N/A
	Default USB voltage and current are defined by the USB 2.0 and USB 3.2 specifications. All USB Type-C Current advertisements are at the USB VBUS voltage defined by these specifications.		N/A
	The USB Type-C Current feature provides the following extensions:		N/A
	Higher current than defined by the USB 2.0, the USB 3.2 or the BC 1.2 specifications		N/A
	Allows the power source to manage the current it provides		N/A
	The USB Type-C connector uses CC pins for configuration including an ability for a Source to advertise to its port partner (Sink) the amount of current it shall supply:		N/A
	Default is the as-configured for high-power operation current value as defined by the USB Specification (500 mA for USB 2.0 ports; 900		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	mA or 1,500 mA for USB 3.2 ports in single-lane or dual-lane operation, respectively)		
	1.5 A		N/A
	3.0 A		N/A
	When a Source is advertising USB Type-C Default current, the Sink behavior is defined as follows:		N/A
	It connects as a USB 2.0 or USB 3.2 device, after which the Sink shall follow the appropriate USB specification.		N/A
	It enters a USB PD contract, after which the Sink shall follow the USB PD specification to determine the current (e.g., Rp will no longer be Default as it is superseded by the USB PD contract).		N/A
	It detects a USB BC 1.2 charging port, after which the Sink shall follow the USB BC 1.2 specification.		N/A
	It attaches as a USB Type-C Power Sinking Device (PSD), after which the Sink may draw up to 500 mA and shall meet the inrush requirement for USB 2.0.		N/A
	A PSD shall fully support USB Type-C Current operation, should support USB PD and may support USB BC 1.2. A PSD may be a Sink or a DRP operating in Sink mode. A PSD shall not have a USB or USB Type-C Alternate Mode communications function.		N/A
	The relationship of USB Type-C Current and the equivalent USB PD Power (PDP) value is shown in Table 4-18.		N/A
	A Sink that takes advantage of the additional current offered (e.g., 1.5 A or 3.0 A) shall monitor the CC pins and shall adjust its current consumption within tSinkAdj to remain within the value advertised by the Source. While a USB PD contract is in place, a Sink is not required to monitor USB Type-C current advertisements and shall not respond to USB Type-C current advertisements.		N/A
	The Source shall supply VBUS to the Sink within tVBUSON. VBUS shall be in the specified voltage range at the advertised current.		N/A
	A Source (port supplying VBUS) shall protect itself from a Sink that draws current in excess of the port's USB Type-C Current advertisement.		N/A
	The Source adjusts Rp (or current source) to advertise which of the three current levels it supports. See Table 4-24 for the termination requirements for the Source to advertise currents.		N/A
	The value of Rp establishes a voltage (vRd) on CC that is used by the Sink to determine the		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	maximum current it may draw.		
	Table 4-35 defines the CC voltage range observed by the Sink that only support default USB current.		N/A
	If the Sink wants to consume more than the default USB current, it shall track vRd to determine the maximum current it may draw. See Table 4-36.		N/A
	Figure 4-36 and Figure 4-37 illustrate where the Sink monitors CC for vRd to detect if the host advertises more than the default USB current.		N/A
4.6.2.2	USB Battery Charging 1.2		N/A
	USB Battery Charging Specification, Revision 1.2 defines a method that uses the USB 2.0 D+ and D- pins to advertise VBUS can supply up to 1.5 A. Support for USB BC 1.2 charging is optional.		N/A
	A USB Type-C port that implements USB BC 1.2 that is capable of supplying at least 1.5 A shall advertise USB Type-C Current at the 1.5 A level within tVBUSON of entering the Attached.SRC state, otherwise the port shall advertise USB Type-C Current at the Default USB Power level. A USB Type-C port that implements USB BC 1.2 that also supports USB Type-C Current at 3.0 A may advertise USB Type-C Current at 3.0 A.		N/A
	If a Sink that supports USB BC 1.2 detection, detects Rp at the Default USB Power level and does not discover a USB BC 1.2-compliant Source, then it shall limit its maximum current consumption to the standard USB levels based on Table 4-17. This will ensure maximum current limits are not exceeded when connected to a Source which does not support USB BC 1.2.		N/A
	A Sink that supports USB BC 1.2 detection and has a maximum current draw greater than Default USB Type-C Current shall monitor vRd on the CC pins to detect the Source's Rp and shall implement Sink Power Sub-State transitions (Figure 4-19). If a Sink that supports USB BC 1.2 detection and has a maximum current draw greater than Default USB Type-C Current detects Rp at USB Type-C Current of 1.5 A or 3.0 A levels but does not detect a USB BC 1.2 source, it shall limit its maximum current consumption to the appropriate USB Type-C Current level advertised, and shall adjust its current consumption to remain within the value advertised by the Source on Sub-State transitions. For Sub-State transitions starting from a higher power level and ending at a lower power level, the Sink shall reduce power consumption within tSinkAdj. See Sections		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	4.5.2.3.2.2 and 4.5.2.3.3.2.		
	While in a Power Delivery Mode, a device acting as a Sink shall not initiate a USB BC 1.2 detection until the port pair is detached or there is an Error Recovery or Hard Reset.		N/A
4.6.2.3	Proprietary Power Source		N/A
	This section has been deprecated. Devices with USB Type-C connectors shall only employ signaling methods defined in USB specifications to negotiate power.		N/A
4.6.2.4	USB Power Delivery		N/A
	USB Power Delivery is a feature on the USB Type-C connector. When USB PD is implemented, USB PD Bi-phase Mark Coded (BMC) carried on the CC wire shall be used for USB PD communications between USB Type-C ports.		N/A
	At attach, VBUS shall be operationally stable prior to initiating USB PD communications.		N/A
	When not in an Explicit Contract, USB PD Sources that are, based on their PDP, capable of supplying:		N/A
	5 V at 3 A or greater shall advertise USB Type-C Current at the 3 A level		N/A
	5 V at 1.5A or greater but less than 3 A shall advertise USB Type-C Current at the 1.5 A level		N/A
	5 V at less than 1.5A shall advertise USB Type-C Current at the Default USB Power level		N/A
	within tVBUSON of entering the Attached.SRC state. For Multi-Port Shared Capacity Chargers, a USB PD Source capable of supplying 5 V at 3A or greater may initially offer USB Type-C Current at the 1.5 A level and subsequently increase the offer after attach (see Section 4.8.6.2). During USB Suspend a USB PD Source may set its Rp value to default to indicate that the Sink shall only draw USB suspend current as defined in Section 4.6.1.1.		N/A
	While a USB PD Explicit Contract is in place, a Source compliant with USB PD Revision 2 shall advertise a USB Type-C Current of either 1.5 A or 3.0 A. The USB PD Revision 2 Source upon entry into an Explicit Contract shall advertise an Rp value of 1.5 A or 3.0 A after it receives the GoodCRC in response to the first PS_RDY Message.		N/A
	While a USB PD Explicit Contract is in place, a Source compliant with USB PD Revision 3 shall set the Rp value according to the collision avoidance scheme defined in Section 5.7 of the USB PD Revision 3 specification. The USB PD Revision 3 Source upon entry into an Explicit Contract shall advertise an Rp value consistent with the USB PD Revision 3 collision avoidance		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	scheme.		
	Refer to Section 1.6 of the USB Power Delivery specification for a definition of an Explicit Contract.		N/A
4.6.2.5	Charge-Through VCONN-Powered USB Device (CTVPD) Current Limitations		N/A
	Since Charge-Through VCONN-Powered USB Devices implement charging by passively connecting the Source's CC and VBUS to the Host, the VCONN-Powered USB Device is effectively increasing the impedance on VBUS, GND, and CC between the Power Source and the Host, resulting in impedances that can exceed the maximum allowed for cables. To avoid communication issues and false disconnects from the increased GND and VBUS drops, the following shall occur:		N/A
	1. The Charge-Through VCONN-Powered USB Device shall report its worst-case GND and VBUS impedance (including the extra mated connector pair and FETs) in its USB PD Discover Identity Command response on SOP'.		N/A
	2. The Host that supports Charge-Through VCONN-Powered USB Device shall use this information, along with inferred information about the cable, to limit its maximum current in the case where the Power Source advertises a current greater than what the Charge-Through VCONN-Powered USB Device would allow.		N/A
	The Host has no way to query the cable, as its VCONN source is consumed by the VCONNPowered USB Device. Instead, the Host may assume the cable is 5 A for the purposes of calculating the Charge-Through current limit only if it receives a USB PD SourceCapability PDO of greater than 3 A (even if the Host ultimately does not Request that PDO, or if the host requests a current of 3 A or less).		N/A
	The Host shall further limit its maximum current beyond that advertised by the Power Source, based on the reported GND impedance and the inferred cable capability. GND impedance is reported in the VPD Discover Identity Command Response in 1-milliohm steps and is used in the following formulas:		N/A
	GND-limited current with a 3A cable inferred = $0.25 \text{ V} / (0.25 \text{ V} / 3 \text{ A} + \text{VPD\_GND\_DCR})$		N/A
	GND-limited current with a 5A cable inferred = $0.25 \text{ V} / (0.25 \text{ V} / 5 \text{ A} + \text{VPD\_GND\_DCR})$		N/A
	In addition, the increased VBUS impedance could result in a greater than 1 V VBUS drop as measured at the input to the Host. Based on the VBUS impedance reported in the VPD Discover Identity Command Response in 2-		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
	milliohm steps and the inferred cable capability, the Host shall either lower its VBUS detach threshold or further limit its maximum current based on the following formulas:		
	VBUS and GND-limited current with a 3A cable inferred = $0.75\text{ V} / (0.75\text{ V} / 3\text{ A} + \text{VPD\_VBUS\_DCR} + \text{VPD\_GND\_DCR})$		N/A
	VBUS and GND-limited current with a 5A cable inferred = $0.75\text{ V} / (0.75\text{ V} / 5\text{ A} + \text{VPD\_VBUS\_DCR} + \text{VPD\_GND\_DCR})$		N/A
4.6.2.6	USB Type-C Sink Requirements for High Voltage Operation		N/A
	This section sets electrical requirements for USB Type-C Sinks that support high-voltage operation. See Section 3.11 for EPR requirements for USB Type-C cables that support EPR.		N/A
	The Sink shall keep the voltage on its VBUS contact to within 12 volts of the voltage on the Source VBUS contact at the time of the cable plug withdrawal for a minimum of 250 $\mu\text{s}$ from the time the VBUS contacts separate (see Figure 3-1). Refer to Appendix H for more information related to high-voltage contact arcing and mitigation guidelines.		N/A
4.7	<b>USB Hubs</b>		P
	USB 2.0, USB 3.2, and USB4 hubs are defined by the USB 2.0, USB 3.2, and USB4 specifications, respectively. USB hubs implemented with one or more USB Type-C connectors shall comply with these specifications as relevant to a USB Type-C implementation. All the downstream facing USB Type-C ports on a USB hub should support the same functionality or shall be clearly marked as to the functionality supported.		P
	USB hubs shall have an upstream facing port (to connect to a host or hub higher in the USB tree) that may be a Sourcing Device (See Section 4.8.4). The hub shall clearly identify to the user its upstream facing port. This may be accomplished by physical isolation, labeling or a combination of both.		P
	USB hub's downstream facing ports shall not have Dual-Role-Data (DRD) capabilities. However, these ports may have Dual-Role-Power (DRP) capabilities.		P
	CC pins are used for port-to-port connections and shall be supported on all USB Type-C connections on the hub.		P
	For USB 2.0 and USB 3.2 hubs, downstream-facing ports shall not implement or pass-through Alternate or Accessory Modes and SBU pins shall not be connected (zSBU Termination) on		P



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	any USB hub port. For USB4 hubs, see Section 5.2.3.2 regarding support for Alternate Modes.		
	The USB hub's DFPs shall support power source requirements for a Source. See Section 4.8.1.		P
	Additional requirements for USB4 hubs are in Chapter 5.		P
<b>4.8</b>	<b>Power Sourcing and Charging</b>		P
	This section defines requirements and recommendations related to using USB Type-C ports for delivering power. Any USB Type-C port that offers more than Default Current and/or supports USB Power Delivery shall meet the requirements as if it is a charger.		P
	The following lists the most applicable subsections by USB Type-C ports on:		P
	Host systems: 4.8.1 and 4.8.5. Note: 4.8.6 is not intended for host systems.		P
	Devices that can supply power: 4.8.4.		N/A
	Hubs:		P
	Traditional hubs – Refer to USB 2.0/USB 3.2 base specifications and 4.8.1 as applicable if USB BC 1.2 is supported.		P
	Hubs that can supply power beyond the base specs – 4.8.1, 4.8.4, 4.8.5 and 4.8.6.		P
	Dedicated chargers:		P
	Single-port chargers – 4.8.1.		P
	Multi-port chargers – 4.8.1 and 4.8.6.		P
<b>4.8.1</b>	<b>DFP as a Power Source</b>		P
	Sources (e.g. battery chargers, hub downstream ports and hosts) may all be used for battery charging. When a charger is implemented with a USB Type-C receptacle or a USB Type-C captive cable, it shall follow all the applicable requirements.		P
	A Source shall expose its power capabilities using the USB Type-C Current method and it may additionally support other USB-standard methods (USB BC 1.2 or USBPD).		P
	A Source advertising its current capability using USB BC 1.2 shall meet the requirements in Section 4.6.2.2 regarding USB Type-C Current advertisement.		P
	A Source that has negotiated a USB-PD contract shall meet the requirements in Section 4.6.2.4 regarding USB Type-C Current advertisement.		P
	If a Source is capable of supplying a voltage greater than default VBUS, it shall fully conform to the USB-PD specification and shall negotiate		P

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Clause	Requirement + Test	Result - Remark	Verdict
	its power contracts using only USB-PD.		
	If a Source is capable of reversing source and sink power roles, it shall fully conform to the USB-PD specification and shall negotiate its power contracts using only USBPD.		P
	If a Source is capable of supplying a current greater than 3.0 A, it shall use the USBPD Discover Identity to determine the current carrying capacity of the cable.		P
4.8.1.1	USB-based Chargers with USB Type-C Receptacles		P
	A USB-based charger with a USB Type-C receptacle (Source) shall only apply power to VBUS when it detects a Sink is attached and shall remove power from VBUS when it detects the Sink is detached (vOPEN).		P
	A USB-based charger with a USB Type-C receptacle shall not advertise current exceeding 3.0 A except when it uses the USB-PD Discover Identity mechanism to determine the cable's actual current carrying capability and then it shall limit the advertised current accordingly.		P
	A USB-based charger with a USB Type-C receptacle (Source) which is not capable of data communication shall advertise USB Type-C Current of at least 1.5 A within tVBUSON of entering the Attached.SRC state and shall short D+ and D- together with a resistance less than 200 ohms. This will ensure backwards compatibility with legacy sinks which may use USB BC 1.2 for charger detection.		P
4.8.1.2	USB-based Chargers with USB Type-C Captive Cables		P
	A USB-based charger with a USB Type-C captive cable that supports USB PD shall only apply power to VBUS when it detects a Sink is attached and shall remove power from VBUS when it detects the Sink is detached (vOPEN).		P
	A USB-based charger with a USB Type-C captive cable that does not support USB PD may supply VBUS at any time. It is recommended that such a charger only apply power to VBUS when it detects a Sink is present and remove power from VBUS when it detects the Sink is not present (vOPEN).		P
	A USB-based charger with a USB Type-C captive cable shall limit its current advertisement so as not to exceed the current capability of the cable (up to 5 A).		P
	A USB-based charger with a USB Type-C captive cable which is not capable of data communication shall advertise USB Type-C Current of at least 1.5 A. It shall short D+ and D- together with a resistance less than 200		P

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Clause	Requirement + Test	Result - Remark	Verdict
	ohms. This will ensure backwards compatibility with legacy sinks which may use USB BC 1.2 for charging detection.		
	The voltage as measured at the plug of a USB-based charger with a USB Type-C captive cable may be up to $0.75 \times I / 3 \text{ V}$ ( $0 < I \leq 3 \text{ A}$ ), or $0.75 \times I / 5 \text{ V}$ ( $0 < I \leq 5 \text{ A}$ ) lower than the standard tolerance range for the chosen voltage, where $I$ is the actual current being drawn.		P
	A USB-based charger that advertises USB Type-C Current shall output a voltage in the range of $4.75 \text{ V} - 5.5 \text{ V}$ when no current is being drawn and between $4.0 \text{ V} - 5.5 \text{ V}$ at $3 \text{ A}$ . The output voltage as a function of load up to the advertised USB Type-C Current (default, $1.5 \text{ A}$ and $3 \text{ A}$ ) shall remain within the cross-hatched area shown in Figure 4-40.		P
	A USB PD-based charger that has negotiated a voltage $V$ at $\leq 3 \text{ A}$ shall output a voltage in the range of $V_{\text{max}} (V + 5\%)$ and $V_{\text{min}} (V - 5\%)$ when no current is being drawn and $V_{\text{max}}$ and $V_{\text{min}} - 0.75 \text{ V}$ at $3 \text{ A}$ . Under all loads, the output voltage shall remain within the cross-hatched area shown in Figure 4-41.		P
	A USB PD-based charger that has negotiated a voltage $V$ at between $3 \text{ A}$ and $5 \text{ A}$ shall output a voltage in the range of $V_{\text{max}} (V + 5\%)$ and $V_{\text{min}} (V - 5\%)$ when no current is being drawn and $V_{\text{max}}$ and $V_{\text{min}} - 0.75 \text{ V}$ at $5 \text{ A}$ . Under all loads, the output voltage shall remain within the cross hatched area shown in Figure 4-42.		P
<b>4.8.2</b>	<b>Non-USB Charging Methods</b>		P
	A product (Source and/or Sink) with a USB Type-C connector shall only employ signalling methods defined in USB specifications to negotiate power over its USB Type-C connector(s).		P
<b>4.8.3</b>	<b>Sinking Host</b>		P
	A Sinking Host is a special sub-class of a DRP that is capable of consuming power but is not capable of acting as a USB device. For example a hub's DFP or a notebook's DFP that operates as a host but not as a device.		P
	The Sinking Host shall follow the rules for a DRP (See Section 4.5.1.4 and Figure 4-15). The Sinking DFP shall support USB PD and shall support the DR_Swap command in order to get the Sink into the DFP data role.		P
<b>4.8.4</b>	<b>Sourcing Device</b>		N/A
	A Sourcing Device is a special sub-class of a DRP that is capable of supplying power but is not capable of acting as a USB host. For example a hub's UFP or a monitor's UFP that		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	operates as a device but not as a host.		
	The Sourcing Device shall follow the rules for a DRP (See Section 4.5.1.4 and Figure 4-15). It shall also follow the requirements for the Source as Power Source (See Section 4.8.1). The Sourcing Device shall support USB PD and shall support the DR_Swap command in order to enable the Source to assume the UFP data role.		N/A
<b>4.8.5</b>	<b>Charging a System with a Dead Battery</b>		N/A
	A system that supports being charged by USB whose battery is dead shall apply $R_d$ to both CC1 and CC2 and follow all Sink rules. When it is connected to a Source, DRP or Sourcing Device, the system will receive the default VBUS. It may use any allowed method to increase the amount of power it can use to charge its battery.		N/A
	Circuitry to present $R_d$ in a dead battery case only needs to guarantee the voltage on CC is pulled within the same range as the voltage clamp implementation of $R_d$ in order for a Source to recognize the Sink and provide VBUS. For example, a 20% resistor of value $R_d$ in series with a FET with $V_{GTH(max)} < V_{CLAMP(max)}$ with the gate weakly pulled to CC would guarantee detection and be removable upon power up.		N/A
	When the system with a dead battery has sufficient charge, it may use the USB PD DR_Swap message to become the DFP.		N/A
<b>4.8.6</b>	<b>USB Type-C Multi-Port Chargers</b>		N/A
	A USB Type-C Multi-Port Charger is a product that exposes multiple USB Type-C Source ports for the purpose of charging multiple connected devices. A compliant USB Type-C charger may offer on each of its ports a mix of power options as defined in Section 4.6.		N/A
	Multi-Port Chargers will generally fall into two categories as defined by the following.		N/A
	1. Assured Capacity Chargers: a multi-port charger where the sum of the maximum capabilities of all of the exposed ports, as indicated to the user, is equal to the total power delivery capacity of the charger.		N/A
	2. Shared Capacity Chargers: a multi-port charger where the sum of the maximum capabilities of all of the exposed ports, as indicated to the user, is less than the total power delivery capacity of the charger.		N/A
	A Multi-Port Charger may offer in a single product separate visually identifiable groupings of charging ports. In this case, each group can independently offer either one of the two		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	charging categories, either an Assured Capacity Charger or a Shared Capacity Charger.		
	This section defines the requirements and provides guidelines for the operation and behaviour of a USB Type-C Multi-Port Charger.		N/A
4.8.6.1	General Requirements		N/A
	Individual source ports shall always comply with power negotiation and rules set forth by the USB Type-C and USB Power Delivery specifications, adjusted as needed when available resources change as other ports take more or less power.		N/A
	The minimum capability of all individual USB Type-C ports of a USB Type-C Multi-Port Charger shall be 5V @ 1.5 A independent of how many of the other ports are in use.		N/A
	When a USB Type-C Charger includes charging ports that are based on USB Standard-A receptacles, the following requirements shall be met.		N/A
	The USB Standard-A ports shall be implemented as an independent group, i.e. USB Standard-A ports shall not be included in a group of USB Type-C ports behaving as a Shared Capacity Charger. Any load change on a USB Type-A port shall not result in a voltage change on any of the USB Type-C ports and vice-versa.		N/A
	The minimum capability of each USB Standard-A port shall be 5V @ 500 mA independent of how many of the other ports are in use.		N/A
4.8.6.2	Multi-Port Charger Behaviors		N/A
	Each Source port of Assured Capacity Chargers shall, by design, behave independently and be unaffected by the status and loading of the other ports. An exception to this behavior is allowed if the charger has to take any action necessary to meet an overall product operational safety requirement due to unexpected behavior on any port.		N/A
	For Shared Capacity Chargers, the following behavioral rules shall apply:		N/A
	Each of the exposed Source Ports shall have the same power capabilities. Each port of the charger shall be capable of the same maximum capability, minimum capability, and be able to draw from the shared power equally.		N/A
	All exposed USB PD unattached Source Ports shall have the same power capabilities.		N/A
	Ports shall have the ability to supply the available shared capacity power up to the port's maximum power.		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
	A shared capacity charger's ports may offer less than this value but shall increase the offer up to the required value when the Sink sets the Capabilities Mismatch bit in its response. This may be done in multiple steps, but all ports in the Shared Capacity Group shall reach the maximum power within three seconds.		N/A
	Whenever a power contract is made or changed on any port, the available shared capacity shall be re-computed, and the source shall send updated Source Capability messages as needed.		N/A
	As ports of a Shared Capacity Group are connected, each remaining unattached Source Port shall be capable of advertising the lower of the Maximum Capability of the port OR the Total Shared Capacity – the contracted power for the attached ports – (the number of unattached ports – 1) * the minimum port power.		N/A
	Ports shall offer at least 7.5 W.		N/A
	When calculating the available shared capacity for ports in a Fixed Supply power contract, the shared capacity charger shall use the Voltage times the Maximum Current in the PDO as the power the port is supplying regardless of the actual Operating Current requested in the RDO request.		N/A
	When calculating the available shared capacity for ports in a Fixed Supply power contract, the shared capacity charger shall use the Voltage times the Maximum Current in the PDO as the power the port is supplying regardless of the actual Operating Current requested in the RDO request.		N/A
	Ports when not in a PD contract shall follow the rules for a shared USB Type-C Current source unless there is sufficient remaining power for each port to advertise 15 W.		N/A
	All exposed USB Type-C Current ports shall have the ability to offer the same power capabilities.		N/A
	All ports shall initially offer at least 1.5 A.		N/A
	The total of offers across all the ports shall never exceed the capacity of the shared supply.		N/A
	Ports that initially offer 1.5 A shall increase to 3 A after attach if they have sufficient available shared capacity within one second.		N/A
	Ports shall never offer less than 1.5 A – e.g. shall not offer Default.		N/A
	As Source ports are connected and begin providing power, the remaining Source ports will each have the same power capabilities. The maximum capability may be less than the		N/A



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	previously connected ports due to less unused capacity of the total power delivery capacity of the charger. For example, if the total power delivery capacity of a USB Type-C two-port charger is 60 W with a port PDP of 35 W and the first connected Source port has established a 35 W power contract with its connected Sink, then the second Source port will only be able to offer a PDP of 25 W.		
	Each port should start by offering the minimum capability for the port and increase the offering to the Sink upon a connection. For example, if the maximum capability of a USB Type-C only Source port is 3 A, then all of the exposed Source ports will be able to offer 3A. Each port should start by offering less than the max (such as 1.5 A) and then increase the offering to 3 A after an attach. This would happen for each port as it is connected until the unused shared capacity is exhausted, at which point no other ports would increase to 3 A offering. A sink, in this example, would see a starting advertisement of USB Type-C Current @ 1.5 A at attach and would then see the USB Type-C Current advertisement increase to 3 A. As another example, if the maximum capability of a USB Type-C Source port is to offer USB PD with a PDP of 35 W, then all of the exposed Source ports would also support USB PD 35 W. Each port would start by offering something less on initial connection, like 15 W, and then increase the offering with new Source Capabilities when it determines the Sink would like more power. If the Sink is not offered the power it requires, it will send a request with the Capability Mismatch bit set to indicate to the source it wants more power. This will happen for each port as it is connected until the unused shared capacity is exhausted, at which point no other ports would increase the power offering.		N/A
	When establishing the remaining available capacity, a charger that supports policy-based power rebalancing may include the power that can be reclaimed from ports already in use:		N/A
	1. by adjusting advertised source capabilities equivalent with a reduced PDP to one or more ports that are already in use; or		N/A
	2. by issuing a USB PD GotoMin command to one or more ports already in use.		N/A
	Policy-based power rebalancing should consider providing good user experience and preserving nominal USB functionality on impacted devices. Fixed rebalancing algorithms that do not factor in overall USB system policy may not be appropriate for power rebalancing		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	implementations.		
4.8.6.3	Multi-Port Charger Port Labeling		N/A
	Multi-port chargers shall have OEM-designed port labeling consistent with the following rules.		N/A
	For Assured Capacity Chargers, each exposed Source port shall be labeled to indicate the PDP of the port. In this case, the user will be able to expect that each of the labeled ports will be able to meet power contracts consistent with the labelling independent of how many of the Source ports are in use.		N/A
	For Shared Capacity Chargers, each Source port shall be labeled to indicate the same PDP. Additionally, the charger shall have a label that, with a minimum of equal visual prominence, indicates the total power delivery capacity being shared across all of the ports identified as a group.		N/A
	A Multi-Port Charger that offers in a single product separate groupings of charging ports, each grouping shall be clearly identified as a separate grouping and each grouping shall be individually labeled consistent with that group's behavior model, either as an Assured Capacity Charger or a Shared Capacity Charger.		N/A
	Refer to the USB Implementers Forum (USB-IF) for USB Type-C Chargers certification along with further labeling guidelines.		N/A
4.8.6.4	Multi-Port Charger that include USB Data Hub Functionality		N/A
	Multi-Port chargers that also incorporate USB data hub capabilities shall meet the same requirements as standalone chargers. These charging-capable hubs shall be self-powered and shall fully operate as a charger independent of the state of the USB data bus connections.		N/A
	For hub-based Multi-Port Chargers that offer power to the upstream-facing port (to the host), this port may either behave as an Assured Capacity Charging port (e.g. be a dedicated charging port) or as a Shared Capacity Charging port (e.g. sharing capacity with downstream-facing ports). In either case, it should be clearly labeled consistent with its designed behavior, including identifying it as part of a group if it is sharing capacity with other ports.		N/A
	When the upstream-facing port is sharing capacity with the downstream-facing ports, the PDP of the upstream-facing port can differ from the downstream-facing ports.		N/A
4.9	<b>Electronically Marked Cables</b>		P

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Clause	Requirement + Test	Result - Remark	Verdict
	All USB Full-Featured Type-C cables shall be electronically marked. USB 2.0 Type-C cables may be electronically marked. An eMarker is element in an Electronically Marked Cable that returns information about the cable in response to a USB PD Discover Identity command.		N/A
	Electronically marked cables shall support USB Power Delivery Structured VDM Discover Identity command directed to SOP' (the eMarker). This provides a method to determine the characteristics of the cable, e.g. its current carrying capability, its performance, vendor identification, etc. This may be referred to as the USB Type-C Cable ID function.		N/A
	Prior to an explicit USB PD contract, a Sourcing Device is allowed to use SOP' to discover the cable's identity. After an explicit USB PD contract has been negotiated, only the Source shall communicate with SOP' and SOP" (see Section 6.2.1).		N/A
	Passive cables that include an eMarker shall follow the Cable State Machine defined in Section 4.5.2.4 and Figure 4-20.		N/A
	Once VCONN is available, all electronically marked cables shall use it as the only power source. If VCONN is applied after VBUS then until VCONN is available, the cable may remain unpowered or may draw power from VBUS. Within tVCONNSwitch, the cable shall switch from VBUS to VCONN. Cables that include an eMarker shall meet the maximum power defined in Table 4-6. The only exception is an Optically Isolated Active Cable (OIAC Section 6), which can draw from both VCONN and VBUS.		N/A
	Refer to Table 4-5 for the requirements of a Source to supply VCONN. When VCONN is not present, a powered cable shall not interfere with normal CC operation including Sink detection, current advertisement and USB PD operation.		N/A
	Figure 4-43 illustrates a typical electronically marked cable. The isolation elements (Iso) shall prevent VCONN from traversing end-to-end through the cable. Ra is required in the cable to allow the Source to determine that VCONN is needed.		N/A
	Figure 4-44 illustrates an electronically marked cable where the VCONN wire does not extend through the cable, therefore an SOP' (eMarker) element is required at each end of the cable. In this case, no isolation elements are needed.		N/A
	For cables that only respond to SOP', the location of the responder is not relevant.		N/A
<b>4.9.1</b>	<b>Parameter Values</b>		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
<b>4.9.2</b>	<b>Active Cables</b>		P
	An active cable is an electronically marked cable that incorporates data bus signal conditioning circuits, for example to allow for implementing longer cables. Active cables with data bus signal conditioning in both plugs shall implement SOP' and may implement SOP". Active cables shall meet the power requirements defined in Table 4-6.		P
	Active cables may support either one TX/RX pair or two TX/RX pairs. The eMarker in the cable shall identify the number of TX/RX lanes supported. Active cables may or may not require configuration management. Active cable configuration management is defined in Section 5.5.4.		P
<b>4.10</b>	<b>VCONN-Powered Accessories (VPAs) and VCONN-Powered USB Devices (VPDs)</b>		P
	VCONN-Powered Accessories and VCONN-Powered USB Devices are both direct-attach Sinks that can operate with just VCONN.		P
	Both expose a maximum impedance to ground of Ra on the VCONN pin and Rd on the CC pin.		P
	The removal of VCONN when VBUS is not present shall be treated as a detach event.		P
<b>4.10.1</b>	<b>VCONN-Powered Accessories (VPAs)</b>		P
	A VCONN-Powered Accessory implements an Alternate Mode (See Appendix E).		P
	VCONN-Powered Accessories shall comply with Table 4-7.		P
	When operating in the Sink role and when VBUS is not present, VCONN-Powered Accessories shall treat the application of VCONN as an attach signal, and shall respond to USB Power Delivery messages.		P
	When powered by only VCONN, a VCONN-Powered Accessory shall negotiate an Alternate Mode. If it fails to negotiate an Alternate Mode within tAMETimeout, its port partner removes VCONN.		P
	When VBUS is supplied, a VCONN-Powered Accessory is subject to all of the requirements for Alternate Modes, including presenting a USB Billboard Device Class interface if negotiation for an Alternate Mode fails.		P
	Should a VCONN-Powered Accessory wish to provide charge-through functionality, it must do so by negotiating voltage and current independently on both the Host and charge-through ports, and possibly re-regulating the voltage from the Source before passing it through to the Sink. The Sink is able to take the		P

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	full current that is advertised to it by the VCONN-Powered Accessory.		
<b>4.10.2</b>	<b>VCONN-Powered USB Devices (VPDs)</b>		P
	A VCONN-Powered USB Device shall implement a USB UFP endpoint.		P
	VCONN-Powered USB Devices shall comply with Table 4-8.		P
	When VBUS is not present, VCONN-Powered USB Devices shall treat the application of VCONN as an attach signal.		P
	A VCONN-Powered USB Device shall respond to USB PD messaging on SOP' and shall not respond to other USB PD messaging. A VCONN-Powered USB Device shall respond to USB PD Hard Reset and Cable Reset signaling.		P
	A Charge-Through VCONN -Powered USB Device shall discard all USB PD messages while a connection is enabled between the host port CC and Charge-Through port CC.		P
	When VBUS is supplied by the Host, the VCONN-Powered USB Device shall behave like a normal UFP Sink, but still only respond to USB PD messaging on SOP'. If VBUS is subsequently removed while VCONN remains applied, the VCONN-Powered USB Device shall remain connected, and use VCONN as the sole detach signal.		P
	Since VCONN-Powered USB Devices do not respond to USB PD on SOP, they cannot enter Alternate Modes.		P
	A VCONN-Powered USB Device may provide Charge-Through functionality via VPD Charge-Through. VCONN-Powered USB Devices shall not provide any data pass-through to the Charge-Through port other than the CC wire.		P
	Since the power and CC negotiation is passed through directly, the Sink shall limit its maximum current based on the additional impedance introduced by the VCONN-Powered USB Device.		P
	Additionally, since power can only flow from the Charge-Through port to the Host, VCONN must be provided by the host, and there is no data connection beyond the CC wire passed through to the connected source, there are limitations on what the Host can advertise and support via USB PD:		P
	The Host shall not negotiate or accept a PR_Swap or VCONN_Swap		P
	The Host shall not enable FR_Swap		P
	The Host may only negotiate a DR_Swap when using USB PD Revision 2.0, and only for the		P



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	purpose of switching which side initiates PD communications. The Host will always remain a DFP for USB data.		
	The Host shall not advertise dual-role data or dual-role power in its SourceCapability or SinkCapability messages – Host changes its advertised capabilities to UFP role/sink only role.		P
	The Host shall not negotiate any Alternate Modes that change the function of pins on the connector.		P
	The Host shall represent itself to the Charge-Through Source using USB PD as if it were a Sink-only, data-less device.		P
<b>4.11</b>	<b>Parameter Values</b>		P
<b>4.11.1</b>	<b>Termination Parameters</b>		N/A
	Table 4-24 provides the values that shall be used for the Source's Rp or current source. Other pull-up voltages shall be allowed if they remain less than 5.5 V and fall within the correct voltage ranges on the Sink side – see Table 4-32, Table 4-33 and Table 4-34. Note: when two Sources are connected together, they may use different termination methods which could result in unexpected current flow.		N/A
	The Sink may find it convenient to implement Rd in multiple ways simultaneously (a wide range Rd when unpowered and a trimmed Rd when powered). Transitions between Rd implementations that do not exceed tCCDebounce shall not be interpreted as exceeding the wider Rd range. Transitions between Rd implementations shall not allow the voltage on CC to go outside the voltage band that defines a connection. Table 4-25 provides the methods and values that shall be used for the Sink's Rd implementation.		N/A
	Table 4-27 provides the minimum impedance value to ground on CC for a device (Sink or Source) to be undetected by a Source. This shall apply for ports in the Disabled state or ErrorRecovery state. This shall also apply for Sources when unpowered (for example a power brick unplugged from AC mains).		N/A
<b>4.11.2</b>	<b>Timing Parameters</b>		P
	Table 4-29 provides the timing values that shall be met for delivering power over VBUS and VCONN.		P
	Figure 4-46 illustrates the timing parameters associated with the DRP toggling process. The tDRP parameter represents the overall period for a single cycle during which the port is exposed as both a Source and a Sink. The portion of the period where the DRP is exposed		P



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	as a Source is established by dcSRC.DRP and the maximum transition time between the exposed states is dictated by tDRPTransition.		
	Table 4-30 provides the timing values that shall be met for DRPs. The clock used to control DRP swap should not be derived from a precision timing source such as a crystal, ceramic resonator, etc. to help minimize the probability of two DRP devices indefinitely failing to resolve into a Source-to-Sink relationship. Similarly, the percentage of time that a DRP spends advertising Source should not be derived from a precision timing source.		P
	Table 4-31 provides the timing requirement for CC connection behaviors.		P
<b>4.11.3</b>	<b>Voltage Parameters</b>		N/A
	Table 4-32, Table 4-33 and Table 4-34 provide the CC voltage values that a Source shall use to detect what is attached based on the USB Type-C Current advertisement (Default USB, 1.5A @ 5 V, or 3.0 A @ 5 V) that the Source is offering.		N/A
	Table 4-35 provides the CC voltage values that shall be detected across a Sink's Rd for a Sink that does not support higher than default USB Type-C Current Source advertisements.		N/A
	Table 4-36 provides the CC voltage values that shall be detected across a Sink's Rd for a Sink that implements detection of higher than default USB Type-C Current Source advertisements. This table includes consideration for the effect that the IR drop across the cable GND has on the voltage across the Sink's Rd.		N/A
	Table 4-37 provides the clamping voltage that any port (Source, Sink or DRP) may clamp its CC pin to protect from damage. The inclusion of clamping shall not impact the functionality when the CC pin is functioning as VCONN Source or Sink.		N/A
<b>5</b>	<b>USB4 Discovery and Entry</b>		N/A
	USB4™ discovery and operational entry differs significantly from USB 2.0 and USB 3.2. This chapter defines the process of discovering across a USB Type-C® connection that both port partners are USB4-capable (or not), having the DFP-side of the link make a decision regarding to enter USB4 operation (or not), and how operational entry is accomplished.		N/A
<b>5.1</b>	<b>Overview of the Discovery and Entry Process</b>		N/A
	The following provides an overview of the general process for discovery and entry into		N/A

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	USB4 operation.		
	1. USB Type-C CC Connection State Machines resolve Source/Sink and the initial data roles (DFP/UFP).		N/A
	2. Initial VBUS and VCONN power is supplied.		N/A
	3. USB Power Delivery protocol is used to establish a power contract between the port partners.		N/A
	4. USB PD Discover Identity process is used by the DFP to identify port partner (SOP) capabilities.		N/A
	5. USB PD Discover Identity process is used by the DFP to identify cable (SOP') capabilities.		N/A
	6. If the cable and port partner both support USB4 operation, the DFP issues USB PD Enter_USB Messages to both the cable (if it is an active cable) and port partner to enter USB4 operation.		N/A
	7. If both port partners are Dual-Role-Data (DRD) capable, either the DFP or UFP can optionally initiate a data-role swap in order to exchange host and device roles.		N/A
	The first three steps above are the same as used for all USB connections for establishing port relationships and power between the port partners. Step 5 where the cable is queried for its capabilities may optionally occur during Step 3, this would most likely be done before if the Source needs to know if the cable supports supplying current beyond 3 A.		N/A
	Depending on the resulting power source relationship after the first few steps, the use of USB PD DR_Swap may be necessary to establish the port partner that is closest to the host as the data role DFP. For example, a hub supplying power to a host and DR_Swap is used to correct the data roles between the hub and host.		N/A
	After the port partner's capabilities are identified by the DFP, it may be appropriate based on what is discovered about the port partner to also query the port partner using the USB PD Alternate Mode SVID discovery process as an extension to Step 4. There are situations where a port partner supports Alternate Modes that may also be useable during USB4 operation and this would be discovered during this additional query.		N/A
	After the cable capabilities are identified by the DFP, it may be appropriate based on what is discovered about the cable to also query the cable using the USB PD Alternate Mode SVID discovery process as an extension to Step 5. There are situations where a cable that supports Thunderbolt™ 3 Alternate Mode may		N/A

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	also be useable for USB4 operation and this would be discovered during this additional query.		
	USB4 operation is entered using a USB PD USB Enter_USB Message. This message will be sent to both the cable (SOP' and also SOP" if present) and the port partner (SOP), each of which will respond with an Accept message to confirm and establish when the cable or port partner is functionally ready for USB4 operation. If the cable to be used will be operating in Thunderbolt 3 Alternate Mode, then the cable will be enabled using the USB PD Enter Mode Command instead of the USB PD USB Enter_USB Message (See Appendix F).		N/A
	USB4 functionally enables an ability for connecting two host platforms and establishing a data channel between the hosts, this is dependent on at least one of these host platforms being capable of Dual-Role-Data operation so that a proper USB Type-C DFP-to-UFP data relationship can be established between them. In most cases, both host platforms will be DRD-capable and once USB4 operation is established, either of these host platforms can choose to initiate a change of its role in the DFP-to-UFP relationship. To accomplish this, the USB PD DR_Swap process is used during Step 7 listed above.		N/A
<b>5.2</b>	<b>USB4 Functional Requirements</b>		N/A
	The following functional requirements are for USB4 hosts and devices.		N/A
<b>5.2.1</b>	<b>USB4 Host Functional Requirements</b>		N/A
	USB4 hosts shall meet the following functional requirements:		N/A
	USB4 hosts with dual-role-data (DRD) support shall respond to USB PD Discover Identity command with both DFP and UFP VDOs.		N/A
<b>5.2.2</b>	<b>USB4 Device Functional Requirements</b>		N/A
	USB4 devices shall meet the following functional requirements:		N/A
	USB4 devices shall respond to USB PD Discover Identity command with UFP VDOs.		N/A
	USB4 devices shall provide a USB interface exposing a USB Billboard Device Class when it cannot connect as a USB4 device within tUSB4Timeout.		N/A
	If the USB4 device additionally supports Alternate Modes, the device shall complete the USB4 discovery and entry process (successful or not) before falling back to USB 3.2 or USB		N/A

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	2.0 and exposing an appropriate USB Billboard Device Class.		
<b>5.2.3</b>	<b>USB4 Alternate Mode Support</b>		N/A
	The USB4 specification enables products to be designed to support Alternate Modes, specifically DisplayPort™ Alt Mode and Thunderbolt 3 Alt Mode. Unlike USB 3.2 and USB 2.0 hubs, this also includes supporting specific Alternate Modes on USB4 hubs.		N/A
5.2.3.1	USB4 Alternate Mode Support on Hosts		N/A
	For USB4 hosts that implement DisplayPort Tunneling, DP Alt Mode with Multi-function support (DP_BR 1 channel signaling combined with USB 3.2 support) as defined by the DisplayPort Alt Mode specification shall be implemented on all of its USB Type-C DFPs.		N/A
	The USB4 host shall support the first connected DisplayPort display on any of its USB Type-C ports. Support for subsequently connected DisplayPort displays is optional.		N/A
	USB4 hosts may optionally implement TBT3 compatibility support as defined by the USB4 specification on its USB Type-C DFPs.		N/A
5.2.3.2	USB4 Alternate Mode Support on Hubs and USB4-based Docks		N/A
	USB4 hubs and USB4-based docks shall implement DP Alt Mode with Multi-function support (DP_BR 1 channel signaling combined with USB 3.2 support) as defined by the DisplayPort Alt Mode specification on all exposed USB Type-C DFPs.		N/A
	USB4 hubs shall support the first connected DisplayPort display on any of its USB Type-C DFPs. Support for subsequently connected DisplayPort displays is optional.		N/A
	USB4-based docks shall support the first connected display on any of its USB Type-C DFPs or non-USB display connectors (if present, collectively). Support for subsequently connected displays is optional.		N/A
	USB4 hubs shall implement TBT3 compatibility support as defined by the USB4 specification on its USB Type-C DFPs. USB4-based docks shall implement TBT3 compatibility support as defined by the USB4 specification on its USB Type-C UFP and USB Type-C DFPs.		N/A
	For USB4 hubs, downstream-facing ports shall not implement Alternate Modes that do not have a USB-IF Standard ID (SID) or Accessory Modes.		N/A
<b>5.3</b>	<b>USB4 Power Requirements</b>		N/A
	USB4 requires that the power connection		N/A

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	between the port partners be established and maintained using USB PD prior to and throughout USB4 operation. A USB4 port, prior to entering USB4 operation, shall operate as a USB 3.2 port with regarding power (See Section 4.6). USB4 does not use the USB device protocols defined in USB 2.0 and USB 3.2 for managing device power.		
<b>5.3.1</b>	<b>Source Power Requirements</b>		N/A
	For USB Type-C ports that support USB4 data bus operation, the following requirements shall be met.		N/A
	USB4 ports shall be minimally capable of supplying at least 7.5 W (i.e. 5 V @ 1.5 A) on VBUS to bus-powered USB4 devices.		N/A
	The minimum capability for powering bus powered devices on data-capable ports shall be independently met on each USB Type-C port of a multi-port host or hub.		N/A
<b>5.3.2</b>	<b>Sink Power Requirements</b>		N/A
	For USB4 devices that rely on bus power to operate (independent of any charging needs), the following requirements shall be met.		N/A
	USB4 devices shall draw only up to 250 mA on VBUS when the Source advertises Default USB power (see Section 4.11.1) prior to a USB PD power contract being made between the device and its port partner.		N/A
	USB4 devices may draw higher levels of power prior to a USB PD power contract being made if the Source advertises USB Type-C Current at either 1.5 A or 3.0 A.		N/A
	USB4 devices shall be minimally capable of operating with a Source that only delivers up to 7.5 W (i.e. 5 V @ 1.5 A).		N/A
	USB4 devices shall not enter into USB4 data bus operation until after a USB PD power contract has been established, and while in USB4 operation, the device shall adhere to USB PD power behavioral requirements at all times including appropriately responding to changes in Source capabilities.		N/A
	In cases where the full functional capabilities or the highest performance of the USB4 device requires more than the power being offered by the host, the device shall be minimally capable of providing the user with basic functionality as expected for the type and listed functions of the device. This allows for making available a higher level of operation or performance when a higher level of power is supplied, e.g. 15 W for full functionality versus 7.5 W for basic functionality. In this case, the device shall expose a Billboard that indicates functionality is limited by the available power.		N/A



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<b>5.3.3</b>	<b>Device Power Management Requirements</b>		N/A
	For USB4, device power management is enabled using a combination of USB PD capabilities that operate in conjunction with the USB4 link states of the device's UFP connection.		N/A
	The connection between the device's UFP and its DFP port partner can be put into a suspend state based on the value of the USB Suspend Supported Flag in the Source-Capabilities Message used in the USB PD explicit power contract.		N/A
	When the USB Suspend Supported Flag is set by the Source, the Sink shall meet the Suspend power requirement when the USB4 link is in the CLd state. Prior to the entry of the link into CLd state, it is expected that the host will have placed all of the device's functions into an appropriate suspend state.		N/A
	Suspend power is defined based on the capabilities of the USB4 device:		N/A
	USB4 Device that is not capable of remote wake or has remote wake disabled: 25 mW		N/A
	USB4 Device that supports remote wake and has remote wake enabled: 50 mW		N/A
	If the Source clears the USB Suspend Supported Flag, the Sink shall follow Explicit Contract power requirements regardless of the USB4 link state. For USB4, the use of USB PD zero negotiated current is not a valid Suspend entry method since it is not coordinated with the host operating system and the function device drivers.		N/A
<b>5.4</b>	<b>USB4 Discovery and Entry Flow Requirements</b>		N/A
	This section provides the detailed requirements for USB4 discovery and entry. Additional requirements related to USB4 operation are in the USB4 Specification.		N/A
	Prior to entering and during USB4 operation, the functional requirements of Chapter 3.11.1 shall be met including all functional interface and configuration channel (CC) requirements.		N/A
<b>5.4.1</b>	<b>USB Type-C Initial Connection</b>		N/A
	For a USB4-capable port, prior to initiating USB4 cable and device discovery, a valid Source-to-Sink connection shall exist and the USB Type-C connection state machine of the port shall either be in the Attached.SRC or Attached.SNK state.		N/A
	When two USB4 dual-role-data (DRD) ports are connected together, e.g. two USB4 hosts, USB Type-C connection process will establish the initial data roles between the port partners.		N/A



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	Once the initial data roles are established, the USB4 DFP may immediately proceed to train the link for USB 3.2. If a UFP is USB4 capable, it shall hold off exposing SuperSpeed USB terminations until the completion of the USB4 discovery and entry process or tUSB4Timeout. Once the USB4 discovery and entry process has completed, the UFP will enable SuperSpeed USB device terminations either via the USB4 SuperSpeed USB tunnel or natively depending on whether the completed port connection is USB4 or USB 3.2, respectively.		N/A
<b>5.4.2</b>	<b>USB Power Delivery Contract</b>		N/A
	Prior to initiating USB4 device discovery, the port partners shall negotiate a USB PD Explicit Contract.		N/A
	During the process of establishing a stable USB PD Explicit Contract, the Source or Sink may have initiated power-role and VCONN swaps. Prior to moving on to USB4 discovery, the functional data role shall be properly established (e.g. a self-powered hub upstream facing port is a DRP and comes up as a Source where DR_Swap is then required to the correct data role to the hub) and the DFP shall be the source of VCONN.		N/A
<b>5.4.3</b>	<b>USB4 Discovery and Entry Flow</b>		N/A
	Figure 5-1 illustrates the basic flow model for USB4 discovery and entry.		N/A
5.4.3.1	USB4 Device Discovery (SOP)		N/A
	USB4 device discovery shall occur only after having a negotiated USB PD Explicit Contract.		N/A
	USB4 device discovery involves the use of the USB PD Discover ID process between the DFP and its port partner (SOP).		N/A
5.4.3.2	USB4 Cable Discovery (SOP' )		N/A
	The DFP shall determine that the attached cable is USB4-compatible prior to entering into USB4 operation. In cases where the USB4 device is directly connected or has a captive cable, the USB4 device shall respond to USB4 cable discovery on SOP' as a captive passive cable and indicating the appropriate USB Signaling support.		N/A
	Table 5-1 summarizes the list of cables that are intended to support USB4-compatible operation. Regarding Active Cables, this list does not include Optically-Isolated Active Cables (OIACs) which are to be handled as a special case given that these cables do not support USB 2.0 and power delivery over the cable (See Chapter 6).		N/A
	Determining if the cable is USB4-compatible starts the use of the USB PD Discover ID		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	process between the DFP and the attached cable (SOP'). If no response is received when the DFP issues a USB PD Discover ID command to the cable, then the USB4 discovery process shall be exited and the DFP shall proceed to establish a functional connection to its UFP port partner following traditional USB 2.0 process.		
	USB4-compatible support is generally determined based on the USB Signaling Support indicated in the cable VDO responses appropriate for the type of cable it is, passive or active, with compatible passive cables being those that indicate USB signaling support for Gen1 or higher and with compatible active cables being those that indicate USB signaling support for Gen2 or higher.		N/A
	When a passive cable is identified as a USB 3.2 Gen2 cable and the DFP is Gen3 capable, the DFP needs to check further using USB PD Alternate Mode process to determine if the cable is a Thunderbolt 3 passive cable supporting Gen3.		N/A
	Some existing Thunderbolt 3 active cables may not support USB4 operation, discovery and use of this cable is optional. Please refer to Appendix F regarding how to discover and support these cables.		N/A
5.4.3.2.1	Discovering Passive Cables		N/A
	The USB PD specification defines the Passive Cable VDO responses to the Discover Identity Command sent by the DFP to a USB4-compatible passive cable.		N/A
	If the USB Signaling field [B2...0] in the Passive Cable VDO response is 011b (USB4 Gen3), the USB4 discovery process is complete and USB4 operation up to as high as 40 Gbps is supported. In Chapter 3 of this specification, these cable assemblies are those with the following cable references: CC4G3-3 and CC4G3-5 indicated in Table 3-1.		N/A
	If the USB Signaling field [B2...0] in the Passive Cable VDO response is 000b (USB 2.0 only), the USB4 discovery process will be exited and the DFP shall proceed to establish a functional connection to its UFP port partner following traditional USB 2.0 process.		N/A
	If the USB Signaling field [B2...0] in the Passive Cable VDO response is either 010b (USB 3.2 Gen2) or 001b (USB 3.2 Gen1), the USB4 discovery process is complete if the DFP is limited to USB4 Gen2. In Chapter 3 of this specification, these cable assemblies are those with the following cable references: CC3G2-3, CC3G2-5, CC3G1-3, and CC3G1-3 indicated in		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	Table 3-1. Note that USB 3.2 Gen1 cables, while not tested and certified to be used for USB 3.2 Gen2 operation, are expected to work for USB4 Gen2 operation.		
	If the USB Signaling field [B2...0] in the Passive Cable VDO response is 010b (USB 3.2 Gen2) but the DFP is capable of USB4 Gen3 operation, then the DFP shall use the USB PD Alternate Mode process to determine if the cable also can be identified as a TBT3 Gen3 cable. Refer to Section 5.4.3.2.3 for TBT3 cable discovery process. If the Cable Speed field of the Discover Modes VDO response is set to 011b, then the USB4 discovery process is complete and USB4 operation up to as high as Gen3 is supported using the TBT3 passive cable (see Table F-11).		N/A
5.4.3.2.2	Discovering Active Cables		N/A
	The USB PD specification defines the Active Cable VDO responses to the Discover Identity Command sent by the DFP to a USB4-compatible active cable.		N/A
	If the USB Signaling Support field [B2...0] in the Active Cable VDO 1 response is 011b (USB4 Gen3), the USB4 discovery process is complete and USB4 operation up to as high as Gen3 is supported.		N/A
	Optionally, discovery and use of existing TBT3 active cables that indicate support for rounded data rate operation is allowed if the active cable isn't explicitly identified as USB4-compatible.		N/A
	Failure to identify that the attached active cable is USB4-compatible will result in exiting the USB4 discovery process and reverting to following traditional USB 3.2 and USB 2.0 process.		N/A
5.4.3.2.3	Process for Discovering Thunderbolt 3 Cables		N/A
	The USB PD specification defines the process for discovering Alternate Mode-enabled cables. The following summarizes this process specific to discovering Thunderbolt 3 cables for purposes of determining USB4-compatibility. Prior to performing these steps, the USB PD Discover Identity process will have already been used to establish if the cable is passive or active.		N/A
	The following steps are used for discovering Thunderbolt 3 cables and the cable's capabilities using the USB PD Alternate Mode process.		N/A
	1. DFP issues the Discover SVIDs command to the cable SOP'.		N/A
	2. If the cable's Discover SVID response indicates 0x8087 (Intel/TBT3) as one of its SVIDs, then proceed to next step, otherwise		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	the cable is not a Thunderbolt 3 cable (see Section F.2.4).		
	3. DFP issues the Discover Modes command with its SVID set to 0x8087 to the cable's SOP'.		N/A
	4. If this discovery is part of the USB4-compatible passive cable discovery process, from the cable's Discover Modes VDO responses (see Section F.2.6), extract the value in the Cable Speed field to complete the process.		N/A
	5. If this discovery is part of the USB4-compatible active cable discovery process, from the cable's Discover Modes VDO responses (see Section F.2.6), extract the value in the TBT_Rounded_Support field to complete the process. [Note: discovery and use of USB4-compatible TBT3 active cables is an optional feature that also would require use of USB PD Enter Mode command to enable the cable for USB4 operation.]		N/A
5.4.3.3	USB4 Operational Entry		N/A
	USB4 operational entry shall occur only after having established that the attached cable, if present, and the port partner are USB4-capable.		N/A
	USB4 operational entry involves the use of the USB PD Enter_USB Message process between the DFP and both the attached USB4-compatible cable and the USB4-capable port partner – sending this message is order specific: SOP' first, SOP" second if present, and SOP third. Sending the USB PD Enter_USB Message to SOP' and SOP" is not needed for passive cables.		N/A
	When using the USB PD Enter_USB Message for enabling USB4 operation, the DFP shall indicate 010b (USB4) in the USB Mode field of the Enter_USB Data Object. The remaining fields shall be set appropriately by the DFP based on the capabilities of the DFP and attached cable.		N/A
<b>5.4.4</b>	<b>USB4 Post-Entry Operation</b>		N/A
5.4.4.1	During USB4 Operation		N/A
	While in USB4 operation, the following are allowed:		N/A
	The USB PD explicit power contract may be re-negotiated.		N/A
	Issue an USB PD Data_Reset command to change the mode of operation, e.g. from USB4 to USB 3.2 or an Alternate Mode.		N/A
	Enable Alternate Modes that do not reconfigure the port interface and operate in parallel with USB4.		N/A
5.4.4.2	Exiting USB4 Operation		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	The USB PD Data_Reset process causes USB data connections to be reset and Alternate Modes to be exited. This process does not change the existing power contract and data roles between the port partners. The Data_Reset process shall include the following steps:		N/A
	Issue a USB PD Data_Reset command to the SOP port partner to reset the data bus, reset the cable, and exit any Alternate Modes while preserving the power on VBUS.		N/A
	The tUSB4Timeout and tAMETimeout timers within the UFP shall be reset upon sending or receiving a USB PD Data_Reset command.		N/A
	Re-enter the USB4 Discovery and Entry process (Section 5.4.3).		N/A
<b>5.5</b>	<b>USB4 Hub Connection Requirements</b>		N/A
	USB4 hub behavior with regard to managing its DFP connections has USB4-specific dependencies on the connection status and capabilities of its single UFP. Additionally, hubs have USB4-specific responsibilities for communicating the capabilities of the USB4 host to downstream-connected USB4 hubs. This section provides both requirements and guidance for USB4 hub port connection behavior.		N/A
<b>5.5.1</b>	<b>USB4 Hub Port Initial Connection Requirements</b>		N/A
	The following requirements apply to all hub ports.		N/A
	1. Run the USB Type-C Connection process,		N/A
	2. Establish an initial USB PD explicit contract,		N/A
	3. If desired, use PR_Swap to establish the preferred power role, and		N/A
	4. Use DR_Swap to establish data role to be consistent with the port's position in the USB tree if needed.		N/A
<b>5.5.2</b>	<b>USB4 Hub UFP and Host Capabilities Discovery</b>		N/A
	The USB4 hub DFPs capabilities are ultimately based on the capabilities seen at its UFP (once it has established a connection to the host). If the USB4 hub's UFP is connected to an upstream USB4 hub, then the capabilities over the connection between the two hubs may not initially represent the capabilities all the way back to the host.		N/A
	The following summarizes the general principles regarding how UFP and host capabilities impact DFP connections.		N/A
	The downstream connection to a device or hub that is attached to the USB4 hub's DFP is based on the capabilities of the hub.		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
	Once the USB4 hub's UFP has established a connection, the hub's capabilities are limited to the capabilities of that UFP connection.		N/A
	When the USB4 hub's UFP connection indicates that a host is not present, once the hub is notified that a host becomes present, the hub will limit its capabilities as needed to match those of the host.		N/A
	Any connections on the USB4 hub's DFPs that existed prior to the host being present are adjusted to align with changes in capabilities if needed.		N/A
	Once a host becomes present in a USB4 tree, all intermediary hubs will update their connections to align with the host capabilities as the host present status is propagated to the downstream connected USB4 hubs.		N/A
	The capabilities seen by the hub's UFP are based on one of the following:		N/A
	An USB PD Enter_USB message is received which indicates the USB operation (USB4, USB 3.2 or USB 2.0) and associated characteristics supported (USB4 PCiesupported, USB4 DP supported, etc.) by the upstream port partner.		N/A
	An USB PD Enter Mode command is received to start a supported Alternate Mode (Thunderbolt 3, DisplayPort).		N/A
	No USB PD Enter_USB message is received within the tUSB4Timeout or USB PD Enter Mode message is received within the tAMETimeout indicating only USB 3.2 and USB 2.0 are available.		N/A
	If the USB4 hub's UFP is connected to an upstream USB4 hub, then the capabilities reported in the received USB PD Enter_USB message shall only be considered the host's capabilities if the Host Present bit is set. If the Host Present bit is reset, then the hub shall wait for a subsequent USB PD Enter_USB message to be received with the Host Present bit set. Once the Host Present bit is set, the capabilities as represented in the USB PD Enter_USB message can be used as the host's capabilities for the purpose of establishing final DFP connections.		N/A
	If the USB4 hub's UFP receives an USB PD Enter_USB message which indicates the USB operation as either USB 3.2 or USB 2.0, the USB4 hub shall not wait for the completion of the tUSB4Timeout before proceeding to establish its UFP and DFP connections following USB 3.2 or USB 2.0 hub requirements, respectively.		N/A
<b>5.5.3</b>	<b>Hub DFP Connection Requirements</b>		N/A
5.5.3.1	Speculative Connections		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
	When a device is attached to the DFP of a USB4 hub prior to the hub's UFP being connected and the host capabilities are known, the hub will speculatively connect to the attached device based on the following requirements.		N/A
	Use USB PD Discover ID and the USB PD Alternate Mode process to determine the full capabilities of the attached cable and device.		N/A
	Based on the discovered capabilities, establish the most capable connection based on the capabilities of the USB4 hub's DFP in the following priority order:		N/A
	1. USB4		N/A
	2. Thunderbolt 3 Alt Mode		N/A
	3. DP Alt Mode		N/A
	4. USB 3.2		N/A
	5. USB 2.0		N/A
	Inhibit port status notifications and data paths upstream from the USB4 hub's DFPs while waiting for the USB4 hub's UFP connection to be established.		N/A
5.5.3.2	Operational Connections		N/A
	Once the USB4 hub's UFP connection is established and the host capabilities are determined (see Section 5.5.2), the hub shall evaluate each existing DFP connection based on the capabilities associated with the hub's UFP connection and perform one of the following actions.		N/A
	If the DFP connection properly aligns with the capabilities of the UFP connection, enable the status notifications and data path for that port.		N/A
	If the DFP connection does not properly align with the capabilities of the UFP connection, the DFP connection shall do one of the following:		N/A
	If the UFP remains in USB4 and the DFP connection is with a downstream USB4 hub, send a revised USB PD Enter_USB message with the Host Present bit set.		N/A
	If the UFP changed to USB 3.2 or USB 2.0 and the DFP connection is with a downstream USB4 hub, the DFP shall be reset the connection using USB PD Data_Reset followed by sending a revised USB PD Enter_USB message indicating USB 3.2 or USB 2.0 and the Host Present bit set.		N/A
	Otherwise, the DFP shall enter the ErrorRecovery state to reset the connection and establish a new connection that aligns with the hub's UFP capabilities.		N/A
5.5.4	<b>Hub Ports Connection Behavior Flow Examples</b>		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	This section illustrates several example connection flows that assume that the hub's DFP connection is established prior to the hub's UFP connection. In these cases, the host capabilities are unknown at the time that the hub's DFP is connecting with the attached device. Given this, the initial connection established by the hub's DFP is speculatively based only on the hub and device's capabilities and may have to be revised once the host capabilities are known if there is a functional mismatch. When the hub's UFP connection is fully established prior to devices appearing on the hub's DFP, the connection can be established with full knowledge of the host's capabilities – flows associated with this relationship are not illustrated.		N/A
	For the example flows in this section, the Source/Sink power roles remain as initially resolved by the CC connection state machine with no PR Swap or DR Swap activity.		N/A
	All these example flows intend to minimize the total connection time for enabling the functionality of the device connected to the hub's DFP. This is accomplished by establishing the highest functional connection based on mutual capabilities between the hub and the device even as the hub's UFP capabilities are unknown or not ready for operation. If the speculatively established connection turns out to be valid once the hub's UFP capabilities are established, then the DFP's connection will be enabled as is. If the speculatively established connection turns out to be invalid, the DFP connection will be reset and a connection that aligns with the hub's UFP capabilities shall be established.		N/A
	Figure 5-2 Illustrates a connection flow aligned across the combination of a USB4 host, hub and device. The expected result is the successful enabling of end-to-end USB4 operation.		N/A
	In the illustrated flow, Cap Discovery includes all USB PD message exchanges needed between the DFP and its UFP port partner to discover the UFP's USB capabilities along with TBT3-compatibility and DP Alt Mode capabilities. For the USB4 hub's DFP, Cap Discovery is done on a speculative basis whenever it does not already know of the capabilities of the host that will eventually be connected via the hub's UFP.		N/A
	Upon completion of Cap Discovery between the hub's DFP and its UFP port partner, the hub DFP will establish the highest functional connection and then wait for the hub UFP to		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	complete its connection. Once the hub's UFP connection is established, the host capabilities available is used to determine what should be done to complete the hub DFP connection to the UFP port partner.		
	Host Cap is based on the resulting configuration (e.g. data bus protocol and speed) of the USB4 Hub's UFP and the Host capabilities information received in the USB PD Enter_USB Message from its DFP port partner (see Section 5.5.2). The USB4 hub uses Host Cap to set the available capabilities of the hub's DFPs.		N/A
	Figure 5-3 illustrates a connection flow aligned across the combination of a USB 3.2 host, a USB4 hub and a USB4 device.		N/A
	In the flow above, once connected to a USB 3.2 host, the Host Cap reflects that the hub can only support USB 3.2 on its DFPs and the speculatively established USB4 connection on the DFP is exited with the USB4 hub now operating as a traditional USB 3.2 hub.		N/A
	Figure 5-4 illustrates a connection flow aligned across the combination of a USB4 hub with a USB4 host and USB 3.2 device.		N/A
	While USB 3.2 devices won't necessarily respond to the Discover ID (SOP), the USB4 hub's DFP will attempt to discover the capabilities of the attached device.		N/A
	In the flow above, after the USB4 connection of the hub's UFP is established, the DFP connection remains valid with the USB 3.2 data path of the DFP being serviced by the USB4 Enhanced SuperSpeed tunnel.		N/A
	Figure 5-5 illustrates a connection flow aligned across the combination of a USB4 hub with a USB 3.2 host and device.		N/A
	While USB 3.2 devices won't necessarily respond to the Discover ID (SOP), the USB4 hub's DFP will attempt to discover the capabilities of the attached device.		N/A
	In the flow above, after the USB 3.2 connection of the hub's UFP is established, the DFP connection remains valid with the USB4 hub now operating as a traditional USB 3.2 hub.		N/A
	Figure 5-6 illustrates a connection flow aligned across the combination of a USB4 host, USB4 hub and a DP Alt Mode device (operating in Multi-function mode). In this case, the expected result is the enabling of the DP Alt Mode as bridged from USB4 DisplayPort tunneling.		N/A
	In the flow above, after the USB4 connection of the hub's UFP is established, the DFP connection remains valid with the DisplayPort and USB 3.2 data paths of the DFP being serviced by the USB4 DisplayPort and		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	Enhanced SuperSpeed tunnels.		
	Figure 5-7 illustrates a connection flow aligned across the combination of a USB 3.2 host, a USB4 hub and a DP Alt Mode device (operating in Multi-function mode). The expected result in this case is that the DP Alt Mode will not be enabled and a Billboard exposed by the device since the host doesn't support USB4.		N/A
	In the flow above, after the USB 3.2 connection of the hub's UFP is established, the DFP connection is no longer valid with the USB4 hub now operating as a traditional USB 3.2 hub. The hub's DFP would then reset the port which will lead to a USB 2.0 connection and the exposure of the Billboard device.		N/A
<b>5.5.5</b>	<b>Connecting to Downstream USB4 Hubs</b>		N/A
	When a USB4 hub is attached on its DFP to the UFP of another USB4 hub, the USB4 hub shall use the Host Present bit of the USB PD Enter_USB message to inform the downstream hub if the USB4 capabilities listed in the message reflects the host's capabilities or not. If an initial connection is made with the downstream hub with the Host Present bit reset in the USB PD Enter_USB message, the USB4 hub shall subsequently send a revised USB PD Enter_USB message with the Host Present bit set after its UFP has been fully established (see Section 5.5.2).		N/A
<b>5.5.6</b>	<b>Fallback Functional Requirements for USB4 Hubs</b>		N/A
	When a USB4 hub is attached on its UFP to a non-USB4 DFP, the USB4 hub shall seamlessly fall back to functioning as and meeting the requirements for a USB 3.2 hub.		N/A
<b>5.6</b>	<b>USB4 Device Connection Requirements</b>		N/A
<b>5.6.1</b>	<b>Fallback Mapping of USB4 Peripheral Functions to USB Device Class Types</b>		N/A
	USB4 peripheral devices provide functions based on data transferred over one or more of the protocol tunnels of USB4: Enhanced SuperSpeed USB, DisplayPort and PCI Express. For all peripheral functions that use the Enhanced SuperSpeed USB protocol tunnel, the mapping of those functions to USB device class specifications is clear but for those based on the other tunneled protocols, this mapping doesn't apply since those functions don't rely on USB device class drivers to operate.		N/A
	Each function of a USB4 device shall be mapped to an equivalent USB device class when possible. USB4 devices that contain mapped USB device class functions shall		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	support operation at USB 3.2 or USB 2.0 when connected to non-USB4 hosts. This requirement is exempted for those functions that rely on DisplayPort or PCIe tunnels for USB4 data transfer that don't reasonably map to an existing USB device class, e.g. a PCIe graphics adapter.		
	The performance of the function when mapped to a lower speed connection is expected to scale appropriately while still providing the functional equivalent of the primary capabilities of the peripheral function.		N/A
	Table 5-2 lists USB Device Class types and the mapping requirements for USB4 device peripheral functions as it relates to fallback when operating over USB 3.2 or USB 2.0.		N/A
	For all USB4 peripheral functions based on DisplayPort and PCIe protocol tunneling that do not map to USB device class equivalents when operating over USB 3.2 or USB 2.0, an appropriate USB Billboard Device Class shall be exposed to enable user notifications by the operating system of the host platform.		N/A
<b>5.7</b>	<b>Parameter Values</b>		N/A
<b>5.7.1</b>	<b>Timing Parameters</b>		N/A
	Table 5-3 provides the timeout requirement for a device that supports USB4 to enable a USB Billboard Device Class interface when the device cannot connect as a USB4 device during the discovery and entry process (Section 5.4).		N/A
<b>6</b>	<b>Active Cables</b>		N/A
	Active cables shall minimally support USB 3.2 Gen 2x2. USB4 active cables shall support all USB 3.2 rates and USB4. Active cables shall support USB PD eMarkers and may support Alternate Modes and advertise them as defined in Section 6.6.5.		N/A
	All USB4™ active cables shall be interoperable with Thunderbolt™ 3 as defined in the USB4 Specification (Chapter 13) and this specification (Section 6.7 and Appendices E and F).		N/A
	Short active cables supporting lengths up to 5 meters shall work in both directions and orientations and should function like passive cables from the user's perspective.		N/A
	Optically Isolated Active Cables (OIACs) support longer lengths up to 50 meters and provide electrical isolation between the two ends of the cable. OIACs are targeted for Industrial, Machine Vision, Remote Sensor, Pro Video, and Medical applications. OIACs do not 'just work' unlike short active cables. Long		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
	OIACs may not function correctly with Hosts, Devices, and Hubs that are not compliant to the USB 3.2 Specification. Table 6-1 shows the limitations of OIACs with short active cables. Legacy USB3 devices may require using an adapter between the device and the OIAC. This adapter is defined in Section 6.6.4.3.1.		
	Since no power runs through an OIAC, they can only be used to connect a Source DRD to a Source DRD or a Source DRD to a DFP. USB PD Revision 3 must be supported on both port partners for an OIAC to function. Each cable plug of an OIAC is locally powered from VCONN and/or optionally from VBUS. OIACs shall function for USB 3.2 when VCONN only is provided and may optionally use VBUS if provided. OIACs may require VBUS for Alternate Mode support. OIACs have no functionality when either cable plug is connected to a Sink/UFP only device (Sink/UFP devices are unable to provide power to the cable plug). OIACs require at least one end of the cable plug to be connected to a DRD (DRP and capable of accepting a DR_Swap to USB Device Role).		N/A
	If a connection to a USB 2.0 Device is required at the end of an OIAC, an adapter with a USB 3.2 to USB 2.0 transaction translator and VBUS/VCONN Source may be connected at the Device side of the cable to convert the USB 3.2 signals to USB 2.0 and provide power to the USB 2.0 Device and the OIAC.		N/A
	If an OIAC supports Alternate Modes that require the use of SBUs, the SBUs shall be optically isolated.		N/A
	All active cables, regardless of length, shall be compliant with this specification, the USB 3.2 including Appendix E, and the USB 3.2 Active Cable CTS.		N/A
<b>6.1</b>	<b>USB Type-C State Machine</b>		N/A
	OIAC cable plugs behave as Sinks on an initial cable connection. OIACs use USB PD Revision 3 to configure one plug as the DFP and one as the UFP as described in Section 6.2.1.		N/A
<b>6.2</b>	<b>USB PD Requirements</b>		N/A
	This specification uses the USB Type-C® terminology for connection states and not the USB PD specification terminology.		N/A
	The temperature sensor shall be co-located with the repeater for accurate thermal reporting.		N/A
	An active cable that contains two repeaters shall support both SOP' and SOP".		N/A
	An active cable that only contains one repeater internal to the active cable (not in the cable plugs) shall implement SOP' and is not required		N/A



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	to implement SOP".		
<b>6.2.1</b>	<b>Active Cable USB PD Requirements</b>		N/A
	Active cables shall support USB PD Revision 3, Version 1.2 or later. Active cables shall support USB PD Structured VDMs.		N/A
6.2.1.1	SOP' and SOP" Requirements		N/A
	Active cables shall respond to Discover_Identity and Get_Status on SOP'. When the SOP" Controller Present bit is set in the Active Cable VDO, they shall respond Get_Status on SOP" as well.		N/A
	OIACs have a different definition for SOP". SOP" is always the far-end cable plug relative to the message initiator.		N/A
6.2.1.2	Discovering Cable Characteristics		N/A
	The USB PD Discover_Identity Command is used to discover the characteristics of the active cable. This command shall only be sent to SOP'. All active cables shall respond to the Discover_Identity Command with Active Cable VDOs that returns information about the cable. Note the active cable shall respond using either USB PD Revision 2 or USB PD Revision 3 following the USB PD Interoperability rules.		N/A
6.2.1.3	Cable Status		N/A
	The USB PD Get_Status Command is used to discover the current state of the active cable. Cable status shall be reported on SOP' and shall also be reported on SOP" when the SOP" Controller Presence bit is set in the Active Cable VDO.		N/A
<b>6.2.2</b>	<b>USB PD Messages for OIAC</b>		N/A
	The following sections outline the USB PD Messages for an OIAC.		N/A
6.2.2.1	USB PD Message Handling on Initial Connection		N/A
	The OIAC shall not forward USB PD messages until after determining the DFP to UFP Connection in the Active State and the Active Cable is configured (Phase 3 complete). The OIAC shall process USB PD messages locally in the USB Type-C plug as defined in Table 6-4 on an initial connection before the disconnect/reconnect and data role establishment.		N/A
6.2.2.2	USB PD Message Handling in the Active State		N/A
	There are some USB PD SOP and SOP" messages that invalid in an OIAC, therefore the next two sections explicitly define all USB PD messages that do not traverse the cable either because the message is targeted to SOP' or are invalid and all USB PD messages that do traverse the cable to SOP" and SOP.		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
6.2.2.2.1	USB PD Messages Which Do Not Traverse the Cable in the Active State		N/A
	The USB PD messages which do not traverse the OIAC when Active are defined in Table 6-5. Section 6.2.2.2.2 describes the messages which traverse the OIAC in Active.		N/A
6.2.2.2.2	USB PD Messages Which Do Traverse the Cable in the Active State		N/A
	All USB PD SOP messages defined in Table 6-6 are forwarded across the cable on SOP. The messages are sent by the Initiator, forwarded optically through the cable, and then driven on CC from the far side cable plug to the Receiver.		N/A
	The timing of the message forwarding is defined in Table 6-7. The GoodCRC is generated locally to the cable plug and returned within tTransmit on a valid Message. The OIAC shall be able to handle messages received with a minimum spacing of tInterFrameGap.		N/A
	The message Initiator expects a response within tSenderResponse and will perform error recovery if no response is received within this time unless the message is a Firmware_Update_Request/Response or a Security_Request/Response. The message Receiver responds within tReceiverResponse unless there is an error. The OIAC shall decide to respond locally or forward the message, send the message across the fiber, and drive the message on the far side plug CC pin within tForward as shown in Figure 6-4 unless the message is Firmware_Update_Request/Response or a Security_Request/Response. The USB PD handler shall forward the messages addressed to SOP defined in Table 6-5. The USB PD Handler shall only forward to the far-end plug any message addressed to SOP" which are defined below:		N/A
	Firmware_Update_Request, Firmware_Update_Response		N/A
	Security_Request, Security_Response		N/A
	Status		N/A
	Enter Mode, Exit Mode, Attention (if the Alternate Modes are supported by the OIAC)		N/A
	The OIAC shall not forward USB PD messages until it completes Phase 3. The cable plug shall send no response if a GoodCRC is not received from the Responder.		N/A
	Some implementations may implement local copies of the SOP" information on the local cable plug and use an internal mechanism to send/receive responses.		N/A
6.2.2.3	USB PD Reset Handling		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	The OIAC shall:		N/A
	1. Detect the Hard Reset ordered set		N/A
	2. Forward it to the remote plug and remote port		N/A
	3. Reset its state machine		N/A
	A Hard Reset signal can occur at any time during normal operation of the cable and also during the cable initialization. This signal will take precedent over the initialization state machine and immediately forward the Hard Reset Message to the remote plug, using an internal cable message.		N/A
6.2.2.4	Internal Cable Messages		N/A
	All SOP" and SOP messages shall be forwarded or terminated as defined in Section 6.2.2 and will not be further described in this section.		N/A
	The messages defined in this section provide informative guidance on internal messages for OIACs. The actual definition and implementation of each message is left to the implementer.		N/A
	In this section and Section 6.3, there is a defined Plug-A and Plug-B to support USB PD communication through the OIAC cable. These designations are established at the time of manufacture and are completely internal to the cable. They are used to simplify the cable initialization and internal messaging.		N/A
6.2.2.4.1	MSG_Keep_Alive		N/A
	A low duty cycle message that is meant to inform the remote cable plug that the local cable plug is still operational.		N/A
	A simple example is that only Plug-A will send MSG_Keep_Alive and Plug-B must respond with MSG_Keep_Alive_ACK. Each end will have its own timeout for MSG_Keep_Alive and MSG_Keep_Alive_ACK.		N/A
6.2.2.4.2	MSG_Keep_Alive_ACK		N/A
	Acknowledgement message to the MSG_Keep_Alive.		N/A
	A simple example is that only Plug-A will send MSG_Keep_Alive and Plug-B must respond with MSG_Keep_Alive_ACK. Each end will have its own timeout for MSG_Keep_Alive and MSG_Keep_Alive_ACK.		N/A
6.2.2.4.3	MSG_Port_Capabilities		N/A
	This message contains all relevant local port capabilities including but not limited to:		N/A
	Chunked/Unchunked capability		N/A
	DRD/DFP/UFP capabilities		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
6.2.2.4.4	MSG_Cable_Config		N/A
	This message contains the final cable configuration based on known system capabilities.		N/A
	It will contain both relevant ports' capabilities and the final DFP/UFP roles for the system.		N/A
	This message will also serve as the signal in Phase 2 for the cable plug to start the reboot process.		N/A
6.2.2.4.5	MSG_Release_Remote_SourceCap_GoodCRC		N/A
	This is a synchronization message to attempt to bring up both ports at the same time.		N/A
	It is used in Phase 3 and is the signal to release the GoodCRC message to the Source Capabilities message from the attached port. At the beginning of Phase 3, after each plug has been rebooted, and depending on the final DFP/UFP role, each plug should wait for MSG_Release_Remote_SourceCap_GoodCRC before it is allowed to release a GoodCRC in response to a Source_Capabilities message from the port.		N/A
6.2.2.4.6	MSG_DR_Swap_Init		N/A
	Initial DR_Swap sent by Plug-A to Plug-B to perform a DR_Swap.		N/A
6.2.2.4.7	MSG_DR_Swap_Reject		N/A
	Plug-B sends this message to report that the initial DR_Swap was rejected by its attached port.		N/A
	This is needed by Plug-A to attempt to re-configure the cable such that the port associated to Plug-B can remain a DFP. This is part of the DR_Swap test in Phase 1, shown in the state diagram transition from M3 to M4 (or M3 to M5). It is also possible that this may be needed in Phase 3, if the port associated with Plug-B rejects the DR_Swap.		N/A
6.2.2.4.8	MSG_DR_Swap_Accept		N/A
	Plug-B sends this message to report that the initial DR_Swap was accepted by its attached port.		N/A
	This is needed by Plug-A to continue (M3--M6 transition) in Phase 1 in the cable initialization.		N/A
6.2.2.4.9	MSG_Force_Detach		N/A
	This message is to request the remote plug to disconnect from its attached port. The disconnect method can be done by raising the voltage on the CC line to above vRd-Connect or removing Rd.		N/A
	This will cause the remote port to remove VCONN from the remote plug all the circuitry should be powered down, therefore resetting		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	any action taken by the plug on the CC line to cause the disconnect.		
6.2.2.4.10	MSG_Hard_Reset		N/A
	This message is to forward a Hard_Reset signal to the remote plug and port.		N/A
	An internal Hard Reset message should be responded to with an Acknowledgement.		N/A
6.2.2.4.11	MSG_Acknowledgement		N/A
	This message is to acknowledge that a message was received.		N/A
	This message has been explicitly defined in a few specific cases but can be used more broadly.		N/A
6.2.2.5	Data Role Swap in Active State		N/A
	OIACs shall support Data Role Swaps on SOP. Each OIAC plug discovers its plug port partner and determines if it is capable of a Data Role Swap during the initialization process described in Section 6.3. OIAC cable plugs generate internal messages to communicate the DR_Swap, Accept, Reject, and Wait to the far side of the cable.		N/A
6.2.3	Short Active Cable Behaviors in Response to Power Delivery Events		N/A
	Each cable plug of the short active cable shall be capable of communicating on SOP' and SOP'' if reported in the Discover_Identity Command.		N/A
6.2.3.1	Data Role Swap		N/A
	Short active cables are transparent to the USB PD Data Role swap.		N/A
6.2.3.2	Power Role Swap		N/A
	Short active cables shall maintain USB 3.2 signaling during a USB PD Power Role swap. The source of VCONN is not affected by a Power Role Swap.		N/A
6.2.3.3	VCONN Swap		N/A
	Short active cables shall maintain USB 3.2 signaling during a USB PD VCONN swap. During a VCONN Swap, the original VCONN Source continues to supply VCONN for some time after the new VCONN Source begins to supply VCONN. This ensures that VCONN is never dropped.		N/A
6.2.3.4	Fast Role Swap		N/A
	Short active cables will drop USB 3.2 signaling as a side-effect of a Fast Role Swap if VCONN is not maintained during the Fast Role Swap.		N/A
6.3	<b>OIAC Connection Flow and State Diagrams</b>		N/A
	This section defines the connection state diagrams for the OIAC.		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
	OIAC plug defined at time of manufacture as either Plug-A or Plug-B for USB PD communication. This in no way indicates the plug has more or less capability, rather it allows for a consistent behavior when making the initial end to end connection.		N/A
	The OIAC communicates using USB PD with its plug partners to determine the partner capabilities. The OIAC performs a series of connect/disconnects to establish the correct UFP/DFP data role for the cable plug. The possible combinations for ports and cable plugs is defined in Table 6-9.		N/A
	The connection and establishment of data roles is performed in three phases.		N/A
<b>6.3.1</b>	<b>OIAC Connection Flow - Discovery - Phase 1</b>		N/A
	The OIAC cable plugs discover the capabilities of their port partners in the Discovery Phase.		N/A
<b>6.3.2</b>	<b>OIAC Connection Flow - Reboot - Phase 2</b>		N/A
	The OIAC cable plugs forward the capabilities of their plug partners and perform disconnect/reconnect.		N/A
	Plug-A will always start with repeatedly sending "MSG_Cable_Config" to Plug-B to start reboot.		N/A
	Plug-B Reboots.		N/A
	Plug-B sees "MSG_Cable_Config" and holds off on SourceCap GoodCRC until it is allowed to release it.		N/A
	Plug-B sends "MSG_Cable_Config" to the Plug-A.		N/A
	Plug-A Reboots.		N/A
	Plug-A sees "MSG_Cable_Config" and holds off on SourceCap GoodCRC until it is allowed to release it.		N/A
<b>6.3.3</b>	<b>OIAC Connection Flow -Configuration-Phase 3</b>		N/A
	The OIAC Plug-A determines DFP/UFP roles for Plug-A and Plug-B. Plug-A releases the PLUG to be configured as the DFP and initiates a DR_Swap. The side that issues the DR_Swap send a DR_Swap and releases the other side SourceCap GoodCRC.		N/A
<b>6.3.4</b>	<b>OIAC Connection State Diagram Plug-A</b>		N/A
	The following sections details a possible OIAC state diagram for Plug-A.		N/A
6.3.4.1	Detached State (M0)		N/A
	The plug is in Detached (M0) when no power is applied. The plug transitions to Remote Handshake (M1) when VCONN is applied.		N/A
6.3.4.2	Remote Handshake State (M1)		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
	The plug is waiting for the "Timeout" timer expiration or a "MSG_Cable_Config" message from Plug-B.		N/A
	The Timeout time is dependent on the duty cycle of Plug-B's Repeat Port Capabilities messages and the maximum cable latency.		N/A
	The plug starts in the USB 3.2 RTSSM eSS.Disabled and remains in eSS.Disabled until cable initialization is complete at the end of Phase 3.		N/A
6.3.4.2.1	Entry to Remote Handshake		N/A
	The plug enters Attached.SNK followed by entry to Remote Handshake (M1).		N/A
6.3.4.2.2	Exit from Remote Handshake		N/A
	The plug transitions to:		N/A
	Plug-A Initial PD Contract (M2) when the "Timeout" timer has expired,		N/A
	Active USB PD Contract 1 (M8) upon receipt of a "MSG_Cable_Config" message when Plug-A resolves to a DFP and Plug-B will resolve to a UFP, or		N/A
	Release Remote Source_Cap GoodCRC 1 (M10) upon receipt of a "MSG_Cable_Config" message when Plug-A resolves to a UFP and Plug-B will resolve to a DFP.		N/A
6.3.4.3	Plug-A Initial PD Contract State (M2)		N/A
	When the plug is in Plug-A Initial PD Contract, the plug has established an initial USB PD contract and evaluated its local port's DRD capability.		N/A
6.3.4.3.1	Entry to Plug-A Initial DP Contract		N/A
	On Entry to Plug-A Initial PD Contract, the plug shall:		N/A
	1. Send a GoodCRC in response to a Source Capabilities message from the local attached port		N/A
	2. Evaluate the local attached port's DRD capability (as indicated in the Source Capabilities message)		N/A
	3. Respond to the Source Capabilities message with the "default" RDO specified in Table 6-11.		N/A
6.3.4.3.2	Exit from Plug-A Initial DP Contract		N/A
	The OIAC plug shall transition to:		N/A
	Local DR Swap Test (M3) upon receipt of a MSG_Port_Capabilities where the Plug-A port is a DRD and the Plug-B port is either a DRD or DFP,		N/A
	Remote DR Swap Test (M4) upon receipt of a MSG_Port_Capabilities where the Plug-A port is a DFP and the Plug-B port is DRD, or		N/A
	Error – USB2 Billboard (M5) upon determination both Plug-A and Plug-B are		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	connected to DFPs.		
6.3.4.4	Local DR Swap Test State (M3)		N/A
	The Local DR Swap Test is a test to ensure that the Plug-A port that is defined as a DRD will accept a DR_Swap request.		N/A
6.3.4.4.1	Entry to Local DR Swap Test		N/A
	On entry to Local DR Swap Test, the plug shall issue DR_Swap request to its local port.		N/A
	If the local port responds to the DR Swap with "Wait," then the plug shall follow the tDRSwapWait timer and retry up to 3 times, after which it will error out and transition to state Error – USB2 Billboard (M5).		N/A
6.3.4.4.2	Exit from Local DR Swap Test		N/A
	The OIAC plug shall transition to:		N/A
	Remote DR Swap Test (M4) upon receipt of a Reject and the Plug-B port reported that it is a DRD,		N/A
	Error – USB2 Billboard (M5) upon receipt of a Reject and the Plug-B port reported that it is a DFP, or		N/A
	Reboot Sequence (M6) upon receipt of an Accept.		N/A
6.3.4.5	Remote DR Swap Test State (M4)		N/A
	The Remote DR Swap Test is a test to ensure that the Plug-B port that is defined as a DRD will accept a DR_Swap request.		N/A
6.3.4.5.1	Entry to Remote DR Swap Test		N/A
	On entry to Remote DR Swap Test, the plug shall issue a DR_Swap_Init to the remote plug.		N/A
6.3.4.5.2	Exit from Remote DR Swap Test		N/A
	The OIAC plug shall transition to:		N/A
	Reboot Sequence (M6) upon receipt of a MSG_DR_Swap_Accept, or		N/A
	Error – USB2 Billboard (M5) upon receipt of a MSG_DR_Swap_Reject.		N/A
6.3.4.6	Error --USB2 Billboard (M5)		N/A
	The plug presents a Billboard indicating an Invalid Configuration is present. For example: "Error: A DFP only device connected to one of the plugs."		N/A
6.3.4.6.1	Entry to Error --USB2 Billboard		N/A
	On entry Error – USB2 Billboard, the plug shall issue present a Billboard message over USB 2.0 and then power down to its lowest possible state.		N/A
6.3.4.6.2	Exit from Error - USB2 Billboard		N/A
	The only means of exiting this Error state, is either from a Reset that disconnects VCONN power or a disconnect event which also		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	disconnects VCONN power.		
6.3.4.7	Reboot Sequence State (M6)		N/A
	When the plug is in the Reboot Sequence, it will disable the High Speed Data path and start to initiate a remote plug reboot.		N/A
6.3.4.7.1	Entry to Reboot Sequence		N/A
	On entry to Reboot Sequence, the plug shall:		N/A
	1) Disable the HS path by changing the SS RX termination to High-Z.		N/A
	2) Determine and store the final System Configuration for this link.		N/A
	a. The System Configuration will contain:		N/A
	i. Host/Device Port information		N/A
	ii. Final Plug-A/Plug-B roles		N/A
	1. If coming from State M3		N/A
	a. Plug-A—DFP (DR_Swap)		N/A
	b. Plug-B—UFP		N/A
	2. If coming from State M4		N/A
	a. Plug-A—UFP		N/A
	b. Plug-B—DFP (DR_Swap)		N/A
	3. If coming from State M9		N/A
	a. Plug-A—UFP		N/A
	b. Plug-B—DFP (DR_Swap)		N/A
	3) Continuously send "MSG_Cable_Config" message to the remote plug.		N/A
6.3.4.7.2	Exit from Reboot Sequence		N/A
	The OIAC plug shall transition to the Force Detach (M7) when a "MSG_Cable_Config" message is received that matches the final configuration that Plug-A sent to Plug-B.		N/A
6.3.4.8	Force Detach State (M7)		N/A
	The plug shall transition to SRC.Open on both CC and VCONN and maintain this state for at least tSRCDisconnect.		N/A
6.3.4.8.1	Entry to Force Detach		N/A
	On entry to Force Detach, the plug shall raise the voltage on the CC-wire above vRd-Connect.		N/A
6.3.4.8.2	Exit from Force Detach		N/A
	The plug transitions to Detached upon exit from Force Detach.		N/A
6.3.4.9	Active USB PD Contract 1 State (M8)		N/A
	Active USB Contract 1 is where OIAC Plug-A creates at USB PD contract with the local port.		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
6.3.4.9.1	Entry to Active USB PD Contract 1		N/A
	The OIAC plug shall follow the steps listed below:		N/A
	1. Begin responding to USB PD messages from its port partner with GoodCRCs.		N/A
	2. Evaluate Fixed 5V PDO in the Source Capabilities message to check if its port partner is a DRD.		N/A
	3. Request for a 5 V @ 0 A power contract.		N/A
	4. May remove Ra to save power.		N/A
6.3.4.9.2	Exit from Active USB PD Contract 1		N/A
	The plug transitions to the DR Swap (M9) when it receives an Accept followed by a PS_RDY message from its port partner.		N/A
6.3.4.10	DR Swap State (M9)		N/A
	The DR Swap is used to set the final data role of the OIAC's Plug-A and signal to the OIAC Plug-B to complete its configuration.		N/A
6.3.4.10.1	Entry to DR Swap		N/A
	The OIAC plug shall issue a DR_Swap to its port partner.		N/A
	If the local port responds to the DR_Swap with "Wait," then the plug shall follow the tDRSwapWait timer and retry up to 3 times, after which it will error out and transition to state Error – USB2 Billboard (M5).		N/A
6.3.4.10.2	Exit from DR Swap		N/A
	If the DR_Swap message is responded to with:		N/A
	An Accept, it shall transition to the Release Remote Source_Cap GoodCRC 2 State (M12), or		N/A
	A Reject it shall transition to the Error - USB2 Billboard + Complete Reset (M13).		N/A
6.3.4.11	Release Remote Source_Cap GoodCRC 1 State (M10)		N/A
	The OIAC is waiting to for Release_Remote_Source_Cap_GoodCRC to better synchronize the power on of the two OIAC plug ends.		N/A
6.3.4.11.1	Entry to Release Remote Source_Cap GoodCRC 1		N/A
	The OIAC plug shall release the Remote SourceCap GoodCRC.		N/A
6.3.4.11.2	Exit from Release Remote Source_Cap GoodCRC 1		N/A
	The OIAC plug shall transition to:		N/A
	Active USB PD Contract 2 State (M11), when a "MSG_Release_Remote_SourceCap_GoodCRC" message is received, or		N/A
	Error – USB2 Billboard + Complete Reset (M13) upon receipt of a		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	MSG_DR_Swap_Reject.		
6.3.4.12	Active USB PD Contract 2 State (M11)		N/A
	Active USB Contract 2 is where OIAC Plug-A creates at USB PD contract with the local port and should end with viable link.		N/A
6.3.4.12.1	Entry to Active USB PD Contract 2		N/A
	The OIAC plug shall follow the steps listed below:		N/A
	1. Begin responding to USB PD messages from its port partner with GoodCRCs.		N/A
	2. Request a 5 V @ 0 A power contract.		N/A
	3. May remove Ra to save power.		N/A
6.3.4.12.2	Exit from Active USB PD Contract 2		N/A
	The plug shall transition to Final System Configuration Verification (M13) for final system verification.		N/A
6.3.4.13	Release Remote Source_Cap GoodCRC 2 State (M12)		N/A
	OIAC Source Plug configuration is completed and the USB 3.2 begins looking for a connection.		N/A
6.3.4.13.1	Entry to Release Remote Source_Cap GoodCRC 2		N/A
	The OIAC plug shall release the Remote SourceCap GoodCRC.		N/A
6.3.4.13.2	Exit from Release Remote Source_Cap GoodCRC 2		N/A
	The plug shall transition to Final System Configuration Verification (M13) for final system verification.		N/A
6.3.4.14	Error-USB2 Billboard + Complete Reset (M13)		N/A
	The plug presents a Billboard indicating an Invalid Configuration is present. For example: "Error: An invalid configuration occurred. Full link will be reset."		N/A
6.3.4.14.1	Entry to Error-USB2 Billboard + Complete Reset (M13)		N/A
	On entry Error – USB2 Billboard + Complete Reset, the plug shall:		N/A
	1) Present a USB2 Billboard message		N/A
	2) Send a MSG_Hard_Reset to the remote Plug		N/A
	3) Wait for Hard Reset Ack from Remote Plug (Unless entry is from an expired WatchDog Timer, in which case, go directly to M13-B)		N/A
	Received ACK (State M13-B):		N/A
	4) Send Hard Reset to the Local Port		N/A
	Did NOT receive ACK (State M13-C):		N/A
	5) Present USB2 Billboard Message: "Error: Internal Cable Communication Error. Unplug		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	both cable ends to reset.”		
6.3.4.14.2	Exit from Error-USB2 Billboard + Complete Reset (M13 B/C)		N/A
	The only means of exiting this Error state, is either from a Reset that disconnects VCONN power or a disconnect event which also disconnects VCONN power from each port.		N/A
6.3.4.14.3	WatchDog Timer Entry		N/A
	A watchdog timer should be implemented for internal cable messages that require a response. The watchdog timer will also provide an entry to an Error State (M13) if the far end plug is unresponsive for any reason.		N/A
	There are a few states where the watchdog timer shall NOT be implemented including but not limited to M2, where it is possible that only a single end of the OIAC is connected and M6, where the reboot sequence can take a few seconds.		N/A
6.3.4.15	Final System Configuration Verification (M14)		N/A
	Final System Configuration Verification is used to do one final check there were no unforeseen changes the local port and the final cable configuration defined by Plug-A.		N/A
6.3.4.15.1	Entry to Final System Configuration Verification		N/A
	The OIAC plug shall check all values in the MSG_Cable_Config match that of the current local port's configuration.		N/A
6.3.4.15.2	Exit from Final System Configuration Verification		N/A
	The plug shall transition to:		N/A
	Rx.Detect, and start far-end receiver termination detection and the USB 3.2 RTSSM State Machine after a successful match of the MSG_Cable_Config and the local port's configuration, or		N/A
	Error - USB2 Billboard + Complete RESET (State M14) after unsuccessful match of the MSG_Cable_Config and the local port's configuration.		N/A
<b>6.3.5</b>	<b>OIAC Connection State Diagram Plug-B</b>		N/A
	The following sections details a possible OIAC state diagram for Plug-B.		N/A
6.3.5.1	Detached State (S0)		N/A
	The plug is in Detached (S0) when no power is applied. The plug transitions to Remote Handshake (S1) when VCONN is applied.		N/A
6.3.5.2	Remote Handshake State (S1)		N/A
	The plug is waiting for the “Timeout” timer expiration or a “MSG_Cable_Config” message from Plug-A.		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
	The Timeout time is dependent on the duty cycle of the Plug-A's Repeat MSG_Cable_Config messages and the maximum cable latency.		N/A
6.3.5.2.1	Entry to Remote Handshake		N/A
	The plug enters Attached.SNK followed by entry to Remote Handshake (S1).		N/A
	The plug starts in the USB 3.2 RTSSM eSS.Disabled and remains in eSS.Disable until cable initialization is complete at the end of Phase 3.		N/A
6.3.5.2.2	Exit from Remote Handshake		N/A
	The plug transitions to:		N/A
	Plug-B Initial PD Contract (S2) when the "Timeout" timer has expired, or		N/A
	Send Repeated Cable Config (S5) upon receipt of a "MSG_Cable_Config" message.		N/A
6.3.5.3	Plug-B Initial DP Contract (S2)		N/A
	The plug takes the following actions in the order defined:		N/A
	1. Send a GoodCRC in response to a Source Capabilities message from the local attached port.		N/A
	2. Evaluate the local attached port's DRD Capability (as indicated in the Source Capabilities message).		N/A
	3. Send the initial RDO (5 V/0 A) and negotiate an explicit power contract.		N/A
	4. Send "MSG_Port_Capabilities" to Plug-A. The plug shall continue to send "MSG_Port_Capabilities" until it exits this state.		N/A
6.3.5.3.1	Entry to Plug-B Initial DP Contract		N/A
	The plug enters Plug-B Initial PD Contract (S2) upon "Timeout" timer expiration.		N/A
6.3.5.3.2	Exit from Plug-B Initial DP Contract		N/A
	The plug transitions to:		N/A
	DR Swap (S3) upon receipt of a "DR_Swap_Init" message from Plug-A, or		N/A
	Force Detach (S4) upon receipt of a "MSG_Cable_Config" message from Plug-A.		N/A
6.3.5.4	DR Swap (S3)		N/A
	The plug determines if a DR_Swap can be performed with the local attached port or Plug-A configured itself.		N/A
6.3.5.4.1	Entry to DR Swap		N/A
	Upon entry into DR Swap (S3) the plug shall:		N/A
	1. Send DR_Swap message to the local attached port.		N/A
	2. Send MSG_DR_Swap_Accept when the plug receives Accept message from the local		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	attached port.		
	3. Send MSG_DR_Swap_Reject when the plug receives Reject message from the local attached port.		N/A
	If the local port responds to the DR Swap with "Wait," then the plug shall follow the tDRSwapWait timer and retry up to 3 times, after which it will error out and transition to state Error – USB2 Billboard (S7).		N/A
6.3.5.4.2	Exit from DR Swap		N/A
	The plug shall transition to:		N/A
	Error – USB2 Billboard (S7) upon rejection of the local attached port DR Swap, or		N/A
	Force Detach (S4) upon receipt of a "MSG_Cable_Config" message from Plug-A.		N/A
6.3.5.5	Force Detach (S4)		N/A
	The plug shall transition to SRC.Open on both CC and VCONN and maintain this state for at least tSRCDisconnect.		N/A
6.3.5.5.1	Entry to Force Detach		N/A
	The plug enters Force Detach (S4) upon receipt of a "MSG_Cable_Config" message from Plug-A.		N/A
6.3.5.5.2	Exit from Force Detach		N/A
	The plug transitions to Detached (S0) upon exit from Force Detach.		N/A
6.3.5.6	Send Repeated Cable Config (S5)		N/A
	The plug repeatedly sends "MSG_Cable_Config" messages in this state to inform Plug-A of the configuration of the local attached port.		N/A
6.3.5.6.1	Entry to Send Repeated Cable Config		N/A
	The plug enters Repeated Cable Config (S5) upon receipt of a "MSG_Cable_Config" message from Plug-A.		N/A
6.3.5.6.2	Exit from Send Repeated Cable Config		N/A
	The plug transitions to Phase 3 PD Contract (S6) upon receipt of a "Release SourceCap GoodCRC" message from the Plug-A port.		N/A
6.3.5.7	Phase 3 PD Contract (S6)		N/A
	The plug performs the following actions in this state:		N/A
	1. Send a GoodCRC in response to a Source Capabilities message from the local attached port.		N/A
	2. Evaluate the attached local attached port's DRD Capability (as indicated in the Source Capabilities message).		N/A
	3. Send the initial RDO (5 V/0 A) in response to the Source Capabilities message and negotiate an explicit power contract.		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
6.3.5.7.1	Entry to Phase 3 PD Contract		N/A
	The plug enters Phase 3 PD Contract upon receipt of a "Release SourceCap GoodCRC" message from Plug-A.		N/A
6.3.5.7.2	Exit from Phase 3 PD Contract		N/A
	The plug transitions to:		N/A
	Final System Configuration Verification (S10) for final system verification upon determination Plug-A is acting as a DFP and it is acting as a UFP, or		N/A
	Phase 3 DR Swap (S8) upon determination Plug-A is acting as a UFP and it is acting as a DFP.		N/A
6.3.5.8	Error - USB2 Billboard (S7)		N/A
	The plug presents a Billboard indicating an Invalid Configuration is present. For example: "Error: A DFP only device connected to one of the plugs."		N/A
6.3.5.8.1	Entry to Error - USB2 Billboard		N/A
	The plug transitions to this state upon rejection of a DR_Swap by the local attached port.		N/A
6.3.5.8.2	Exit from Error - USB2 Billboard		N/A
	The only means of exiting this Error state, is either from a Reset that disconnects VCONN power or a disconnect event which also disconnects VCONN power.		N/A
6.3.5.9	Phase 3 DR Swap State (S8)		N/A
	The plug issues a DR_Swap with its local attached port in this state.		N/A
6.3.5.9.1	Entry to Phase 3 DR Swap		N/A
	The plug enters Phase 3 DR Swap upon determination Plug-A is connected as a UFP and Plug-B should connect as a DFP.		N/A
6.3.5.9.2	Exit from Phase 3 DR Swap		N/A
	The plug shall transition to:		N/A
	Final System Configuration Verification (S10) for final system verification after successful completion of the DR_Swap with the local attached port, or		N/A
	Error - USB2 Billboard (S7) after unsuccessful completion of the DR_Swap with the local attached port.		N/A
6.3.5.10	Error - USB2 Billboard + Complete RESET (S9)		N/A
	The plug presents a Billboard indicating an Invalid Configuration is present. For example: "Error: An invalid configuration occurred. Full link will be reset."		N/A
6.3.5.10.1	Entry to Error - USB2 Billboard + Complete RESET		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	On entry Error – USB2 Billboard + Complete RESET, the plug shall:		N/A
	1. Present a USB2 Billboard message.		N/A
	2. Send Hard_Reset to the Local Plug.		N/A
6.3.5.10.2	Exit from Error – USB2 Billboard + Complete RESET		N/A
	The only means of exiting this Error state, is either from a Reset that disconnects VCONN power or a disconnect event which also disconnects VCONN power.		N/A
6.3.5.10.3	WatchDog Timer Entry		N/A
	A watchdog timer should be implemented for internal cable messages that require a response. The watchdog timer will also provide an entry to an Error State (M13) if the far end plug is unresponsive for any reason.		N/A
	There are a few states where the watchdog timer shall NOT be implemented including but not limited to S5, where the reboot sequence can take a few seconds.		N/A
6.3.5.11	Final System Configuration Verification (S10)		N/A
	The Final System Configuration Verification is used to one final check there were no unforeseen changes the local port and the final cable configuration defined by Plug-A.		N/A
6.3.5.11.1	Entry to Final System Configuration Verification		N/A
	The OIAC plug shall check all values in the MSG_Cable_Config match that of the current local port's configuration.		N/A
6.3.5.11.2	Exit from Final System Configuration Verificati		N/A
	The plug shall transition to:		N/A
	Rx.Detect, and start far-end receiver termination detection and the USB 3.2 RTSSM State Machine after a successful match of the MSG_Cable_Config and the local port's configuration, or		N/A
	Error – USB2 Billboard + Complete RESET (State S9) after unsuccessful match of the MSG_Cable_Config and the local port's configuration.		N/A
<b>6.4</b>	<b>Active Cable Power Requirements</b>		N/A
<b>6.4.1</b>	<b>VBUS Requirements</b>		N/A
	Short active cables shall meet the limits of the IR Drop on VBUS and ground defined in Section 4.4.1.		N/A
	Short active cables shall provide VBUS and support at least 3 A and optionally 5 A current.		N/A
<b>6.4.2</b>	<b>OIAC VBUS Requirements</b>		N/A
	The OIAC cable plugs have two power contracts. The first contract is defined at first		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	connection of the cable. The second contract is after the data role establishment in the Active state.		
6.4.2.1	OIAC VBUS Requirements on Initial Connection		N/A
	The OIAC cable plugs shall negotiate a power contract with their plug partners as defined in this section on Initial Connection. The USB PD Sink Capabilities PDO presented by the OIAC cable plug (SOP) on Initial Connection is defined in Table 6-10. The Sink RDO (SOP) before data role establishment is defined in Table 6-11.		N/A
	The OIAC cable plug (SOP) shall wait tTypeCSinkWaitCap after VBUS is presented before issuing a Hard Reset to restart sending of the Source Capabilities.		N/A
<b>6.4.3</b>	<b>USB PD Rules in Active State</b>		N/A
	The OIAC cable plugs shall negotiate a power contract with their plug partners as defined in this section in the Active State. The OIAC shall follow the message applicability rules defined in Table 6-4 until entry to the Active State.		N/A
	The minimum USB PD Sink Capabilities PDO presented by the OIAC cable plug (SOP) is defined in Table 6-13. The OIAC may request additional Sink Capabilities (higher voltages and currents) for performance optimization. The minimum Sink RDO is provided as an example in Table 6-14. The OIAC shall function when receiving the minimum Source PDO.		N/A
	The OIAC cable plug (SOP) shall wait tTypeCSinkWaitCap after VBUS is presented before issuing a Hard Reset to restart sending of the Source Capabilities		N/A
<b>6.4.4</b>	<b>VCONN Requirements</b>		N/A
	Active Cables shall:		N/A
	Meet the VCONN sink requirement defined in Table 4-6, Table 6-20 and Table 6-30.		N/A
	Active cables shall meet the VCONN requirements specified in Section 4.9.		N/A
<b>6.5</b>	<b>Mechanical</b>		N/A
	All active cables shall meet the mechanical requirements defined in the Section 3.8.		N/A
<b>6.5.1</b>	<b>Thermal</b>		N/A
6.5.1.1	Thermal Shutdown		N/A
	All active cables shall implement a temperature sensor and place the USB 3.2 signals in the eSS.Disabled state when the plug skin temperature reaches the maximum defined in Table 6-15. Active cables shall indicate they are in thermal shutdown if queried via the USB PD Get_Status command.		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	OIACs shall billboard in shutdown. For example: "Error: The Optical Cable has experienced a thermal shutdown."		N/A
	The Thermal Shutdown is cleared by the following events:		N/A
	Disconnect		N/A
	USB PD Hard Reset		N/A
6.5.1.2	Maximum Skin Temperature		N/A
	Active cable plug's skin temperature shall not exceed a maximum operating temperature of 30 °C above the ambient temperature for a plastic/rubber housing and 15 °C for a metal housing in any operating mode.		N/A
6.5.1.3	Thermal Reporting		N/A
	Active cables shall implement reporting their maximum internal operating temperature in the USB PD Discover_ID Command. Active cables shall implement reporting their current internal operating temperature in the USB PD Get_Status Command on SOP' and SOP" when supported. Active cables shall update their reported Internal Temperature at least every 500 ms.		N/A
	The plug's Internal Temperature is reported in °C and shall be monotonic. It is not the plug's skin temperature, but cable manufacturers shall correlate the maximum internal operating temperature with the maximum plug skin temperature to ensure shutdown when the maximum plug skin temperature is reached.		N/A
	Sources and/or Sinks may take action to reduce VBUS current to reduce the cable plug internal operating temperature to below the reported maximum operating temperature. It is recommended Sources and/or Sinks poll the plug's Internal Temperature every 2 seconds.		N/A
6.5.2	<b>Plug Spacing</b>		N/A
	Active cables will support the USB Type-C vertical and horizontal spacing defined Section 3.10.2 when functioning in USB 3.2 x1 operation. However, this spacing may impose thermal constraints. Appendix D provides system design guidance to minimize the thermal impact due to connector spacing. It is recommended that products designed for USB 3.2 x2 operation with multiple adjacent USB Type-C connectors follow the design guidance in Appendix D to minimize the likelihood the active cable will go into thermal shutdown.		N/A
6.6	<b>Electrical Requirements</b>		N/A
6.6.1	<b>Shielding Effectiveness Requirement</b>		N/A
	All active cables shall meet the shielding		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
	effectiveness requirement defined in Section 3.7.7 and Figure 3-65.		
<b>6.6.2</b>	<b>Low Speed Signal Requirement</b>		N/A
<b>6.6.2.1</b>	<b>CC Channel Requirements</b>		N/A
	Active cables shall meet the Low-Speed Signal Requirements in Section 3.7.2.4.		N/A
6.6.2.2	SBU Requirements		N/A
6.6.2.2.1	Short Active Cables		N/A
	Short active cables SBU wires shall meet the requirements defined in Table 6-16 and shall meet the crosstalk requirements both near-end and far-end between the low speed signals as defined in Section 3.7.2.4.		N/A
	SBUs have no guaranteed performance when Vconn is not provided to the cable. The Host or Device shall not provide any signal beyond what is defined in Table 6-16 when VCONN has not been provided.		N/A
6.6.2.2.2	Optically Isolated Cables		N/A
	OIACs are not required to support SBU1/2 for USB 3.2 support. SBUs are not usable until the cable has entered an Alternate Mode. OIACs which choose to support SBU signals shall meet the requirements of the Alternate Mode(s) they support. Definition of the SBU requirements for Alternate Modes is outside the scope of this document.		N/A
<b>6.6.3</b>	<b>USB 2.0</b>		N/A
	The USB 2.0 support depends on the type of active cable.		N/A
6.6.3.1	Short Active Cables		N/A
	Short active cables shall meet the USB 2.0 requirements defined in Section 3.7.2.4 and 3.7.2.7.		N/A
6.6.3.2	Optically Isolated Active Cables		N/A
	OIACs forward USB 3.2 and do not forward USB 2.0. The OIAC will take action to reset the link when the USB Device drops from USB 3.2 to USB 2.0.		N/A
	During the initial connection the OIAC shall present as a USB 2.0 DFP and provide a 15K Ohm pull down on the D+/D- pins on both ends of the cable. The cable plug shall not issue a USB 2.0 Reset in this state.		N/A
	The OIAC cable plug shall issue a USB 2.0 Reset upon detecting a USB 2.0 connection on D+/D- (LS, FS, or HS USB 2.0 connection). The cable plug shall issue a USB 2.0 Bus Reset by pulling D+ and D- low for at least 50 ms.		N/A
	The OIAC shall implement a tDisableCount		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	counter to determine how many times the cable has transitioned from USB 3.2 to USB 2.0. The tDisableCount counter shall be reset to zero on either condition:		
	Power on Reset of the OIAC, or		N/A
	Successful transition to USB 3.2 U0.		N/A
	The OIAC shall present and latch a USB 2.0 billboard when tDisableCount counter reaches three.		N/A
<b>6.6.4</b>	<b>USB 3.2</b>		N/A
	Active cables shall meet the requirements in this section regardless of length. Active cables shall incorporate AC-coupling from the plug to repeater on both the USB 3.2 TX and RX signals. Active cables shall provide a discharge path for discharging the AC-coupling capacitors in the cable on unplug per USB 3.2.		N/A
6.6.4.1	USB 3.2 Active Cable Architectures		N/A
	Active cables may have the combinations of re-timers and re-drivers as illustrated in Figure 6-18. Active cables without at least one re-timer are out of scope. Active cables without retimers connected to TP3 are out of scope. Active cables shall support the features defined in Table 6-2.		N/A
6.6.4.2	USB 3.2 Power-on and Rx.Detect		N/A
	Active cables shall present a high impedance to ground of ZRX-HIGH-IMP-DC-POS when not powered. Active cables shall present a high impedance to ground of ZRX-HIGH-IMP-DC-POS at initial power-on. The active cable shall perform far-end receiver termination detection on both cable ends upon receiving VCONN. Upon detecting a far-end low-impedance receiver termination (RRX-DC), the active cable shall enable its low-impedance receiver termination (RRX-DC) to mirror the presence of the Host/Device. The active cable shall perform far-end receiver termination detection for Repeaters per USB 3.2 including in low power states U2/U3.		N/A
	An active cable shall complete power-on and far-end receiver termination detection through the cable within tFWD_RX.DETECT.		N/A
	Active cables including OIACs shall reflect the receiver terminations across the cable to replicate the behavior of a passive cable.		N/A
6.6.4.3	USB 3.2 U0 Delay		N/A
	All active cables shall meet the USB 3.2 delay defined in Table 6-18.		N/A
6.6.4.3.1	OIAC Legacy Adapter		N/A
	Table 6-19 defines the all scenarios in which an		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	OIAC will not function without an OIAC legacy adapter between the OIAC and the Legacy Device, Hub, or Host.		
	The OIAC Adapter requires the following capabilities:		N/A
	1. USB Type-C DRP/Source on the upward facing port connected to the OIAC,		N/A
	2. USB PD on the upward facing port connected to the OIAC,		N/A
	3. USB 3.2 Hub incorporating the Pending_HP_Timer ECN, and		N/A
	4. Optional: USB 2.0 to USB 3.2 transaction translator on the downstream facing port (only needed if connecting to USB 2.0-only devices, hubs, or hosts).		N/A
6.6.4.4	USB 3.2 U-State Power Requirements		N/A
	Active cables shall meet the VCONN power requirements for USB 3.2 operation in Table 6-20. These requirements are for the entire cable not just a cable plug.		N/A
6.6.4.5	USB 3.2 U-State Exit Latency		N/A
	Active cables shall meet the U-state exit latency defined in USB 3.2 Appendix E.		N/A
6.6.4.6	USB 3.2 Signal Swing		N/A
	An active cable transmitter only has to drive 8.5 dB insertion loss at 5 GHz to the Host/Device controller receiver for USB 3.2 Gen2, if the transmitter is located in the cable plug next to the receiving port.		N/A
	A Host/Device controller transmitter must drive a total loss of 23 dB at 5 GHz to the far side for USB 3.2 Gen2. The difference in loss budget allows the active cable transmitter swing to be reduced. An active cable receiver can assume a larger receiver swing than in the Host/Device for the same reason.		N/A
6.6.4.6.1	TP1 - Active Cable Input Stressed Source		N/A
	The active cable input stressed source is generated at TP1 per Table 6-21 for amplitude and per Table 6-22 for jitter. SSC shall be present in the stressed signal at TP1. Table 6-21 is a subset of the USB 3.2 Table 6-18. Table 6-22 is a subset of USB 3.2 Table 6-28. If any discrepancy exists between this specification and the USB 3.2 specification, the USB 3.2 specification shall take precedence.		N/A
	The maximum swing with the maximum de-emphasis and pre-shoot shall be tested with the minimum loss compliance test board. The minimum swing with the minimum de-emphasis and pre-shoot shall be tested with the maximum loss compliance test board. The input jitter composition is the same for both the minimum and maximum swing stressed		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	sources.		
6.6.4.6.2	TP2 - Active Cable Input (Informative)		N/A
	The values in Table 6-23 indicate the informative input signal swings at TP2 for an active cable. Table 6-23 is included to provide guidance beyond the normative requirements of Table 6-21 and Table 6-22. An active cable can be fully compliant with the normative requirements of this specification and not meet all the values in Table 6-23. Similarly, an active cable that meets all the values in Table 6-23, is not guaranteed to be in fully compliance with the normative part of this specification.		N/A
6.6.4.6.3	TP3 - Active Cable Output (Informative)		N/A
	The values in Table 6-24 indicate the informative output signal swings at TP3 for an active cable. Table 6-24 is included to provide guidance beyond the normative requirements of Table 6-21 and Table 6-22. An active cable can be fully compliant with the normative requirements of this specification and not meet all the values in Table 6-24. Similarly, an active cable that meets all the values in Table 6-24, is not guaranteed to be in full compliance with the normative part of this specification.		N/A
6.6.4.6.4	TP4 - Active Cable Output		N/A
	The active cable transmitter output is defined at TP4 for both high and low loss channels. The requirements for TP4 are defined in the USB 3.2 specification Table 6-20. The input signal for the test shall be applied at TP1 as defined in the USB 3.2 specification.		N/A
	The low loss test board shall be used to test the maximum output swing. The maximum loss test board shall be used to test the minimum output swing. Jitter must be met with both test boards.		N/A
	The active cable bit-error-rate shall be tested at TP4 and meet or exceed a BER of 10 <sup>-12</sup> . The error detector used shall have the ability to remove SKP ordered sets.		N/A
<b>6.6.5</b>	<b>USB4</b>		N/A
	This section describes the electrical requirements and compliance testing for USB4 active cables. The compliance testing is defined to ensure interoperability in terms of data integrity and electrical specifications enabling the active cable to reliably receive an input signal and output a valid signal at its other end.		N/A
	The USB4 active cable types are:		N/A
	1. Re-timer-based active cable (this section covers re-timer based cable for USB4 only, USB 3.2 re-timer cable is defined in Section		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	6.6.4)		
	2. Linear re-driver-based (LRD-based) active cable (USB 3.2 and USB4)		N/A
	3. Linear optical active cable (electrical spec not defined yet)		N/A
6.6.5.1	Electrical Requirements That Apply to All Active Cable Types		N/A
6.6.5.1.1	System Compliance Test Point Definition		N/A
	All measurements shall be referenced to the following compliance points. Calibration shall be applied in cases where direct measurement is not feasible.		N/A
6.6.5.1.2	Compliance Receptacle Test Boards		N/A
	The USB Type-C high speed test fixture shall be used to enable cable compliance testing. The fixture shall be comprised of a high-quality USB Type-C receptacle and a short PCB trace that may be connected to coaxial cable with SMA/SMP connector at its end. Because TP2 and TP3' reference points are located on the USB Type-C plug side of the connector, the loss and distortion of the receptacle fixture shall be calibrated such that all the measured values correspond to the standard reference points. The reference point TP3 is defined such that the insertion-loss from the connector pads to the compliance point is $0.5 \text{ dB} \pm 0.25 \text{ dB}$ at 5GHz and $1 \text{ dB} \pm 0.25 \text{ dB}$ at 10 GHz. Extra loss and distortion elements shall be compensated by physical and/or mathematical means.		N/A
	The target impedance of the fixture shall be 85 $\Omega$ . AC coupling capacitors shall be placed on the receptacle test fixture following the Router Assembly requirements as specified in USB4 specification and CTS.		N/A
6.6.5.1.3	AC Coupling Capacitors		N/A
	Active cables shall include AC-coupling capacitance between 135 nF and 265 nF inside their plugs placed at the output transmit path and between 300 nF and 363 nF at the input receive path. Discharge resistors between 200 K $\Omega$ and 242 K $\Omega$ shall be placed at the input receive path. See Figure 3-3 in the USB4 specification for a diagram of the AC-coupling capacitors and discharge resistors.		N/A
	Active cable designs need to consider that a change of current consumption from VBUS as allowed by USB Power Delivery can add a considerable amount of common mode offset that may not be handled by the AC-coupling in this spec.		N/A
6.6.5.1.4	Differential Return-Loss Mask (Informative)		N/A
	Re-timer and re-driver cable input and output return-loss measurements shall be referenced		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
	to a differential impedance of 85 $\Omega$ . When measured at TP3' and TP1 (respectively), the differential mode return loss recommended to not exceed the limits given in the following equation:		
6.6.5.2	Re-timer-based Active Cable Electrical Specifications		N/A
	This section describes the electrical requirements and compliance testing for USB4 re-timerbased active cables.		N/A
6.6.5.2.1	Output Equalization		N/A
	A USB4 active cable shall implement tunable 3-tap finite-impulse-response (FIR) equalization at its output. The transmit equalization shall support 16 preset configurations with different de-emphasis and pre-shoot settings as specified in the USB4 specification, and shall be measured at TP3'.		N/A
6.6.5.2.3	Cable Compliance Testing		N/A
	Table 6-26 defines the USB4 Active Cable specifications for Gen2 and Gen3 systems at TP3'. These parameters shall be measured at the Active Cable's output while applying a stressed signal at the input as specified in Table 6-27.		N/A
	A USB4 active cable shall be tested by injecting several different periodic jitter components, one at a time. The test shall include sinusoidal jitter frequencies of 1 MHz, 2 MHz, 10 MHz, 50 MHz, and 100 MHz. In all cases, the incoming signal shall include SSC modulation on top of the sinusoidal jitter component at the range of 300ppm to -5300ppm. PRBS31 pattern shall be used for USB4 active cable compliance testing. However, calibration of the stressed signal source may be performed with a periodic pattern shorter than PRBS31. AC commonmode noise shall be added at the pattern generator output to ensure worst-case transmitter characteristics. The total common-mode noise shall be 100 mV peak-to-peak at TP2, where the added noise profile shall be sinewave at frequency not smaller than 400 MHz. All the specified jitter values shall be calibrated while applying the reference CDR defined in the USB4 specification.		N/A
	A USB4 active cable receiver may configure its Link Partner's TX equalizer during the Link establishment. The pattern generator shall support tunable 3-tap FIR at its output, which may be adjusted during the test by the receiver under test through out-of-band software channel.		N/A
6.6.5.2.4	Cable Error-Bursts Testing		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
	In order to facilitate proper FEC operation, an active cable receiver shall take steps to limit the probability that a burst of errors is restarted immediately after receiving one or more correct bits (see USB4 specification). The cable receiver under test shall trigger on bit-errors and shall capture error events that follow.		N/A
	The test setup shall be initialized with the same configuration used for testing the uncoded BER with periodic jitter component of 100 MHz. As part of this setup, PRBS31 pattern is assumed and neither forward-error-correction nor pre-coding are applied. After initialization, the periodic jitter magnitude shall be increased to the point where uncoded BER of $1E-8$ is observed. The receiver under test shall trigger on bit-error and shall capture error events that follow. An error event is defined as a mismatch between the received data and the reference PRBS31 pattern. At least 32 consecutive bits shall be examined for errors starting from the initial trigger. The probability for burst renewal shall be $5E-7$ or less (i.e. one error burst restart per 2 million error captures).		N/A
	where '1' represents a bit error and '0' represents a correct bit, as expected from "exclusive or" (XOR) operation between the received bits and the synchronized reference PRBS31 pattern. Captured_data[0] corresponds to the error event trigger.		N/A
6.6.5.2.5	Noise Contributed by Integrated Return Loss (NRL)		N/A
	This section will be added in a future ECN.		N/A
6.6.5.3	Linear Re-driver-based Active Cable Electrical Requirements		N/A
	Linear re-driver-based (LRD-based) active cables shall be tested as a complete component for compliance.		N/A
	An LRD-based active cable is expected to receive a reference signal (referenced to TP2) defined in this specification and output a signal at the other end with electrical characterization that meets the requirements (referenced to TP3).		N/A
	As shown in Figure 6-27, a compliant USB Type-C receptacle shall be connected to both ends of the active cable for injecting and measuring the signal to the corresponding TP2 and TP3 reference points. Details of the Compliance Receptacle and boards can be found in Section 3.3.6 of USB4 Specification.		N/A
6.6.5.3.1	General Implementation Notes		N/A
	This specification was developed considering electrical interoperability with legacy systems, as the LRD-based Active Cables were added to		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	the USB ecosystem in a late phase when a lot of devices were already in the field.		
	The USB Type-C interconnect ecosystem assumes the worst case 1 m/2 m/0.8 m passive cable is the worst-case connection (for USB 3.2, USB4 Gen2 and USB4 Gen3 respectively).		N/A
	The intent is to align the LRD-based Active-Cable specifications to the existing passive cable specifications defined in Chapter 3 of this specification, such that the LRD-based active cable characteristics will be equal or better than those of the worst-case passive cable. The worstcase passive cable is defined in the USB 3.2 and USB4 Compliance Test Specification (CTS). This specification will define the electrical characteristics of the LRD-based cable that shall meet this requirement.		N/A
	The LRD-based active cable specification assumes no change is needed to the existing TX/RX specification of the endpoint PHYs so that compatibility to existing certified USB 3.2 and USB4 devices is maintained.		N/A
	Given this background, the following are assumptions regarding the LRD-based active cable implementation:		N/A
	1. LRD-based active cable is assumed to have no clock mechanism in its datapath (such as CDR).		N/A
	2. LRD-based active cable is assumed to not have a dynamic amplitude control (such as AGC) to avoid masking the txfe training from the receiver.		N/A
	3. LRD-based active cable is assumed to not use the training patterns to train itself, especially it is assumed to not block the output data during any phase of the training period.		N/A
	4. Receiver systems rely on the low-pass-filter nature of the cable and having an overequalized cable (i.e. weak LPF characteristic) can lead to interoperability issues. Therefore, it is recommended that when developing an LRD-based active cable, the cable should be built and tuned in a way that will make it the most passive-cable-like as opposed to most equalized cable.		N/A
6.6.5.3.2	USB4 Linear Re-driver-based Active Cable Compliance Testing		N/A
	Table 6-28 defines the USB4 linear re-driver-based active cable specifications for USB 3.2 and for USB4 Gen2 and Gen3 systems at TP3.		N/A
	These parameters shall be measured at the LRD-based active cable's output while applying a reference signal at the input as specified in Table 6-29.		N/A
	An LRD-based active cable shall be tested by injecting several patterns, calibrated to TP2.		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
6.6.5.3.3	Measurement Methods		N/A
	The compliance testing of an LRD-based active cable to this specification will be done based on measurements from both time and frequency domains.		N/A
	For all time domain specification items, the measured LRD-based active cable parameters will be compared to the worst-case passive cable supported in each technology (with nominal cable length of 1 m for USB 3.2, 2 m for USB4 Gen2 and 0.8 m for USB4 Gen3) measured in the exact same setup to reduce testing complexity.		N/A
	The worst-case passive cable is defined in the active cable CTS.		N/A
	More details on the measurement methods can be found in the active cable CTS.		N/A
6.6.5.3.4	Cable ILfit Mask (DC/f1/Nq/f2/f3/WB)		N/A
6.6.5.3.5	OUTPUT_NOISE ( $\sigma_n$ )		N/A
	$\sigma_{nn}$ is the standard deviation of the uncorrelated additive noise added to the output signal of the linear re-driver-based active cable.		N/A
	To achieve an accurate measurement, the calculation will be done based on a low frequency signal (SQ512 pattern) applied to the cable input, with 0.3 Vpp amplitude.		N/A
	Since the noise calculation is referred to the receiver input, a 2nd order Butterworth LPF filter with -2 dB @ Nq shall be applied on the captured wave to account for the receiver BW and device side platform.		N/A
	The limit of OUTPUT_NOISE is defined as function of the IL at Nyquist frequency. This allows a degree of freedom to the cable developer to trade between the cable's gain and noise.		N/A
6.6.5.3.6	SIGMA_E ( $\sigma_e$ )		N/A
	$\sigma_{eee}$ is the standard deviation of the non-linearity related noise added by the linear re-driverbased active cable.		N/A
	This measurement shall be performed twice: once with minimum input swing and once with maximum input swing.		N/A
	More details on the calculation of the non-linearity noise can be found in the Active Cable CTS and in Appendix G of this document.		N/A
6.6.5.3.7	Integrated Return-Loss (IRL)		N/A
	The IRL term for an LRD-based active cable is calculated similarly to the passive cable, see 3.7.2.3.1.		N/A
6.6.5.3.8	Integrated Multi-Reflection (IMR)		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	The IMR term for an LRD-based active cable is calculated similarly to the passive cable, see 3.7.2.3.2.		N/A
6.6.5.3.9	Evaluating Channel Operation Margin (COM)		N/A
	Channel operating margin (COM) shall be calculated for LRD-based active cables supporting USB4 Gen3, for evaluating a reference receiver margin based on the cable's measured S parameters.		N/A
	The measurements of the cable and the setting of the associated COM tool is defined in the Active Cable CTS.		N/A
6.6.5.3.10	Cable Output Eye Mask		N/A
	An LRD-based active cable shall meet eye mask limits at its output.		N/A
	The test setup shall be identical to the USB 3.2 and USB4 calibrated receiver test which includes worst case passive cable.		N/A
	During the test, a reference CTLE, DFE and TXFFE settings shall be tuned according to the USB 3.2 /USB4 spec for obtaining the optimal eye.		N/A
	1. USB 3.2 have fixed TXFFE setting according to the USB 3.2 Gen2 TX specification.		N/A
	2. USB4 can tune the TXFFE according to the TXFFE preset table in USB4 Specification Table 3-5.		N/A
	After obtaining the optimal eye with the passive cable, repeat the same measurement with the LRD cable under test, and compare the extracted eyes.		N/A
6.6.5.3.11	Cable OUTPUT_ISI		N/A
	To limit irregularity in the LRD-based active cable due to additional components (IC package etc.), an ISI-Margin test is used to evaluate the regularity of the cable's output. ISI-margin is calculating both pre-cursor and post-cursor side of the pulse and output single value. An optimal reference equalization (TXFFE, CTLE, DFE) is applied on the raw captured output signal to distinguish between equalizeable and un-equalizeable ISI.		N/A
	The following steps shall be applied for calculating OUTPUT_ISI:		N/A
	1. Using the extracted un-equalized pulse response $h(nn)$ described in section 6.6.5.3.4 and mathematically applying the reference TX equalizer, RX CTLE and DFE as defined in the relevant specification (USB 3.2 and USB4). The transmit and receiver equalization shall be selected such that the OUTPUT_ISI is maximized.		N/A
	2. Using the equalized pulse response $h_{ee}(nn)$ to calculate OUTPUT_ISI as the ratio between		N/A

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	the signal and the sum of the absolute values of the pre-cursor taps and the post cursor taps from tap 2 and above.		
	To simplify the measurement and avoid de-embedding the cable from the setup, the limit for OUTPUT_ISI is defined to be equal to or higher than a worst-case cable measured on the same setup.		N/A
6.6.5.3.12	Cable CM_NOISE		N/A
	CM_NOISE is defined as the maximum peak value of the signal captured in the cable output with common mode setting on the scope (p+n) and prbs15 data pattern.		N/A
	The CM_NOISE shall not exceed 100mV.		N/A
6.6.5.4	USB4 CL-State Power Requirements		N/A
	Active cables shall meet the VCONN power requirements for USB4 operation in Table 6-30. These requirements are for the entire cable not just a cable plug.		N/A
<b>6.6.6</b>	<b>Return Loss</b>		N/A
	Return loss is defined in the USB 3.2 specification.		N/A
<b>6.7</b>	<b>Active Cables That Support Alternate Modes</b>		N/A
	Active cables may support Alternate Modes. Active cables that support Alternate Modes shall be discoverable via USB PD. They shall use the standard USB PD mechanisms to discover, enter and exit Alternate Modes.		N/A
<b>6.7.1</b>	<b>Discover SVI</b>		N/A
	Active cables that support an Alternate Mode shall report support for SVIDs on SOP' only.		N/A
<b>6.7.2</b>	<b>Discover Modes</b>		N/A
	Active cables that support an Alternate Mode shall report support for Modes on SOP' only.		N/A
<b>6.7.3</b>	<b>Enter/Exit Modes</b>		N/A
	Enter and Exit mode shall be communicated on SOP' and on SOP'' when the SOP'' Controller Present bit is set in the Active Cable. It is recommended that Enter Mode be sent initially to SOP' and then SOP'' if supported and then SOP. It is recommended Exit Mode be sent initially to SOP and then to SOP'' if supported and then SOP'.		N/A
<b>6.7.4</b>	<b>Power in Alternate Modes</b>		N/A
	The power dissipation in an active cable's Alternate Mode shall maintain the plug's Maximum Skin Temperature below the requirement defined in Table 6-15.		N/A
	Alternate Modes should reduce power in active cables in sleep states for best user experience.		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
<b>A</b>	<b>Audio Adapter Accessory Mode</b>		N/A
<b>A.1</b>	<b>Overview</b>		N/A
	Analog audio headsets are supported by multiplexing four analog audio signals onto pins on the USB Type-C® connector when in the Audio Adapter Accessory Mode. The four analog audio signals are the same as those used by a traditional 3.5 mm headset jack. This makes it possible to use existing analog headsets with a 3.5 mm to USB Type-C adapter. The audio adapter architecture allows for an audio peripheral to provide up to 500 mA back to the system for charging.		N/A
	An analog audio adapter could be a very basic USB Type-C adapter that only has a 3.5 mm jack, or it could be an analog audio adapter with a 3.5 mm jack and a USB Type-C receptacle to enable charge-through. The analog audio headset shall not use a USB Type-C plug to replace the 3.5 mm plug.		N/A
	A USB host that implements support for USB Type-C Analog Audio Adapter Accessory mode shall also support USB Type-C Digital Audio (TCDA) with nominally equivalent functionality and performance. A USB device that implements support for USB Type-C Analog Audio Adapter Accessory mode should also support TCDA with nominally equivalent audio functionality and performance.		N/A
<b>A.2</b>	<b>Detail</b>		N/A
	An analog audio adapter shall use a captive cable with a USB Type-C plug or include an integrated USB Type-C plug.		N/A
	The analog audio adapter shall identify itself by presenting a resistance to GND of $\leq R_a$ on both A5 (CC) and B5 (VCONN) of the USB Type-C plug. If pins A5 and B5 are shorted together, the effective resistance to GND shall be less than $R_a/2$ .		N/A
	A DFP that supports analog audio adapters shall detect the presence of an analog audio adapter by detecting a resistance to GND of less than $R_a$ on both A5 (CC) and B5 (VCONN).		N/A
	The analog audio signaling presented by the headset on the 3.5 mm jack is expected to comply with at least one of the following:		N/A
	The traditional American headset jack pin assignment, with the jack sleeve used for the microphone signal, supported by CTIA-The Wireless Association		N/A
	"Local Connectivity: Wired Analogue Audio" from the Open Mobile Terminal Forum (OMTP)		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
	forum		
	“Technical Requirements and Test Methods for Wired Headset Interface of Mobile Communication Terminal” (YT/D 1885-2009) from the China Communications Standards Association		N/A
	When in the Audio Adapter Accessory Mode, the system shall not provide VCONN power on either CC1 or CC2. Failure to do this may result in VCONN being shorted to GND when an analog audio peripheral is present.		N/A
	The system shall connect A6/B6, A7/B7, A8 and B8 to an appropriate audio codec upon entry into the Audio Adapter Accessory Mode. The connections for A8 (SBU1) and B8 (SBU2) pins are dependent on the adapter's orientation. Depending on the orientation, the microphone and analog ground pins may be swapped. These pins are already reversed between the two major standards for headset jacks and support for this is built into the headset connection of many codecs or can be implemented using an autonomous audio headset switch. The system shall work correctly with either configuration.		N/A
<b>A.3</b>	<b>Electrical Requirements</b>		N/A
	The maximum ratings for pin voltages are referenced to GND (pins A1, A12, B1, and B12). The non-GND pins on the plug shall be isolated from GND on the USB Type-C connector and shall be isolated from the USB plug shell. To minimize the possibility of ground loops between systems, AGND shall be connected to GND only within the system containing the USB Type-C receptacle. Both the system and audio device implementations shall be able to tolerate the Right, Left, Mic, and AGND signals being shorted to GND. The current provided by the amplifier driving the Right and Left signals shall not exceed $\pm 150$ mA per audio channel, even when driving a 0 $\Omega$ load.		N/A
	The maximum voltage ratings for Left and Right signals are selected to encompass a 2 Vrms sine wave ( $2.828 V_p = 5.657 V_{pp} = 6$ dBV) which is a common full-scale voltage for headset audio output.		N/A
	Headset microphones operate on a positive bias voltage provided by the system's audio codec and AC-couple the audio signal onto it. Some headsets may produce an audio signal level up to 0.5 Vrms ( $0.707 V_p = 1.414 V_{pp} = -6$ dBV) but this is biased so that the voltage does not swing below GND. The bias voltage during operation is typically around 1.25 V but it varies quite a bit depending on the specifics of		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	the manufacturer's design, therefore the maximum voltage rating for the SBU pins is selected to allow a variety of existing solutions.		
	While one SBU pin carries the Mic signal, the other SBU pin serves as AGND carrying the return current for Left, Right, and Mic. If we assume a worst-case headset speaker impedance of 16 $\Omega$ per speaker, then the worst-case return current for the speakers is $\pm 0.2A$ . If we assume that the worst-case resistance from the AGND pin to GND within the USB Type-C system is 1 $\Omega$ (due to FET RON within the signal multiplexer, contact, and trace resistances), then the voltage of the AGND pin with respect to USB Type-C GND can vary between $\pm 0.2 V$ . The minimum voltage rating for the SBU pins has been selected to allow for this scenario with some additional margin to account for Mic signal return current and tolerances.		N/A
	The system shall exhibit no more than -48 dB linear crosstalk between the Left and Right audio channels and exhibit no more than -51 dB linear crosstalk from the Left or Right channel to the Mic channel. Crosstalk measurements shall be made using a measurement adapter plug that supports USB Type-C analog audio connections according to Table A-1. In the measurement adapter, the Left and Right channels are terminated with 32 $\Omega$ resistors to AGND, the Mic channel is terminated with 2k $\Omega$ resistor to AGND; AGND is connected to USB Type-C Plug Pin A8, and the Mic channel is connected to USB Type-C Plug Pin B8.		N/A
	A DTS shall cease to supply VBUS within tVBUSOFF of exiting AttachedDeb.SRC.		N/A
<b>A.4</b>	<b>Example Implementations</b>		N/A
<b>A.4.1</b>	<b>Passive 3.5 mm to USB Type-C Adapter - Single Pole Detection Switch</b>		N/A
	Figure A-1 illustrates how a simple 3.5 mm analog audio adapter can be made. In this design, there is an audio plug that contains a single-pole detection switch that is used to completely disconnect the CC and VCONN pins from digital GND when no 3.5 mm plug is inserted. This has the effect of triggering the USB Type-C presence detect logic upon insertion or removal of either the 3.5 mm plug or the audio adapter itself.		N/A
<b>A.4.2</b>	<b>3.5 mm to USB Type-C Adapter Supporting 500 mA Charge-Through</b>		N/A
	Figure A-2 illustrates a 3.5 mm analog audio adapter that supports charge-through operation. Charging power comes into the		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	<p>adapter through a USB Type-C receptacle and is routed directly to the adapter's USB Type-C plug, which is plugged into the device being charged. This design is limited to providing 500 mA of charge-through current since it has no way to advertise greater current-sourcing capability. The USB Type-C receptacle presents Rd on both of its CC pins because a CC pull-down must be present for the receptacle to indicate that it wants to consume VBUS current. USB Type-C systems that support analog audio should ensure that charging is not interrupted by insertion or removal of the 3.5 mm audio plug and that audio is not interrupted by insertion or removal of the cable connected to the audio adapter's USB Type-C receptacle by using the system's presence detection logic monitoring the states of both the CC1 and CC2 pins and VBUS.</p>		
<b>B</b>	<b>Debug Accessory Mode</b>		N/A
<b>B.1</b>	<b>Overview</b>		N/A
	<p>This appendix covers the functional requirements for the USB Type-C® Debug Accessory Mode (DAM), Debug and Test System (DTS), and Target System (TS). The USB Type-C connector is ideal for debug of closed-chassis, form-factor devices. Debug covers many areas, ranging from detailed JTAG Test Access Port (TAP)-level debug in a lab to high-level debug of software applications in production. Lab debug requires early debug access to hardware registers soon after reset, whereas software debug uses kernel debuggers, etc. to access software state. Debug Accessory Mode in USB Type-C enables debug of closedchassis, form-factor devices by re-defining the USB Type-C ports for debug purposes.</p>		N/A
	<p>Basic debug requirements are defined as a standard feature, and additional debug features may be added as per vendor specifications.</p>		N/A
<b>B.2</b>	<b>Functional</b>		N/A
	<p>The USB Type-C Debug Accessory Mode follows a layered structure as shown in Figure B-1, defining the minimum physical layer for Attach, Detection and Power. Orientation detection is optional normative. The transport layer is left proprietary and is not covered in this document.</p>		N/A
<b>B.2.1</b>	<b>Signal Summary</b>		N/A
	<p>Figure B-2 shows the pin assignments of the DTS plug that are used to support DAM. The</p>		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	pins highlighted in yellow are those available to be configured for debug signals. Both CC1 and CC2 are used for current advertisement and optional orientation detection.		
	The DTS and TS must follow the USB Safe State as defined in the USB PD specification at all times (whether in DAM or not).		N/A
<b>B.2.2</b>	<b>Port Interoperability</b>		N/A
	Table B-1 summarizes the expected results when interconnecting a DTS Source, Sink or DRP port to a TS Source, Sink or DRP port.		N/A
<b>B.2.3</b>	<b>Debug Accessory Mode Entry</b>		N/A
	The typical flow for the configuration of the interface in the general case of a DTS to a TS is as follows:		N/A
	1. Detect a valid connection between the DTS (Source, Sink, or DRP) and TS (Source, Sink, or DRP)		N/A
	2. Optionally determine orientation of the plug in the receptacle		N/A
	3. Optionally establish USB PD communication over CC for advanced power delivery negotiation and Alternate Modes. USB PD communication is allowed only if the optional orientation of the plug is determined.		N/A
	4. Establish test access connections with the available USB Type-C signals		N/A
	The DTS DRP will connect as either a Source or a Sink, but its state diagram gives preference to the Source role.		N/A
<b>B.2.3.1</b>	<b>Detecting a Valid DTS-to-TS Connection</b>		N/A
	The general concept for setting up a valid connection between a DTS and TS is based on being able to detect the typical USB Type-C termination resistances. However, detecting a Debug Accessory Mode connection requires that both CC pins must detect a pull-up (Rp) or pull-down (Rd) termination. A USB Type-C Cable does not pass both CC wires so a receptacle to receptacle Debug Accessory Mode connection cannot be detected.		N/A
	A DTS is only allowed to connect to a TS that is presenting either Rp/Rp or Rd/Rd. Otherwise, the TS does not support Debug Accessory Mode.		N/A
	To detect either an Rp/Rp or Rd/Rd, the DTS must be a captive cable or a direct-attach device with a USB Type-C plug and the TS must have a USB Type-C receptacle.		N/A
<b>B.2.4</b>	<b>Connection State Diagrams</b>		N/A
	This section provides reference connection state diagrams for CC-based behaviors of the DTS. The TS connection state diagrams are found in Section 4.5.2.		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	Refer to Section B.2.4.1 for the specific state transition requirements related to each state shown in the diagrams.		N/A
	Refer to Section B.2.4.3 for a description of which states are mandatory for each port type and a list of states where USB PD communication is permitted.		N/A
B.2.4.1	Connection State Machine Requirements		N/A
	The DTS state machine requirements follow those outlined in Section 4.5.2.2 for the general USB Type-C state machines with the additional following states defined.		N/A
B.2.4.1.1	Exiting from ErrorRecovery State		N/A
	The ErrorRecovery state is where the DTS cycles its connection by removing all terminations from the CC pins for tErrorRecovery followed by transitioning to the appropriate UnattachedDeb.SNK or UnattachedDeb.SRC state based on DTS type.		N/A
	The DTS should transition to the ErrorRecovery state from any other state when directed.		N/A
	A DTS may choose not to support the ErrorRecovery state. If the ErrorRecovery state is not supported, the DTS shall be directed to the Disabled state if supported. If the Disabled state is not supported, the DTS shall be directed to either the UnattachedDeb.SNK or UnattachedDeb.SRC states.		N/A
	A DTS Sink shall transition to UnattachedDeb.SNK after tErrorRecovery.		N/A
	A DTS Source shall transition to UnattachedDeb.SRC after tErrorRecovery.		N/A
	A DTS DRP shall transition to UnattachedDeb.SRC after tErrorRecovery.		N/A
B.2.4.1.2	UnattachedDeb.SNK State		N/A
	When in the UnattachedDeb.SNK state, the DTS is waiting to detect the presence of a TS Source.		N/A
	A DTS with a dead battery shall enter this state while unpowered.		N/A
B.2.4.1.2.1	UnattachedDeb.SNK Requirements		N/A
	The DTS shall not drive VBUS.		N/A
	Both CC pins shall be independently terminated to ground through Rd.		N/A
B.2.4.1.2.2	Exiting from UnattachedDeb.SNK State		N/A
	The DTS shall transition to AttachWaitDeb.SNK when a TS Source connection is detected, as indicated by the SNK.Rp state on both of its CC pins.		N/A
	A DTS DRP shall transition to UnattachedDeb.SRC within tDRPTransition after the state of one or both CC pins is		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
	SNK.Open for tDRP – dcSRC.DRP · tDRP, or if directed.		
B.2.4.1.3	AttachWaitDeb.SNK State		N/A
	When in the AttachWaitDeb.SNK state, the DTS has detected the SNK.Rp state on both CC pins and is waiting for VBUS.		N/A
B.2.4.1.3.1	AttachWaitDeb.SNK Requirements		N/A
	The requirements for this state are identical to UnattachedDeb.SNK.		N/A
B.2.4.1.3.2	Exiting from AttachWaitDeb.SNK State		N/A
	A DTS Sink shall transition to UnattachedDeb.SNK when the state of one or both CC pins is SNK.Open for at least tPDDebounce.		N/A
	A DTS DRP shall transition to UnattachedDeb.SRC when the state of one or both CC pins is SNK.Open for at least tPDDebounce.		N/A
	A DTS Sink shall transition to AttachedDeb.SNK when neither CC pin is SNK.Open after tCCDebounce and VBUS is detected.		N/A
	A DTS DRP shall transition to TryDeb.SRC when neither CC pin is SNK.Open after tCCDebounce and VBUS is detected.		N/A
B.2.4.1.4	AttachedDeb.SNK State		N/A
	When in the AttachedDeb.SNK state, the DTS is attached and operating as a DTS Sink.		N/A
B.2.4.1.4.1	AttachedDeb.SNK Requirements		N/A
	This mode is for debug only		N/A
	The port shall not drive VBUS.		N/A
	The port shall provide an Rd as specified in Table 4-15 on both CC pins if orientation is not needed. See Section B.2.6 for orientation detection.		N/A
	The port shall monitor to detect when VBUS is removed.		N/A
	If the DTS needs to establish a USB PD communications, it shall do so only after entry to this state. In this state, the DTS takes on the initial USB PD role of UFP/Sink.		N/A
	The DTS shall connect the debug signals for Debug Accessory Mode operation only after entry to this state.		N/A
	The DTS may follow the DAM Sink Power Sub-State behavior specified in Section 4.5.2.3.		N/A
B.2.4.1.4.2	Exiting from AttachedDeb.SNK State		N/A
	A DTS shall transition to UnattachedDeb.SNK when VBUS is no longer present		N/A
B.2.4.1.5	UnattachedDeb.SRC State		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
	When in the UnattachedDeb.SRC state, the DTS is waiting to detect the presence of a TS Sink		N/A
B.2.4.1.5.1	UnattachedDeb.SRC Requirements		N/A
	The DTS shall not drive VBUS.		N/A
	The DTS shall source current on both CC pins independently.		N/A
	The DTS shall provide a unique Rp value on each CC pin as specified in Section 4.5.2.3.		N/A
B.2.4.1.5.2	Exiting from UnattachedDeb.SRC State		N/A
	The DTS shall transition to AttachWaitDeb.SRC when the SRC.Rd state is detected on both CC pins.		N/A
	A DTS DRP shall transition to UnattachedDeb.SNK within tDRPTransition after dcSRC.DRP · tDRP, or if directed.		N/A
B.2.4.1.6	AttachWaitDeb.SRC State		N/A
	The AttachWaitDeb.SRC state is used to ensure that the state of both of the CC pins is stable after a TS Sink is connected.		N/A
B.2.4.1.6.1	AttachWaitDeb.SRC Requirements		N/A
	The requirements for this state are identical to UnattachedDeb.SRC.		N/A
B.2.4.1.6.2	Exiting from AttachWaitDeb.SRC State		N/A
	The DTS shall transition to AttachedDeb.SRC when VBUS is at vSafe0V and the SRC.Rd state is detected on both of the CC pins for at least tCCDebounce.		N/A
	A DTS Source shall transition to UnattachedDeb.SRC and a DTS DRP to UnattachedDeb.SNK when the SRC. Open state is detected on either of the CC pins.		N/A
B.2.4.1.7	AttachedDeb.SRC State		N/A
	When in the AttachedDeb.SRC state, the DTS is attached and operating as a DTS Source.		N/A
B.2.4.1.7.1	AttachedDeb.SRC Requirements		N/A
	The DTS shall provide a unique Rp value on each CC pin as specified in Section B.2.4.2.		N/A
	The DTS shall supply VBUS current at the level it advertises. See Section B.2.6.1.1 for advertising current level.		N/A
	The DTS shall supply VBUS within tVBUSON of entering this state, and for as long as it is operating as a power source.		N/A
	If the DTS needs to establish USB PD communications, it shall do so only after entry to this state. The DTS shall not initiate any USB PD communications until VBUS reaches vSafe5V. In this state, the DTS takes on the initial USB PD role of DFP/Source.		N/A
	The DTS shall connect the debug signals for		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	Debug Accessory Mode operation only after entry to this state.		
B.2.4.1.7.2	Exiting from AttachedDeb.SRC State		N/A
	A DTS Source shall transition to UnattachedDeb.SRC when the SRC. Open state is detected on either CC pin.		N/A
	A DTS DRP shall transition to UnattachedDeb.SNK when SRC. Open is detected on either CC pin.		N/A
	A DTS shall cease to supply VBUS within tVBUSOFF of exiting AttachedDeb.SRC.		N/A
B.2.4.1.8	TryDeb.SRC State		N/A
	When in the TryDeb.SRC state, the DTS DRP is querying to determine if the TS is also a DRP, to favor the DTS taking the Source role.		N/A
B.2.4.1.8.1	TryDeb.SRC Requirements		N/A
	The DTS shall not drive VBUS.		N/A
	The DTS shall source current on both CC pins independently.		N/A
	The DTS shall provide a unique Rp value on each CC pin as specified in Section B.2.4.2.		N/A
B.2.4.1.8.2	Exiting from TryDeb.SRC State		N/A
	The DTS shall transition to AttachedDeb.SRC when the SRC.Rd state is detected on both CC pins for at least tTryCCDebounce.		N/A
	The DTS shall transition to TryWaitDeb.SNK after tDRPTry if the state of both CC pins is not SRC.Rd.		N/A
B.2.4.1.9	TryWaitDeb.SNK State		N/A
	When in the TryWaitDeb.SNK state, the DTS has failed to become a DTS Source and is waiting to attach as a DTS Sink.		N/A
B.2.4.1.9.1	TryWaitDeb.SNK Requirements		N/A
	The DTS shall not drive VBUS.		N/A
	Both CC pins shall be independently terminated to ground through Rd.		N/A
B.2.4.1.9.2	Exiting from TryWaitDeb.SNK State		N/A
	The DTS shall transition to AttachedDeb.SNK when neither CC pin is SNK.Open after tCCDebounce and VBUS is detected.		N/A
	The DTS shall transition to UnattachedDeb.SNK when the state of one of the CC pins is SNK.Open for at least tPDDebounce or if VBUS is not detected within tPDDebounce.		N/A
B.2.4.2	Power Sub-State Requirements		N/A
B.2.4.2.1	TS Sink Power Sub-State Requirements		N/A
	When in the DebugAccessory.SNK state and the DTS Source is supplying default VBUS, the TS Sink shall operate in one of the sub-states		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	shown in Figure B-6. The initial TS Sink Power Sub-State is PowerDefaultDeb.SNK. Subsequently, the TS Sink Power Sub-State is determined by the DTS Source's USB Type-C current advertisement determined by the Rp value on each CC pin as shown in Table B-2. The TS Sink in the attached state shall remain within the TS Sink Power Sub-States until either VBUS is removed or a USB PD contract is established with the Source.		
	The TS Sink is only required to implement TS Sink Power Sub-State transitions if the TS Sink wants to consume more than default USB current.		N/A
B.2.4.2.2	PowerDefaultDeb.SNK Sub-State		N/A
	This sub-state supports DAM Sinks consuming current within the lowest range (default) of Source-supplied current.		N/A
B.2.4.2.2.1	PowerDefaultDeb.SNK Requirements		N/A
	The port shall draw no more than the default USB power from VBUS. See Section 4.6.2.1.		N/A
	If the DTS Sink wants to consume more than the default USB power, it shall monitor vRd on both CC pins to determine if more current is available from the Source.		N/A
B.2.4.2.2.2	Exiting from PowerDefaultDeb.SNK		N/A
	For any change on CC indicating a change in allowable power, the DAM Sink shall not transition until the new vRd voltages on each CC pin have been stable for at least tRpValueChange.		N/A
	For vRd voltages on the CC pins indicating 1.5 A mode, the DAM Sink shall transition to the Power1.5Deb.SNK Sub-State.		N/A
	For vRd voltages on the CC pins indicating 3 A mode, the DAM Sink shall transition to the Power 3.0Deb.SNK Sub-State.		N/A
B.2.4.2.3	Power1.5Deb.SNK Sub-State		N/A
	This sub-state supports DAM Sinks consuming current within the two lower ranges (default and 1.5 A) of DAM Source-supplied current.		N/A
B.2.4.2.3.1	Power1.5Deb.SNK Requirements		N/A
	The DAM Sink shall draw no more than 1.5 A from VBUS.		N/A
	The DAM Sink shall monitor both vRd voltages while it is in this sub-state.		N/A
B.2.4.2.3.2	Exiting from Power1.5Deb.SNK		N/A
	For any change on the CC pins indicating a change in allowable power, the DAM Sink shall not transition until the new vRd voltages on both CC pins have been stable for at least tRpValueChange.		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	For vRd voltages on the CC pins indicating Default USB Power mode, the port shall transition to the PowerDefaultDeb.SNK Sub-State and reduce its power consumption to the new range within tSinkAdj.		N/A
	For vRd voltages on the CC pins indicating 3 A mode, the port shall transition to the Power 3.0 Deb.SNK Sub-State.		N/A
B.2.4.2.4	Power3.0Deb.SNK Sub-State		N/A
	This sub-state supports DAM Sinks consuming current within all three ranges (default, 1.5 A and 3.0 A) of DAM Source-supplied current.		N/A
B.2.4.2.4.1	Power3.0Deb.SNK Requirements		N/A
	The port shall draw no more than 3.0 A from VBUS.		N/A
	The port shall monitor both vRd voltages while it is in this sub-state.		N/A
B.2.4.2.4.2	Exiting from Power3.0Deb.SNK		N/A
	For any change on the CC pins indicating a change in allowable power, the port shall not transition until the new vRd voltages on both CC pins have been stable for at least tRpValueChange.		N/A
	For vRd voltages on the CC pins indicating Default USB Power mode, the port shall transition to the PowerDefaultDeb.SNK Sub-State and reduce its power consumption to the new range within tSinkAdj.		N/A
	For vRd voltages on the CC pins indicating 1.5 A mode, the DAM Sink shall transition to the Power 1.5Deb.SNK Sub-State.		N/A
B.2.4.2.5	DTS Sink Power Sub-State Requirements		N/A
	A DTS Sink follows the same power sub-states defined in Section 4.5.2.2.22. The TS Source will be advertising current with a standard Rp value that is the same for each CC pin. If optional orientation detection is performed, the DTS Sink will only be able to determine the Rp value from the CC pin that is set for USB PD communication.		N/A
B.2.4.3	Connection States Summary		N/A
	Table B-3 defines the mandatory and optional states for each type of port. For states allowing USB PD communication, DAM connections requiring USB PD communication shall determine orientation by the steps described in Section B.2.6.		N/A
<b>B.2.5</b>	<b>DTS Port Interoperability Behavior</b>		N/A
	This section describes interoperability behavior between DTS ports and TS ports.		N/A
B.2.5.1	DTS Port to TS Port Interoperability Behaviors		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	The following sub-sections describe typical port-to-port interoperability behaviors for the various combinations of DTS and TS Sources, Sinks and DRPs as presented in Table B-1.		N/A
B.2.5.1.1	DTS Source to TS Sink Behavior		N/A
	The following describes the behavior when a DTS Source is connected to a TS Sink.		N/A
	1. DTS Source and TS Sink in the unattached state		N/A
	2. DTS Source transitions from UnattachedDeb.SRC to AttachedDeb.SRC through AttachWaitDeb.SRC		N/A
	DTS Source detects the TS Sink's pull-downs on both CC pins and enters AttachWaitDeb.SRC. After tCCDebounce it then enters AttachedDeb.SRC		N/A
	DTS Source turns on VBUS		N/A
	3. TS Sink transitions from Unattached.SNK to DebugAccessory.SNK through AttachWait.SNK		N/A
	TS Sink in Unattached.SNK detects the DTS Source's pull-ups on both CC pins and enters AttachWait.SNK. After that state persists for tCCDebounce and it detects VBUS, it enters DebugAccessory.SNK		N/A
	4. While the DTS Source and TS Sink are in the attached state:		N/A
	DTS Source adjusts both Rp values as needed for offered current		N/A
	TS Sink detects and monitors vRd on the CC pins for available current on VBUS and performs any orientation required		N/A
	DTS Source monitors both CC pins for detach and when detected on either pin, enters UnattachedDeb.SRC		N/A
	TS Sink monitors VBUS for detach and when detected, enters Unattached.SNK		N/A
B.2.5.1.2	DTS Source to TS DRP Behavior		N/A
	The following describes the behavior when a DTS Source is connected to a TS DRP.		N/A
	1. DTS Source and TS DRP in the unattached state		N/A
	TS DRP alternates between Unattached.SRC and Unattached.SNK		N/A
	2. DTS Source transitions from UnattachedDeb.SRC to AttachedDeb.SRC through AttachWaitDeb.SRC		N/A
	DTS Source detects the TS DRP's pull-downs on both CC pins and enters AttachWaitDeb.SRC. After tCCDebounce it then enters AttachedDeb.SRC		N/A
	DTS Source turns on VBUS		N/A
	3. TS DRP transitions from Unattached.SNK to DebugAccessory.SNK through AttachWait.SNK		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
	TS DRP in Unattached.SNK detects the DTS Source's pull-ups on both CC pins and enters AttachWait.SNK. After that state persists for tCCDebounce and it detects VBUS, it enters DebugAccessory.SNK		N/A
	4. While the DTS Source and TS DRP are in their respective attached states:		N/A
	DTS Source adjusts both Rp values as needed for offered current		N/A
	TS DRP detects and monitors vRd on both CC pins for available current on VBUS and performs any orientation required		N/A
	DTS Source monitors both CC pins for detach and when detected, enters UnattachedDeb.SRC		N/A
	TS DRP monitors VBUS for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)		N/A
B.2.5.1.3	DTS Sink to TS Source Behavior		N/A
	The following describes the behavior when a DTS Sink is connected to a TS Source.		N/A
	1. TS Source and DTS Sink in the unattached state		N/A
	2. TS Source transitions from Unattached.SRC to UnorientedDebugAccessory.SRC through AttachWait.SRC		N/A
	TS Source detects the DTS Sink's pull-downs on both CC pins and enters AttachWait.SRC. After tCCDebounce, it enters UnorientedDebugAccessory.SRC.		N/A
	TS Source turns on VBUS		N/A
	3. DTS Sink transitions from UnattachedDeb.SNK to AttachedDeb.SNK through AttachWaitDeb.SNK.		N/A
	DTS Sink in UnattachedDeb.SNK detects the TS Source's pull-ups on both CC pins and enters AttachWaitDeb.SNK.		N/A
	DTS Sink in AttachWaitDeb.SNK detects that the pull-ups on both CC pins persist for tCCDebounce and it detects VBUS. It enters AttachedDeb.SNK		N/A
	DTS sink determines advertised current from vRd on either CC pin.		N/A
	4. If orientation supported, DTS Sink adjusts Rd on the non-CC communication pin as needed for orientation detection.		N/A
	5. If orientation supported, TS Source detects change in vRd of one of the CC pins and transitions from UnorientedDebugAccessory.SRC to OrientedDebugAccessory.SRC and performs any orientation required.		N/A
	6. While the TS Source and DTS Sink are in the attached state:		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	If orientation is supported, DTS sink determines any change in advertised current from vRd of the CC pin that has been set as the CC communication pin.		N/A
	TS Source monitors both CC pins for detach and when detected, enters Unattached.SRC		N/A
	DTS Sink monitors VBUS for detach and when detected, enters UnattachedDeb.SNK		N/A
B.2.5.1.4	DTS Sink to TS DRP Behavior		N/A
	The following describes the behavior when a DTS Sink is connected to a TS DRP.		N/A
	1. DTS Sink and TS DRP in the unattached state		N/A
	TS DRP alternates between Unattached.SRC and Unattached.SNK		N/A
	2. TS DRP transitions from Unattached.SRC to UnorientedDebugAccessory.SRC through AttachWait.SRC		N/A
	TS DRP in Unattached.SRC detects both CC pull-downs of DTS Sink in UnattachedDeb.SNK and enters AttachWait.SRC		N/A
	TS DRP in AttachWait.SRC detects that the pull-downs on both CC pins persist for tCCDebounce. It then enters UnorientedDebugAccessory.SRC and turns on VBUS		N/A
	3. DTS Sink transitions from UnattachedDeb.SNK to AttachedDeb.SNK through AttachWaitDeb.SNK.		N/A
	DTS Sink in UnattachedDeb.SNK detects the TS DRP's pull-ups on both CC pins and enters AttachWaitDeb.SNK. After that state persists for tCCDebounce and it detects VBUS, it enters AttachedDeb.SNK		N/A
	DTS sink determines advertised current from vRd on either CC pin.		N/A
	7. If orientation is supported, DTS Sink adjusts Rd on the non-CC communication pin as needed for orientation detection.		N/A
	8. If orientation supported, TS DRP detects change in vRd on one of the CC pins and transitions to OrientedDebugAccessory.SRC and performs the required orientation.		N/A
	9. While the TS DRP and DTS Sink are in the attached state:		N/A
	If orientation is supported, DTS sink determines any change in advertised current from vRd of the CC pin that has been set as the CC communication pin.		N/A
	TS DRP monitors both CC pins for detach and when detected, enters Unattached.SNK		N/A
	DTS Sink monitors VBUS for detach and when detected, enters UnattachedDeb.SNK		N/A
B.2.5.1.5	DTS DRP to TS Sink Behavior		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	The following describes the behavior when a DTS DRP is connected to a TS Sink.		N/A
	1. DTS DRP and TS Sink in the unattached state		N/A
	DTS DRP alternates between UnattachedDeb.SRC and UnattachedDeb.SNK		N/A
	2. DTS DRP transitions from UnattachedDeb.SRC to AttachedDeb.SRC through AttachWaitDeb.SRC		N/A
	DTS DRP in UnattachedDeb.SRC detects both of the CC pull-downs of TS Sink enters AttachWaitDeb.SRC		N/A
	DTS DRP in AttachWaitDeb.SRC detects that the pull-downs on both CC pins persist for tCCDebounce. It then enters AttachedDeb.SRC		N/A
	DTS DRP turns on VBUS		N/A
	3. TS Sink transitions from Unattached.SNK to DebugAccessory.SNK through AttachWait.SNK		N/A
	TS Sink in Unattached.SNK detects the DTS DRP's pull-ups on both CC pins and enters AttachWait.SNK		N/A
	TS Sink in AttachWait.SNK detects that the pull-ups on both CC pins persist for tCCDebounce and it detects VBUS. It enters DebugAccessory.SNK		N/A
	4. While the DTS DRP and TS Sink are in their respective attached states:		N/A
	DTS DRP adjusts Rp as needed for offered current		N/A
	TS Sink detects and monitors vRd on the CC pins for available current on VBUS and performs any orientation required		N/A
	DTS DRP monitors both CC pins for detach and when detected, enters UnattachedDeb.SNK		N/A
	TS Sink monitors VBUS for detach and when detected, enters Unattached.SNK		N/A
B.2.5.1.6	DTS DRP to TS DRP Behavior		N/A
	The following describes the behavior when a DTS DRP is connected to TS DRP.		N/A
	Case #1:		N/A
	1. Both DRPs in the unattached state		N/A
	DTS DRP alternates between UnattachedDeb.SRC and UnattachedDeb.SNK		N/A
	TS DRP alternate between Unattached.SRC and Unattached.SNK		N/A
	2. DTS DRP transitions from UnattachedDeb.SRC to AttachWaitDeb.SRC		N/A
	DTS DRP in UnattachedDeb.SRC detects both CC pull-downs of TS DRP in Unattached.SNK and enters AttachWaitDeb.SRC		N/A
	3. TS DRP transitions from Unattached.SNK to AttachWait.SNK		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	TS DRP in Unattached.SNK detects both CC pull-ups of DTS DRP and enters AttachWait.SNK		N/A
	4. DTS DRP transitions from AttachWaitDeb.SRC to AttachedDeb.SRC		N/A
	DTS DRP in AttachWaitDeb.SRC continues to see both CC pull-downs of TS DRP for tCCDebounce, enters AttachedDeb.SRC and turns on VBUS		N/A
	5. TS DRP transitions from AttachWait.SNK to DebugAccessory.SNK		N/A
	TS DRP detects DTS DRP's pull-ups on both CC pins for tCCDebounce and detects VBUS and enters DebugAccessory.SNK		N/A
	TS DRP detects and monitors vRd on the CC pins for available current on VBUS and performs any orientation required		N/A
	6. While the TS DRP and DTS DRP are in the attached state:		N/A
	TS DRP monitors VBUS for detach and when detected, enters Unattached.SNK		N/A
	DTS DRP monitors both CC pins for detach and when detected, enters UnattachedDeb.SNK		N/A
	Case #2:		N/A
	1. Both DRPs in the unattached state		N/A
	DTS DRP alternates between UnattachedDeb.SRC and UnattachedDeb.SNK		N/A
	TS DRP alternate between Unattached.SRC and Unattached.SNK		N/A
	2. DTS DRP transitions from UnattachedDeb.SNK to AttachWaitDeb.SNK		N/A
	DTS DRP in UnattachedDeb.SNK detects both CC pull-ups of TS DRP in Unattached.SRC and enters AttachWaitDeb.SNK		N/A
	3. TS DRP transitions from Unattached.SRC to UnorientedDebugAccessory.SRC through AttachWait.SRC		N/A
	TS DRP in Unattached.SRC detects both CC pull-downs of DTS DRP and enters AttachWait.SRC		N/A
	TS DRP in AttachWait.SRC continues to see both CC pull-downs of TS DRP for tCCDebounce, enters UnorientedDebugAccessory.SRC and turns on VBUS		N/A
	4. DTS DRP transitions from AttachWaitDeb.SNK to TryDeb.SRC		N/A
	DTS DRP in AttachWaitDeb.SNK continues to see both CC pull-ups of TS DRP for tCCDebounce and detects VBUS, enters TryDeb.SRC		N/A
	5. TS DRP transitions from UnorientedDebugAccessory.SRC to		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	Unattached.SNK		
	TS DRP in UnorientedDebugAccessory.SRC detects the removal of both CC pull-downs of DTS DRP and enters Unattached.SNK		N/A
	6. TS DRP transitions from Unattached.SNK to AttachWait.SNK		N/A
	TS DRP in Unattached.SNK detects both CC pull-ups of DTS DRP and enters AttachWait.SNK		N/A
	7. DTS DRP transitions from TryDeb.SRC to AttachedDeb.SRC		N/A
	DTS DRP in TryDeb.SRC detects both CC pull-downs of TS DRP for tTryCCDebounce and enters AttachedDeb.SRC		N/A
	DTS DRP turns on VBUS		N/A
	8. TS DRP transitions from AttachWait.SNK to DebugAccessory.SNK		N/A
	TS DRP detects DTS DRP's pull-ups on both CC pins for tCCDebounce and detects VBUS and enters DebugAccessory.SNK		N/A
	9. While the DTS DRP and TS DRP are in their respective attached states:		N/A
	DTS DRP adjusts Rp as needed for offered current		N/A
	TS DRP detects and monitors vRd on the CC pins for available current on VBUS and performs any orientation required		N/A
	DTS DRP monitors both CC pins for detach and when detected, enters UnattachedDeb.SNK		N/A
	TS DRP monitors VBUS for detach and when detected, enters Unattached.SNK		N/A
B.2.5.1.7	DTS DRP to TS Source Behavior		N/A
	The following describes the behavior when a DTS DRP is connected to TS Source.		N/A
	1. DTS DRP and TS Source in the unattached state		N/A
	DTS DRP alternates between UnattachedDeb.SRC and UnattachedDeb.SNK		N/A
	TS Source in Unattached.SRC		N/A
	2. DTS DRP transitions from UnattachedDeb.SNK to AttachWaitDeb.SNK		N/A
	DTS DRP in UnattachedDeb.SNK detects pull-ups on both CC pins and enters AttachWaitDeb.SNK		N/A
	3. TS Source transitions from Unattached.SRC to UnorientedDebugAccessory.SRC through AttachWait.SRC		N/A
	TS Source in Unattached.SRC detects both CC pull-downs of DTS DRP and enters AttachWait.SRC		N/A
	TS Source in AttachWait.SRC continues to see both CC pull-downs of DTS DRP for tCCDebounce, enters		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
	UnorientedDebugAccessory.SRC and turns on VBUS		
	4. DTS DRP transitions from AttachWaitDeb.SNK to TryDeb.SRC		N/A
	DTS DRP in AttachWaitDeb.SNK continues to see both CC pull-ups of TS DRP for tCCDebounce and detects VBUS, enters TryDeb.SRC		N/A
	5. TS Source transitions from UnorientedDebugAccessory.SRC to Unattached.SRC		N/A
	TS Source in UnorientedDebugAccessory.SRC detects the removal of both CC pull-downs of DTS DRP and enters Unattached.SRC		N/A
	6. DTS DRP transitions from TryDeb.SRC to TryWaitDeb.SNK		N/A
	After tDRPTry, DTS DRP does not see pull-downs on both CC pin and enters TryWaitDeb.SNK		N/A
	7. TS Source transitions from Unattached.SRC to UnorientedDebugAccessory.SRC		N/A
	TS Source in Unattached.SRC detects pull-downs on both CC pins and enters AttachWait.SRC		N/A
	TS Source continues to detect pull-downs on both CC pins for tCCDebounce and enters UnorientedDebugAccessory.SRC and outputs VBUS		N/A
	8. DTS DRP transitions from TryWaitDeb.SNK to AttachedDeb.SNK		N/A
	DTS DRP sees pull-ups on both CC pins for tCCDebounce and detects VBUS and enters AttachedDeb.SNK		N/A
	If orientation required, DTS DRP adjusts Rd on the non-CC communication pin as needed for orientation detection		N/A
	9. If orientation supported, TS Source detects change in vRd on one of the CC pins and transitions to OrientedDebugAccessory.SRC and performs the required orientation.		N/A
	10. While the TS Source and DTS DRP are in the attached state:		N/A
	If orientation is supported, DTS DRP determines any change in advertised current from vRd of the CC pin that has been set as the CC communication pin.		N/A
	TS Source monitors both CC pins for detach and when detected, enters Unattached.SRC		N/A
	DTS DRP monitors VBUS for detach and when detected, enters UnattachedDeb.SNK		N/A
B.2.5.2	DTS Port to non-DAM TS Port Interoperability Behaviors		N/A
	The following sub-sections describe the non-functional port-to-port interoperability behaviors for the various combinations of DTS and TS Sources, Sinks, and DRPs that do not support		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	DAM.		
B.2.5.2.1	DTS Source to non-DAM TS Sink Behavior		N/A
	The following describes the behavior when a DTS Source is connected to a non-DAM TS Sink.		N/A
	1. DTS Source and TS Sink in the unattached state		N/A
	2. DTS Source transitions from UnattachedDeb.SRC to AttachedDeb.SRC through AttachWaitDeb.SRC		N/A
	DTS Source detects the non-DAM TS Sink's pull-downs on both CC pins and enters AttachWaitDeb.SRC. After tCCDebounce it then enters AttachedDeb.SRC		N/A
	DTS Source turns on VBUS		N/A
	3. Non-DAM TS Sink transitions from Unattached.SNK to AttachWait.SNK.		N/A
	Non-DAM TS Sink in Unattached.SNK detects the DTS Source's pull-ups on both CC pins and enters AttachWait.SNK.		N/A
	Non-DAM TS Sink continues to detect pull-ups on both CC pins and stays in AttachWait.SNK because it does not support DAM (will not enter Attached.SNK because it does not detect SNK.Open on either pin)		N/A
	4. While the DTS Source and non-DAM TS Sink are in their final state:		N/A
	DTS Source adjusts Rp as needed for offered current		N/A
	Non-DAM TS Sink may draw USB default current from DTS Source as permitted by Section 4.5.2.2 but will not enter DAM		N/A
	DTS Source monitors both CC pins for detach and when detected, enters UnattachedDeb.SRC		N/A
	Non-DAM TS Sink monitors both CC pins for detach and when detected, enters Unattached.SNK		N/A
B.2.5.2.2	DTS Source to non-DAM TS DRP Behavior		N/A
	The following describes the behavior when a DTS Source is connected to a non-DAM TS DRP.		N/A
	1. DTS Source and non-DAM TS DRP in the unattached state		N/A
	Non-DAM TS DRP alternates between Unattached.SRC and Unattached.SNK		N/A
	2. DTS Source transitions from UnattachedDeb.SRC to AttachedDeb.SRC through AttachWaitDeb.SRC		N/A
	DTS Source detects the non-DAM TS Sink's pull-downs on both CC pins and enters AttachWaitDeb.SRC. After tCCDebounce it then enters AttachedDeb.SRC		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	DTS Source turns on VBUS		N/A
	3. Non-DAM TS DRP transitions from Unattached.SNK to AttachWait.SNK.		N/A
	Non-DAM TS DRP in Unattached.SNK detects the DTS Source's pull-ups on both CC pins and enters AttachWait.SNK.		N/A
	Non-DAM TS DRP continues to detect pull-downs on both CC pins and stays in AttachWait.SNK because it does not support DAM (will not enter Attached.SNK because it does not detect SNK.Open on either pin)		N/A
	4. While the DTS Source and non-DAM TS DRP are in their final state:		N/A
	DTS Source adjusts Rp as needed for offered current		N/A
	Non-DAM TS DRP may draw USB default current from DTS Source as permitted by Section 4.5.2.2 but will not enter DAM		N/A
	DTS Source monitors both CC pins for detach and when detected, enters UnattachedDeb.SRC		N/A
	Non-DAM TS DRP monitors both CC pins for detach and when detected, enters Unattached.SRC		N/A
B.2.5.2.3	DTS Sink to non-DAM TS Source Behavior		N/A
	The following describes the behavior when a DTS Sink is connected to a non-DAM TS Source.		N/A
	1. Non-DAM TS Source and DTS Sink in the unattached state		N/A
	2. Non-DAM TS Source transitions from Unattached.SRC to AttachWait.SRC		N/A
	Non-DAM TS Source detects the DTS Sink's pull-downs on both CC pins and enters AttachWait.SRC.		N/A
	Non-DAM TS Source continues to detect pull-downs on both CC pins and stays in AttachWait.SRC because it does not support DAM (will not enter Attached.SRC because it does not detect SRC.Rd on only one CC pin)		N/A
	3. DTS Sink transitions from UnattachedDeb.SNK to AttachWaitDeb.SNK.		N/A
	DTS Sink in UnattachedDeb.SNK detects the non-DAM TS Source's pull-ups on both CC pins and enters AttachWaitDeb.SNK		N/A
	DTS Sink remains in AttachWaitDeb.SNK because it does not detect VBUS		N/A
	4. While the non-DAM TS Source and DTS Sink are in their final state:		N/A
	Non-DAM TS Source monitors both CC pins for detach and when detected, enters Unattached.SRC		N/A
	DTS Sink monitors VBUS for attach and both CC pins for detach and enters		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	UnattachedDeb.SNK when both CC pins go to SNK.Open		
B.2.5.2.4	DTS Sink to non-DAM TS DRP Behavior		N/A
	The following describes the behavior when a DTS Sink is connected to a non-DAM TS DRP.		N/A
	1. DTS Sink and non-DAM TS DRP in the unattached state		N/A
	Non-DAM TS DRP alternates between Unattached.SRC and Unattached.SNK		N/A
	DTS Sink in UnattachedDeb.SNK		N/A
	2. Non-DAM TS DRP transitions from Unattached.SRC to AttachWait.SRC		N/A
	Non-DAM TS DRP detects the DTS Sink's pull-downs on both CC pins and enters AttachWait.SRC.		N/A
	Non-DAM TS DRP continues to detect pull-downs on both CC pins and stays in AttachWait.SRC because it does not support DAM (will not enter Attached.SRC because it does not detect SRC.Rd on only one CC pin)		N/A
	3. DTS Sink transitions from UnattachedDeb.SNK to AttachWaitDeb.SNK.		N/A
	DTS Sink in UnattachedDeb.SNK detects the non-DAM TS DRP's pull-ups on both CC pins and enters AttachWaitDeb.SNK		N/A
	DTS Sink remains in AttachWaitDeb.SNK because it does not detect VBUS		N/A
	4. While the non-DAM TS DRP and DTS Sink are in their final state:		N/A
	Non-DAM TS DRP monitors both CC pins for detach and when detected, enters Unattached.SNK		N/A
	DTS Sink monitors VBUS for attach and both CC pins for detach and enters UnattachedDeb.SNK when both CC pin go to SNK.Open		N/A
B.2.5.2.5	DTS DRP to non-DAM TS Sink Behavior		N/A
	The DTS DRP to non-DAM TS Sink behavior follows the flow in Section B.2.5.2.1.		N/A
B.2.5.2.6	DTS DRP to non-DAM TS DRP Behavior		N/A
	The DTS DRP to non-DAM TS DRP behavior follows the flows in Section B.2.5.2.2 and Section B.2.5.2.4 depending on the role forced by the non-DAM TS DRP		N/A
B.2.5.2.7	DTS DRP to non-DAM TS Source Behavior		N/A
	The following describes the behavior when a DTS DRP is connected to non-DAM TS Source.		N/A
	1. DTS DRP and non-DAM TS Source in the unattached state		N/A
	DTS DRP alternates between UnattachedDeb.SRC and UnattachedDeb.SNK		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	Non-DAM TS Source in Unattached.SRC		N/A
	2. DTS DRP transitions from UnattachedDeb.SNK to AttachWaitDeb.SNK		N/A
	DTS DRP in UnattachedDeb.SNK detects pull-ups on both CC pins and enters AttachWaitDeb.SNK		N/A
	3. Non-DAM TS Source transitions from Unattached.SRC to AttachWait.SRC		N/A
	Non-DAM TS Source in Unattached.SRC detects pull-downs on both CC pins and enters AttachWait.SRC		N/A
	Non-DAM TS Source continues to detect pull-downs on both CC pins and stays in AttachWait.SRC because it does not support DAM (will not enter Attached.SRC because it does not detect SRC.Rd on only one CC pin)		N/A
	DTS Sink remains in AttachWaitDeb.SNK because it does not detect VBUS		N/A
	5. While the non-DAM TS Source and DTS DRP are in their final state:		N/A
	Non-DAM TS Source monitors both CC pins for detach and when detected, enters Unattached.SRC		N/A
	DTS DRP monitors VBUS for attach and both CC pins for detach and enters UnattachedDeb.SRC when both CC pin go to SNK. Open		N/A
B.2.5.2.8	DTS Sink to non-DAM TS Sink with Accessory Support Behavior		N/A
	The following describes the behavior when a DTS Sink is connected to a non-DAM USB Type-C TS Sink with Accessory Support.		N/A
	1. DTS Sink and non-DAM TS Sink with Accessory Support ("non-DAM TS Sink" for the remainder of this flow) in the unattached state		N/A
	Non-DAM TS Sink alternates between Unattached.SNK and Unattached.Accessory		N/A
	DTS Sink in UnattachedDeb.SNK		N/A
	2. Non-DAM TS Sink transitions from Unattached.Accessory to AttachWait.Accessory		N/A
	Non-DAM TS Sink detects the DTS Sink's pull-downs on both CC pins and enters AttachWait.Accessory		N/A
	Non-DAM TS Sink continues to detect pull-downs on both CC pins and enters USB Type-C Debug Accessory Mode		N/A
	3. DTS Sink transitions from UnattachedDeb.SNK to AttachWaitDeb.SNK.		N/A
	DTS Sink in UnattachedDeb.SNK detects the non-DAM TS Sinks pull-ups on both CC pins and enters AttachWaitDeb.SNK		N/A
	DTS Sink remains in AttachWaitDeb.SNK because it does not detect VBUS		N/A
	4. While the non-DAM TS DRP and DTS Sink		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
	are in their final state:		
	Non-DAM TS Sink monitors both CC pins for detach and when detected, enters Unattached.SNK		N/A
	DTS Sink monitors both CC pins for detach and enters UnattachedDeb.SNK when both CC pins go to SNK.Open		N/A
<b>B.2.6</b>	<b>Orientation Detection</b>		N/A
	Orientation detection is optional normative. A USB Type-C port supporting Debug Accessory Mode is not required to perform orientation detection. If orientation detection is required, this method shall be followed.		N/A
B.2.6.1	Orientation Detection using Rd and/or Rp Values		N/A
	In this optional normative flow, the DTS shall always initiate an orientation detection sequence, independent of its role as Source, Sink, or DRP. This means that the TS must detect this orientation sequence and perform multiplexing to orient and connect the port signals to the proper channels as well as determine the proper CC pin for USB-PD communication.		N/A
B.2.6.1.1	Orientation Detection with DTS as a Source		N/A
	When the DTS is presenting an Rp, it shall present asymmetric Rp values (Rp1/Rp2) on CC1/CC2 to indicate orientation to the TS. The DTS as a source shall indicate a weaker resistive value on CC2. Table B-2 shows the values of Rp resistance on each CC pin to indicate orientation and advertise the USB Type-C current available on VBUS. See Table 4-24 for the Rp resistance ranges.		N/A
	Once the TS sink enters the DebugAccessory.SNK state, after the vRd on both CC pins is stable for tRpValueChange, it will orient its signal multiplexor based on the detected orientation indicated by the relative voltages of the CC pins. The CC pin with the greater voltage is the plug CC pin, which establishes the orientation of the DTS plug in the TS receptacle and also indicates the USB-PD CC communication wire. The TS Sink cannot perform USB-PD communication or connect any orientation-sensitive debug signals until orientation is determined.		N/A
B.2.6.1.2	Orientation Detection with DTS as a Sink		N/A
	When the DTS is a sink, it shall follow a two-step approach.		N/A
	1. The DTS sink shall present Rd/Rd on the CC pins of the debug accessory plug. This will put the system into debug accessory mode		N/A
	2. Once the DTS sink enters AttachedDeb.SNK		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	state, it shall present a resistance to GND of $\leq R_a$ on B5 (CC2)		
	The asymmetric signaling is detected by the TS Source in the UnorientedDebugAccessory.SRC state. Once Detected, the TS Source will move to the OrientedDebugAccessory.SRC. Once the TS source enters the OrientedDebugAccessory.SRC state, after the SRC.Ra level is detected on one of the CC pins, it will orient its signal multiplexor based on the detected orientation indicated by the relative voltages of the CC pins. The CC pin with the greater voltage is the plug CC pin, which establishes the orientation of the DTS plug in the TS receptacle and also indicates the USB-PD CC communication wire. The TS Source cannot perform USB-PD communication or connect any orientation-sensitive debug signals until orientation is determined.		N/A
<b>B.3</b>	<b>Security/Privacy Requirements:</b>		N/A
	Debug port(s) typically provide system access beyond the normal operation of USB hardware and protocol. Additional protection against unintended use is needed. The design must incorporate appropriate measures to prohibit unauthorized access or modification of the unit under test and to prevent exposure of private user data on the unit under test. The method of protection is not explicitly defined in this specification.		N/A
	The vendor shall assert as part of USB compliance certification that:		N/A
	The device has met the requirement to protect the system's security and user's privacy in its vendor-specific implementation of the port, and		N/A
	The device requires the user to take an explicit action to authorize access to or modification of the unit.		N/A
<b>C</b>	<b>USB Type-C Digital Audio</b>		N/A
<b>C.1</b>	<b>Overview</b>		N/A
	One of the goals of USB Type-C® is to help reduce the number of I/O connectors on a host platform. One connector type that could be eliminated is the legacy 3.5 mm audio device jack. While USB Type-C does include definition of an analog audio adapter accessory (see Appendix A), that solution requires a separate adapter that can be readily lost and the host implementation in support of analog audio is technically challenging. To best serve the user		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	experience, a simplified USB Type-C digital audio solution based on native USB protocol is simpler/more interoperable with both the host platform and audio device being connected directly without the need for adapters and operates seamlessly through existing USB topologies (e.g. through hubs and docks).		
	This appendix is for the optional normative definition of digital audio support on USB Type-C based products. Any USB Audio Class product, having either a USB Type-C plug or receptacle, and whether it is a host system, typically an audio source, and an audio device, typically an audio sink, shall meet the requirements of this appendix in addition to all other applicable USB specification requirements.		N/A
<b>C.2</b>	<b>USB Type-C Digital Audio Specifications</b>		N/A
	USB Type-C Digital Audio (TCDA), when implemented per this specification, shall be compliant with either the USB Audio Device Class 1.0, 2.0 or 3.0 specifications as listed below. While allowed, basing a TCDA on USB Audio Device Class 1.0 is not recommended. Given the number of benefits in terms of audio profile support, simplified enumeration and configuration, and improved low-power operation, use of the USB Audio Device Class 3.0 is strongly recommended.		N/A
	USB Audio Device Class 1.0 including:		N/A
	USB Device Class Definition for Audio Devices, Release 1.0		N/A
	USB Device Class Definition for Audio Data Formats, Release 1.0		N/A
	USB Device Class Definition for Audio Terminal Types, Release 1.0		N/A
	USB Audio Device Class 2.0 including:		N/A
	USB Device Class Definition for Audio Devices, Release 2.0		N/A
	USB Device Class Definition for Audio Data Formats, Release 2.0		N/A
	USB Device Class Definition for Audio Terminal Types, Release 2.0		N/A
	USB Audio Device Class 3.0 including:		N/A
	USB Device Class Definition for Audio Devices, Revision 3.0		N/A
	USB Device Class Definition for Audio Data Formats, Release 3.0		N/A
	USB Device Class Definition for Audio Terminal		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	Types, Release 3.0		
	USB Device Class Definition for Basic Audio Functions, Release 3.0		N/A
	USB Audio Device Class 3.0 specifications now include the definition of basic audio function profiles (Basic Audio Device Definition, BADD). TCDA devices based on USB Audio Device Class 3.0 will implement one of the defined profiles. TCDA-capable hosts based on USB Audio Device Class 3.0 will recognize and typically implement all of the profiles that are relevant to the capabilities and usage models for the host.		N/A
	TCDA devices shall fall into one of the following two configurations:		N/A
	a traditional VBUS-powered USB device that has a USB Type-C receptacle for use with a standard USB Type-C cable, or		N/A
	a VCONN-Powered USB Device (VPD) that has a captive cable with a USB Type-C plug (including thumb drive style products).		N/A
	USB Type-C plug-based TCDA devices shall not be implemented as a variant of the USB Type-C Analog Audio Adapter Accessory (Appendix A).		N/A
<b>D</b>	<b>Thermal Design Considerations for Active Cables</b>		N/A
<b>D.1</b>	<b>Introduction</b>		N/A
	USB Type C® active cables use active circuitry to realize a longer link than passive cables and to maintain the electrical performance at high speed data transmission (USB 3.2 Gen2 single-lane or USB 3.2 Gen1 or Gen2 dual-lane). The additional power dissipation due to active components in the plug over-mold, creates a thermal challenge to passively dissipate power from its active components off limited outer surface area of cable over-mold. Furthermore, the VBUS current, up to 5 A for power delivery, generates joule heat from the conductors along VBUS and GND lines, including copper wires, solder joints, contact pins insides connectors and copper traces on paddle board.		N/A
	This appendix provides some case studies to show the thermal impacts of certain factors affecting the maximum over-mold surface temperature TS such as IC power inside over-mold (PO), thermal boundary, VBUS current level, and port to port spacing. The case study provided is for a specific mechanical design of the cable. When a different mechanical design (geometry or material, etc.) are used, these		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	impacts need further investigation. The methodology of the study is thermal modelling. The modeling results has been validated for some cases (1.5 W PO and 5A VBUS) with lab test results within $\pm 3^{\circ}\text{C}$ , but not for all cases. Note that this appendix is not a full factorial or complete Design of Experiment (DOE) study and whether there is interaction among any of these factors are not covered here.		
	To meet thermal requirements specified in Section 5.2.4.1, as well as the junction temperature TJ requirement of any active components, an active cable should be carefully designed to facilitate the desired heat flow paths. A desirable thermal resistance between powered IC to over-mold surface is achieved when neither TS nor TJ exceeds their specifications. This appendix focuses solely on TS as output of the study, as the TJ requirement varies depending on the IC requirements.		N/A
	It is recommended that system integrator such as host or device designer should take into consideration the heat transferred to or from an active cable in the system level thermal analysis.		N/A
<b>D.2</b>	<b>Model</b>		N/A
<b>D.2.1</b>	<b>Assumptions</b>		N/A
	A system model was built which includes a half active cable with one over-mold on the end, a mated pair of connectors (plug and receptacle) and a motherboard as its host or device side thermal boundary. The model assumes the cable is symmetric with VCONN power to be equally divided and each end of cable consumes half of VCONN power for the active components.		N/A
	It is a Computational Fluid Dynamics (CFD) model with heat transfer of conduction, natural convection and radiation. Emissivity of the plug over-mold and cable jacket is assumed to be 0.92 and the connector metal surfaces is assumed to be 0.05.		N/A
<b>D.2.2</b>	<b>Model Architecture</b>		N/A
	The specific system and cable architecture used in the model is shown below.		N/A
	The simplified cable model uses a pure copper cable, representing a typical short active cable, with total cross section of the copper conductors being about 3.8 mm <sup>2</sup> .		N/A
	The cable model incorporates a plastic boot for the over-mold which allows a higher surface temperature threshold than some other materials such as metal or glass. The over-		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
	mold length in the study was 35 mm.		
	In this specific cable design, two active components are surface mounted on plug PCB (or paddle board). Thermal Interface Material (TIM) are placed between "hot components" and "heat spreading material" such as metal housings to reduce thermal resistance between component junctions to ambient. Metal shells help to reduce TS by spreading heat across the over-mold surface and avoid hot spots.		N/A
	The plug PCB and motherboard are assumed to be FR4 based material. The motherboard is a bulk model assumed to be at a constant temperature without a point heat source on it. The receptacle is top mounted on the motherboard in single port and horizontal stacked cases, Figure D-6; and is vertically mounted in vertical stack up cases, Figure D-4 and Figure D-5.		N/A
<b>D.2.3</b>	<b>Heat Sources</b>		N/A
	Main heat sources include:		N/A
	Active component power such as re-timer, voltage regulator, etc.; the overall power inside over-mold is PO, which is about half of VCONN power consumed by the full cable.		N/A
	Joule heat from the any conductor that carries high current, e.g. raw cable VBUS and GND copper wire, the plug PCB copper traces, contact pins of connectors, etc.		N/A
<b>D.2.4</b>	<b>Heat Flow</b>		N/A
	The main power sources and heat flow paths are illustrated in Figure D-3. The overall heat generated from the cable is mainly dissipated from over-mold surfaces, cable jacket and path to motherboard. The higher thermal resistance of one heat path, the more heat it will "push off" to other heat paths and the more risk that active component junction is overheated. Since heat flow to motherboard is not a desired path from the perspective of system design, cable and over-mold design are critical to achieve balanced heat dissipation paths so not to violate either TS or TJ requirements.		N/A
<b>D.3</b>	<b>USB 3.2 Single Lane Active Cable</b>		N/A
	Based on the assumption that VCONN power consumption is equally split between two ends of the cable and the 1 W maximum VCONN power dissipation in the USB Type-C active cable (See Table 4-5), active component power in each end or over-mold power (PO) can go up to 0.5 W in a USB 3.2 active cable.		N/A
<b>D.3.1</b>	<b>USB 3.2 Single-Lane Active Cable Design Considerations</b>		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	The active cable designer should design for TS less than 30 °C above TA in the condition where thermal boundary TMB is of 25 °C above TA per Section 5.5.4.		N/A
D.3.1.1	USB 3.2 Single-Lane Active Cable in a Single Port Configuration		N/A
	An active cable connected to a single port in a host or device can take full advantage of the overall plug surface area for heat dissipation. Table D-2 shows that when PO is 0.5 W, it is achievable to keep the plug over-mold surface temperature TS of a single cable below the requirement, at both 3 A and 5 A VBUS, assuming the motherboard temperature is no higher than (TA +25) °C.		N/A
D.3.1.2	USB 3.2 Single-Lane Active Cable in a Multiple Port Configuration		N/A
	When multi-port connector spacing is small, there is heat transfer between cables resulting in heat dissipation through natural convection being less effective than in the single port case. Radiation is also less effective due to the proximity of hot surfaces. This section lists a few typical 3-port configurations to show the impacts of receptacle spacing to the thermal performance of an active cable. For Figure D-4 and Figure D-5 minimum spacing center to center is 7 mm; for Figure D-6 it is 12.85 mm.		N/A
D.3.1.2.1	USB 3.2 Single-Lane 3A Active Cable in a 3-Port Configuration		N/A
	When three active cables are stacked up, the port in the center position is usually in the worst situation for heat transfer. Figure D-7 shows the temperature difference between maximum over-mold surface temperature TS of three ports and the ambient temperature TA when three USB 3.2 3A cables are plugged on a 60 °C motherboard in 35°C ambient.		N/A
	In all 3-port configurations shown in Figure D-4, Figure D-5, and Figure D-6, it is achievable to keep the all three plug over-mold surface temperature TS below the requirement, at 3 A VBUS, assuming the motherboard temperature is no higher than (TA +25) °C. Specific cable design should be tested and validated because the margin of center port in VERT and HZ90 is less than 1 °C at minimum port spacing in thermal modeling.		N/A
D.3.1.2.2	USB 3.2 Single-Lane 5A Active Cable in a 3-Port Configuration		N/A
	Figure D-8 shows the temperature difference between maximum over-mold surface temperature TS of three ports and the ambient temperature TA when three USB 3.2 5A cables		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	are plugged on a 60 °C motherboard in 35 °C ambient.		
	All solid lines indicate the minimum spacing cases and dash lines the enlarged spacing cases. Center port is the worst case in all configurations. Three 5A cables at VERT and HZ90 configurations at minimum spacing could exceed the (TA +30 °C) specification by up to 5 °C. HORZ configuration marginally meet spec on side ports but failed on center port.		N/A
	Enlarging spacing between ports greatly reduce TS. Especially in HZ90 configuration, spacing from 7 mm to 15 mm reduced TS by about 8 °C.		N/A
<b>D.4</b>	<b>Dual-Lane Active Cables</b>		N/A
	USB 3.2 defines two lanes of SuperSpeed USB data and in dual-lane operation typically has higher active component power consumption than USB 3.2 single-lane Gen2 active cables.		N/A
	Higher power could heat up the over-mold and raise TS above user comfort zone when plugging or unplugging the cable.		N/A
	USB 3.2 dual-lane active cable may consume up to 1.5 W of power from VCONN. This compares with the 1 W allowed for USB 3.2 single-lane active cables.		N/A
	Section D.4.1 shows TS resulting from 0.75 W over-mold power PO in a 1.5 W dual-lane USB 3.2 active cable for a certain design, in both single-port and multiple-port configurations. Results reveals that thermal solution is necessary to meeting cable design requirements especially in multiple-port configuration.		N/A
	Both over-mold power PO and thermal boundary of the cable TMB have impacts on TS. The correlation of three are studied in Section D.4.1.2 which helps system and cable designer to take both factors into consideration.		N/A
<b>D.4.1</b>	<b>USB 3.2 Dual-Lane Active Cable Design Considerations</b>		N/A
	The cable designer should design for TS of the over-mold less than 30 °C above TA in the condition where thermal boundary TMB is of 25 °C above TA per Section 5.5.4.		N/A
<b>D.4.1.1</b>	<b>USB 3.2 Dual-Lane Active Cable in a Single Port Configuration</b>		N/A
	An active cable connected to a single port in a host or device can take full advantage of the overall plug surface area for heat dissipation. Table D-3 shows that when PO is 0.75 W, it is achievable to keep the plug over-mold surface temperature TS of a single cable below (TA +30) °C at both 3 A and 5 A VBUS, assuming		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	the motherboard temperature is no higher than $(T_A + 25) ^\circ\text{C}$ .		
	In 5 A VBUS case, TS is much closer to specified limit than 3 A VBUS case (Section D.3.1.1), so test and verification of thermal design is highly recommended.		N/A
D.4.1.2	Impact of Over-mold Power PO and Thermal Boundary Temperature TMB		N/A
	In Figure D-9, the area under graph indicate the combination of over-mold power PO and thermal boundary temperature TMB that can achieve $TS < (T_A + 30) ^\circ\text{C}$ in a single port configuration in a 3 A VBUS application.		N/A
	In Figure D-10, the area under graph indicate the combination of over-mold power PO and thermal boundary temperature TMB that can achieve $TS < (T_A + 30) ^\circ\text{C}$ in a single port configuration in a 5 A VBUS application.		N/A
D.4.1.3	Dongle Cable		N/A
	When overall active component power is higher than the maximum over-mold power PO that could meet TS requirement, cable may be re-designed to move the thermal load away from the USB Type-C plug over-mold such as in a dongle cable as illustrated in Figure D-11.		N/A
	The cable should be designed so that the over-mold directly plugged in the host or device dissipates no more than maximum PO and extra heat is migrated to another part of the cable such as a dongle, so neither extra heat will flow into host and device, nor over-mold surface temperature is too hot for users to touch.		N/A
D.4.2	<b>USB 3.2 Dual-Lane Active Cable in a Multi-Port Configuration</b>		N/A
	Multi-port connector spacing results in less effective heat dissipation by natural convection and radiation. This section lists a few typical 3-port configurations to show the impacts of receptacle spacing to the thermal performance of USB 3.2 active cables. Naming of configurations used in this section are the same as in Section D.3.1.2.		N/A
D.4.2.1	USB 3.2 Dual-Lane 3A Active Cable in a 3-Port Configuration		N/A
	Figure D-12 shows the temperature difference between maximum over-mold surface temperature TS of three ports and the ambient temperature TA when three USB 3.2 dual-lane 3A VBUS and 1.5 W cables are plugged on a $60 ^\circ\text{C}$ motherboard in $35 ^\circ\text{C}$ ambient. The port in the center position is usually in the worst situation for heat transfer.		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	All solid lines indicate the minimum spacing cases and dash lines the enlarged spacing cases. Center port is the worst case in all configurations. TS of center port in VERT and HZ90 configurations at minimum spacing could be more than 6 °C over the (TA +30 °C) specification and in HORZ configuration about 2 °C over specification.		N/A
	Enlarging spacing between ports could greatly reduce TS. Especially in HZ90 configuration, spacing from 7 mm to 15 mm reduced TS by about 11 °C, which help to reduce TS to meet specification.		N/A
D.4.2.2	USB 3.2 Dual-Lane 5A Active Cable in a 3-Port Configuration		N/A
	Figure D-13 shows the temperature difference between maximum over-mold surface temperature TS of three ports and the ambient temperature TA when three USB 3.2 dual-lane 5 A VBUS and 1.5 W cables are plugged on a 60 °C motherboard in 35 °C ambient. The TS port in the center position is still the highest of all three in all cases.		N/A
	In all 3-port configurations listed in Figure D-4, Figure D-5, and Figure D-6, plug over-mold surface temperature TS of all three ports have exceeded the requirement, at 5 A VBUS, assuming the motherboard temperature is at (TA +25) °C. TS of center port in VERT and HZ90 configurations at minimum spacing are the highest, near 12 °C over the (TA +30 °C) specification and in HORZ configuration about 6 °C over specification.		N/A
	Enlarging spacing between ports could help reduce TS. The largest reduction is seen in HZ90 configuration, which is near 12 °C and it brings TS back close to target, when spacing is enlarged from 7 mm to 15 mm. However, when port spacing is not sufficient to bring TS down to desired range, further design options in cable and host/device should be investigated.		N/A
D.5	<b>USB 3.2 Host and Device Design Considerations</b>		N/A
	Multi-port USB 3.2 systems should follow the connector minimum spacing requirement defined in Section 3.10.2.		N/A
	From heat flow schematics (Section D.2.4), when flow path 1 (over-mold surface dissipation) is less effective due to the limited spacing between cables, more heat would flow to motherboard and cable. It is recommended that system designer evaluate the heat flow to the system in a system level thermal analysis and provide a heat solution at the system level to reduce the motherboard temperature at		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
	these ports if necessary.		
<b>D.5.1</b>	<b>Heat Spreading or Heat Sinking from Host or Device</b>		N/A
	Proper thermal solutions may be needed on host or device to meet cable thermal requirements. Below are examples of placement of thermal interface material on host or device USB Type-C receptacle connector to spread heat or conduct heat away from chassis. This is to help either direct heat away from active components inside cable plug or limit amount of heat from flowing from host or device into the cable plug. Both would prevent the increased junction temperature of active components and increased cable plug surface temperature over the finger touch temperature limit. The heat management solution shown below are not limited to certain type or size.		N/A
<b>D.5.2</b>	<b>Motherboard Temperature Control</b>		N/A
	Motherboard as a thermal boundary for the cable, could impact the thermal performance of cable greatly. Lowered mother temperature especially the area local around the receptacles could help reduce plug surface temperature TS and component junction temperature TJ. See more discussion in Section D.4.1.1.		N/A
<b>D.5.3</b>	<b>Wider Port Spacing for Multi-Port Applications</b>		N/A
	Wider spacing between receptacle connectors, especially when no additional heat sinking is available, is recommended for multiport application. Section D.3.1.2.1 and section D.3.1.2.2 show the impact from adjustment of port spacing.		N/A
<b>D.5.4</b>	<b>Power Policies</b>		N/A
	To be added in a future update.		N/A
<b>E</b>	<b>Alternate Modes</b>		N/A
	All hosts and devices (except chargers and clearly marked charge-through ports) using a USB Type-C® receptacle shall expose a USB interface (minimally USB 2.0). In the case where the host or device optionally supports Alternate Modes:		N/A
	The host and device shall use USB Power Delivery Structured Vendor Defined Messages (Structured VDMs) to discover, configure and enter/exit modes to enable Alternate Modes.		N/A
	The device is strongly encouraged to provide equivalent USB functionality where such exists for best user experience.		N/A
	Where no equivalent USB functionality is		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	implemented, the device shall provide a USB interface exposing a USB Billboard Device Class used to provide information needed to identify the device. A device is not required to provide a USB interface exposing a USB Billboard Device Class for non-user facing modes (e.g., diagnostic modes).		
	As Alternate Modes do not traverse the USB hub topology, they shall only be used between a host connected directly to a device.		N/A
	There are Alternate Mode devices that look like a USB hub – the downstream facing ports of such devices are USB Type-C receptacles that support Alternate Modes. These devices are referred to as Alternate Mode expanders:		N/A
	The Alternate Mode port expander's downstream facing USB Type-C receptacles shall expose a USB 2.0 interface.		N/A
	An Alternate Mode port expander with the capability to pass SuperSpeed USB through its upstream facing port should expose SuperSpeed USB on its downstream facing USB Type-C receptacles.		N/A
<b>E.1</b>	<b>Alternate Mode Architecture</b>		N/A
	The USB Power Delivery Structured VDMs are defined to extend the functionality a device exposes. Only Structured VDMs shall be used to alter the USB functionality or reconfigure the pins the USB Type-C Connector exposes. Structured VDMs provide a standard method to identify the modes a device supports and to command the device to enter and exit a mode. The use of Structured VDMs are in addition to the normal USB PD messages used to manage power. Structured VDMs may be interspersed within the normal USB PD messaging stream, however they shall not be inserted in the middle of an ongoing PD power negotiation.		N/A
	The Structured VDMs consist of a request followed by a response. The response is either a successful completion of the request (ACK), an indication that the device needs time before it can service a request (BUSY), or a rejection of the request (NAK). A host and device do not enter a mode when either a NAK or BUSY is returned.		N/A
	Multiple modes may exist and/or function concurrently. For example, a Structured VDM may be used to manage an active cable at the same time that another Structured VDM is used to manage the device so that both the cable and device are operating in a compatible mode.		N/A
<b>E.2</b>	<b>Alternate Mode Requirements</b>		N/A
	The host and device shall negotiate a USB PD Explicit Contract before Structured VDMs may		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	be used to discover or enter an Alternate Mode.		
	The ACK shall be sent after switching to the Alternate Mode has been completed by the UFP for Enter Mode and Exit Mode requests. See Section 6.4.4 in the USB Power Delivery Specification.		N/A
	If a device fails to successfully enter an Alternate Mode within tAMTimeout then the device shall minimally expose a USB 2.0 interface (USB Billboard Device Class) that is powered by VBUS. If the device additionally supports USB4, then the device should defer exposing a USB 2.0 interface (USB Billboard Device Class) due to an Alternate Mode timeout until the USB4 discovery and entry process has completed (See Section 5.2.2).		N/A
	When a device offers multiple modes, especially where multiple Alternate Mode definitions are needed in order to be compatible with multiple host-side implementations, successfully entering an Alternate Mode may be predicated on only one of the available modes being successfully recognized by a host. In this case, the device is not required to expose but may still expose a USB Billboard Device Class interface to indicate to the host the availability and status of the modes it supports.		N/A
	The host may send an Enter Mode after tAMTimeout. If the device enters the mode, it shall respond with an ACK and discontinue exposing the USB Billboard Device Class interface. The device may expose the USB Billboard Device Class interface again with updated capabilities.		N/A
	The current supplied over VCONN may be redefined by a specific Alternate Mode but the power shall not exceed the current rating of the pin (See Section 3.7.8.4).		N/A
<b>E.2.1</b>	<b>Alternate Mode Pin Reassignment</b>		N/A
	The USB 2.0 data pins (A6, A7) shall remain connected to the USB host controller during entry, while in and during exit of an Alternate Mode except in the case of a direct connect application that remaps A6 and A7. Direct connect applications that remap A6 and A7 through the use of an Alternate Mode shall provide a USB Billboard Class device that is presented if the remapped Alternate Mode is not entered within tAMTimeout.		N/A
<b>E.2.2</b>	<b>Alternate Mode Electrical Requirements</b>		N/A
	Signaling during the use of Alternate Modes shall comply with all relevant cable assembly, adapter assembly and electrical requirements of Chapter 3.		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	Several requirements are specified in order to minimize risk of damage to the SuperSpeed USB transmitters and receivers in a USB host or device when operating in an Alternate Mode:		N/A
	If pin pairs B11, B10 (RX1) and A11, A10 (RX2) are used on a captive cable, they shall be AC coupled either before or in the USB Type-C plug.		N/A
	If pin pairs B11, B10 (RX1) and A11, A10 (RX2) are used on a USB Type-C receptacle, they may be AC coupled and discharged per USB 3.2 before the receptacle.		N/A
	AC coupling on pin pairs A2, A3 (TX1) and B2, B3 (TX2) as defined for SuperSpeed USB signaling per USB 3.2 shall be used for Alternate Mode signaling.		N/A
	Signals being received at the USB Type-C receptacle shall not exceed the value specified for VTX-DIFF-PP in Table 6-18 of the USB 3.2 specification.		N/A
	Direct Connect applications that remap pins A6 and A7 shall place pins A6 and A7 in a hi-Z state before transmitting the USB PD Enter_Mode command to the Sink. The Source shall not enable the alternate use of the A6 and A7 pins until an ACK has been received by the Source. In the event of a failure to enter the Alternate Mode after transmission of the USB PD Enter_Mode command, the Source shall restore pins A6 and A7 to the normative USB 2.0 operation.		N/A
	Direct connect applications shall ensure that any stubs introduced by repurposing the extra D+/D- pair do not interfere with USB communication with compliant hosts that short the pairs of pins together on the receptacle. This can be ensured by placing the Alternate Mode switch close to the plug, by adding inductors to eliminate the stubs at USB 2.0 frequencies, by ACterminating the long stubs to remove reflections at the cost of attenuated signal, or by other means.		N/A
	Direct connect applications shall ensure that any stubs introduced by repurposing the extra D+/D- pair do not interfere with USB communication with compliant hosts that short the pairs of pins together on the receptacle. This can be ensured by placing the Alternate Mode switch close to the plug, by adding inductors to eliminate the stubs at USB 2.0 frequencies, by ACterminating the long stubs to remove reflections at the cost of attenuated signal, or by other means.		N/A
	The AC coupling requirement are the same as defined in the USB 3.2 specification. The TX signals shall be AC coupled within the system		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	before the physical connector. The RX signals may be DC coupled or AC coupled and discharged within the system.		
	It should be noted that the AC coupling capacitor is placed in the system next to the USB Type-C receptacle, so that the system components (the orientation switch, the Alternate Mode selection multiplexer, and other system components) operate within the common mode limits set by the local PHY. This applies, in the SuperSpeed USB operation, to both the transmit path and the receive path within the local system. The receive path is isolated from the common mode of the port partner by the AC coupling capacitors that are implemented on the TX path in the port partner.		N/A
	In the case where the Alternate Mode System is required to implement DC blocking capacitors within the system between active system components and the Alternate Mode connector, then this provides the necessary isolation and further capacitors in the USB Type-C to Alternate Mode adapter cable are not necessary, and may indeed impair signal integrity.		N/A
	The USB Safe State is defined by the USB PD specification. The USB Safe State defines an electrical state for the SBU1/2 and TX/RX for DFPs, UFPs, and Active Cables when transitioning between USB and an Alternate Mode. SBU1/2 and TX/RX must transition to the USB Safe State before entering to or exiting from an Alternate Mode. Table E-1 defines the electrical requirements for the USB Safe State. See the USB-PD Specification for more detail on entry/exit mechanisms to the USB Safe State.		N/A
<b>E.3</b>	<b>Parameter Values</b>		N/A
<b>E.4</b>	<b>Example Alternate Mode - USB DisplayPort™ Dock</b>		N/A
	This example illustrates the use of Structured VDMs to expose and access functionality beyond the basic functionality defined by the USB Type-C Connector. The device uses its USB Type-C connector to make connection when placed in a cradle dock. This example only illustrates the functional connections.		N/A
<b>E.4.1</b>	<b>USB DisplayPort™ Dock Example</b>		N/A
	The cradle dock provides mechanical alignment and attachment in addition to those provided by the USB Type C connector allowing for only one orientation eliminating the need for an orientation MUX in the dock.		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
	The dock and system use USB PD to manage charging and power.		N/A
	The dock uses DisplayPort to drive a DisplayPort-to-HDMI adapter to support connecting an HDMI monitor.		N/A
	The dock has a USB hub that exposes two external USB ports and attached internal USB Devices, e.g. a USB audio Device (a 3.5 mm audio jack), and a USB Billboard Device.		N/A
	The system uses USB PD Structured VDMs to communicate with the dock to discover that it supports a compatible Alternate Mode. The system then uses a Structured VDM to enter the dock mode. Since USB PD is used, it may also be used to negotiate power for the system and dock. In this example, the SuperSpeed USB signals allow the dock to work as a USBOnly dock when attached to a system that does not fully support the dock or even USB PD.		N/A
<b>E.4.2</b>	<b>Functional Overview</b>		N/A
	The following summarizes the behavior resulting from attaching the example USB DisplayPort Dock for three likely host system cases.		N/A
	1. Host system does not support USB PD or supports USB PD without Structured VDMs		N/A
	The host does not support USB PD, or supports USB PD but not Structured VDMs, so it will not look for SVIDs using the Structured VDM method.		N/A
	The host will discover the USB hub and operates as it would when connected to any USB hub.		N/A
	Since the host will not send an Enter Mode command, after tAMTimeout the dock will expose a USB Billboard Device Class interface that the host will enumerate. The host then reports to the user that an unsupported Device has been connected, identifying the type of Device from the USB Billboard Device Class information.		N/A
	2. Host system supports USB PD and Structured VDMs but does not support this specific USB DisplayPort Dock		N/A
	The host discovers the USB hub and operates as it would when connected to any USB hub.		N/A
	The Host looks for SVIDs that it recognizes. The VID associated with this USB DisplayPort Dock may or may not be recognized by the Host.		N/A
	If that VID is recognized by the Host, the Host then requests the modes associated with this VID. The mode associated with this USB		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	DisplayPort Dock is not recognized by the Host. Since the host does not recognize the mode as being supported hence will not send the Enter Mode command, after tAMETimeout the dock will expose a USB Billboard Device Class interface that the host will enumerate. The host then reports to the user that an unsupported Device has been connected, identifying the type of Device from the USB Billboard Device Class information.		N/A
	3. Host system supports this specific USB DisplayPort Dock		N/A
	The Host looks for SVIDs that it recognizes. The VID associated with this USB DisplayPort Dock is recognized by the Host.		N/A
	The Host then requests the modes associated with this VID. The mode associated with this USB/Display Dock is recognized by the Host.		N/A
	Since this mode is recognized as supported, the Host uses the Enter Mode command to reconfigure the USB Type-C receptacle and enter the USB DisplayPort Dock mode.		N/A
	The USB DisplayPort Dock may optionally expose the USB Billboard Device Class interface to provide additional information to the OS.		N/A
<b>E.4.3</b>	<b>Operational Summary</b>		N/A
	The following summarizes the basic process of discovery through configuration when the USB DisplayPort Dock is attached to the Host.		N/A
	1. Host detects presence of a device (CC pins) and connector orientation		N/A
	2. Host applies default VBUS		N/A
	3. Host applies VCONN because the dock presents Ra		N/A
	4. Host uses USB PD to make power contract with the USB DisplayPort Dock		N/A
	5. Host runs the Discover Identify process		N/A
	a. Sends Discover Identity message		N/A
	b. Receives an ACK message with information identifying the cable		N/A
	6. Host runs the Discover SVIDs process		N/A
	a. Sends Discover SVID message		N/A
	b. Receives an ACK message with list of SVIDs for which the Dock device has modes		N/A
	7. Host runs the Discover Modes process		N/A
	a. Sends Discover Modes VDM for the VIDs previously discovered		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	b. Receives an ACK message with a list of modes associated with each VID		N/A
	c. If USB DisplayPort Dock mode not found, dock will timeout and present the USB Billboard Device Class interface and the OS will inform the user of the error - done		N/A
	d. Else		N/A
	8. Host runs the Enter Mode process		N/A
	a. Sends Enter Mode VDM with VID and USB DisplayPort Dock mode		N/A
	b. Receives an ACK message – Host is now attached to the USB DisplayPort Dock and supports DisplayPort signaling to interface additional functions in combination with USB signaling		N/A
	9. Host stays in the USB DisplayPort Dock mode until		N/A
	a. Explicitly exited by an Exit Mode VDM		N/A
	b. System physically disconnected from the USB DisplayPort Dock		N/A
	c. Hard Reset on USB PD		N/A
	d. VBUS is removed		N/A
<b>F</b>	<b>Thunderbolt 3 Compatibility Discovery and Entry</b>		N/A
	The USB4™ specification includes defined support for compatibility between USB4 products that are designed to interoperate with existing Thunderbolt™ 3 (TBT3) products. This appendix documents the normative methodology to discover and enter into TBT3 between two port partners – this methodology relies on Alternate Mode protocol as defined in Appendix E of this specification and the USB Power Delivery specification.		N/A
	Thunderbolt 3 technology is organized into two primary product categories: hosts and devices. Most TBT3 devices include at least one upstream and one downstream port although a TBT3 device may include more than one downstream port in a manner similar to a hub or no downstream ports in a manner similar to a peripheral.		N/A
<b>F.1</b>	<b>TBT3 Compatibility Mode Functional Requirements</b>		N/A
	In order to successfully interoperate with existing TBT3 products, the functional requirements in the following subsections must be met.		N/A
<b>F.1.1</b>	<b>TBT3-Compatible Power Requirements</b>		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	Before two TBT3-compatible port partners can enter TBT3 mode, a USB PD explicit power contract shall be established.		N/A
<b>F.1.2</b>	<b>TBT3-Compatible Host Requirements</b>		N/A
	All TBT3-compatible host ports shall meet the following requirements.		N/A
	Support DRP operation		N/A
	If resolved to a UFP, use USB PD DR_Swap to attempt to switch into the DFP data role when DFP is preferred		N/A
	If resolved to a DFP, do not accept USB PD DR_Swap to remain in the DFP data role when DFP is preferred		N/A
<b>F.1.3</b>	<b>TBT3-Compatible Device Upstream Requirements</b>		N/A
F.1.3.1	Self-Powered Device		N/A
	The TBT3-compatible upstream port of a self-powered device shall meet the following requirements.		N/A
	Support DRP operation		N/A
	Prefer Sink/UFP through the implementation and use of Try.SNK as needed		N/A
	If resolved to a DFP, accept USB PD DR_Swap to switch into the UFP data role		N/A
F.1.3.2	Bus-Powered Device		N/A
	The TBT3-compatible upstream port of a bus-powered device shall meet the following requirements.		N/A
	Support Sink/UFP operation		N/A
	Reject USB PD DR_Swap to remain in the UFP data role		N/A
<b>F.1.4</b>	<b>TBT3-Compatible Device Downstream Requirements</b>		N/A
F.1.4.1	Self-Powered Device		N/A
	The TBT3-compatible downstream stream port of a self-powered device shall meet the following requirements.		N/A
	Support DRP operation		N/A
	Prefer Source/DFP through the implementation and use of Try.SRC as needed		N/A
	If resolved to a DFP, do not accept USB PD DR_Swap and remain in the DFP data role		N/A
F.1.4.2	Bus-Powered Device		N/A
	The TBT3-compatible downstream port of a bus-powered device shall meet the following requirements.		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	Support Sink		N/A
<b>F.1.5</b>	<b>TBT3-Compatible Self-Powered Device Without Predefined Upstream Port Rules</b>		N/A
	A TBT3-compatible device port may behave as either a downstream or upstream port based on its connection state to a TBT3-compatible host as described below.		N/A
	When no TBT3-compatible host is connected, the USB Type-C® ports shall:		N/A
	Prefer to be configured as a UFP		N/A
	Implement and use Try.SNK as needed to get into the UFP state		N/A
	If resolved to a DFP, initiate or accept USB PD DR_Swap to switch to the UFP data role		N/A
	Accept USB PD DR_Swap to switch to the DFP data role		N/A
	When resolved to a UFP, identify this port as being connected to the host		N/A
	Put the remaining downstream ports into the ErrorRecovery state.		N/A
	After a TBT3-compatible host is initially connected, the remaining downstream USB Type-C ports shall:		N/A
	Implement and use Try.SRC as needed to get into the DFP state		N/A
	Issue a Hard Reset if a USB PD DR_Swap is received when both a connection is present, and an Alternate Mode is in place		N/A
	Issue a USB PD DR_Swap to switch to the DFP data role if a connection is present but no Alternate Mode has been entered (this includes performing a disconnect/reconnect on the port)		N/A
	Accept USB PD DR_Swap to switch to the DFP data role if a connection is present but no Alternate Mode has been entered (this includes performing a disconnect/reconnect on the port)		N/A
	When a TBT3-compatible host that was identified as a host is disconnected, the downstream USB Type-C ports shall:		N/A
	Enter the ErrorRecovery state		N/A
	Behave as if no host is connected		N/A
<b>F.1.6</b>	<b>TBT3-Compatible Devices with a Captive Cable</b>		N/A
	TBT3-compatible devices with a captive cable shall respond to USB PD messages both SOP and SOP'.		N/A
<b>F.2</b>	<b>TBT3 Discovery and Entry Flow</b>		N/A
<b>F.2.1</b>	<b>TBT3 Passive Cable Discover Identity</b>		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
	<b>Responses</b>		
<b>F.2.2</b>	<b>TBT3 Active Cable Discover Identity Responses</b>		N/A
<b>F.2.3</b>	<b>TBT3 Device Discover Identity Responses</b>		N/A
<b>F.2.4</b>	<b>TBT3 Discover SVID Responses</b>		N/A
	If the Intel/TBT3 SVID of 0x8087 is not returned in response to the Discover SVID command, a cable is a Non-TBT3 cable.		N/A
	If a Non-TBT3 cable's Product Type is Active Cable, it shall be regarded as not compatible with TBT3, and TBT3 Discovery shall exit.		N/A
	If a Non-TBT3 cable's Product Type is Passive Cable, the USB Highest Speed field in the cable's Passive Cable VDO shall determine TBT3 functionality and speed. If USB Highest speed is "USB4 Gen3", the cable shall be regarded as a TBT3 capable cable at Gen3 performance. If USB Highest speed is "USB 3.2 Gen1" or "USB 3.2/USB4 Gen2", it shall be regarded as a TBT3 capable cable limited to passive Gen2 performance. If USB Highest Speed indicates "USB 2.0-only, No SuperSpeed", TBT3 Discovery shall exit.		N/A
<b>F.2.5</b>	<b>TBT3 Device Discover Mode Responses</b>		N/A
<b>F.2.6</b>	<b>TBT3 Cable Discover Mode Responses</b>		N/A
<b>F.2.7</b>	<b>TBT3 Cable Enter Mode Command</b>		N/A
<b>F.2.8</b>	<b>TBT3 Device Enter Mode Command</b>		N/A
	The values to be used when sending the TBT3 Device Enter Mode command to the SOP of a TBT3 device are determined based on information retained from earlier in the discovery flow as follows:		N/A
	B31 and B30: return the values received in the B31 and B30 fields of the TBT3 Device Discover Mode Response.		N/A
	B26: return the value received in the B26 field of the TBT3 Device Discover Mode Response.		N/A
	B25: return the value received in the B25 field of the TBT3 Device Discover Mode Response.		N/A
	B23: if using a TBT3 cable, return the value received in the B23 field of the TBT3 Cable Discover Mode Response, otherwise set to 0.		N/A
	B22: if using a TBT3 cable, return the value received in the B22 field of the TBT3 Cable Discover Mode Response, otherwise set to 0.		N/A
	B21: if using a TBT3 cable, return the value received in the B21 field of the TBT3 Cable Discover Mode Response, otherwise set to 0.		N/A
	B20...19: if using a TBT3 cable, return the value received in the B20...19 field of the TBT3 Cable Discover Mode Response, otherwise set to 00b.		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	B18...16: if using a TBT3 cable, return the value received in the B18...16 field of the TBT3 Cable Discover Mode Response, otherwise set to 010b.		N/A
<b>F.2.9</b>	<b>TBT3 Cable Functional Difference Summary</b>		N/A
<b>G</b>	<b>Extracting Pulse Response from Sampled Data and Calculating Non-Linearity Noise</b>		N/A
	The following procedure is used to determine the linear fit pulse response and error for Linear Re-Driver (LRD) based cables.		N/A
	1. The transmitter shall be configured to transmit PRBS15 pattern (as defined in USB4 Specification section 4.2.1.3.4).		N/A
	2. Extract the linear fit pulse from the measured waveform using the parameters specified in Table G-1.		N/A
	3. Define an input pattern $x(n)$ to be a single PRBS period of length $N_{seq}$ and an output signal to be the captured waveform $y(n)$ , sampled at $M$ times the signal baud rate.		N/A
	4. Average the captured waveform at intervals of 2 PRBS repetitions ( $2 \cdot N \cdot M$ samples) for filtering out uncorrelated noise.		N/A
	5. Correlate the averaged waveform and the reference input pattern for extracting output signal $y_1(n)$ aligned to the input pattern $x(n)$ ( $N \cdot M$ samples).		N/A
	6. Concatenate the post-cursor input pattern corresponding to the first waveform sample at the left of the input vector $x(n)$ , and the pre-cursor input pattern corresponding to the last waveform sample at the right of the input vector as following:		N/A
	7. Zero pad $x_1(n)$ to yield $x_z(n)$ such that $M-1$ zeros are inserted between each adjacent entry, before the first entry and after the last entry of $x_1(n)$ .		N/A
	8. Present the output signal $y_1(n)$ as the convolution of $x_z(n)$ and FIR filter $h(n)$ containing $N_{taps} \cdot M$ coefficients:		N/A
	9. Extract the filter $h$ coefficients by applying least-squares fitting:		N/A
	where the superscript "T" denotes the matrix transpose operation.		N/A
	10. Extract the linear fitting error waveform:		N/A
	11. Since $ee$ has $M$ phases, need to calculate $ee$ for each phase.		N/A
	a. Align the $ee$ vector to be in length of $M \cdot N$		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
<b>H</b>	<b>USB PD High-Voltage Design Considerations</b>		N/A
	This appendix considers the impact of having higher voltages across the USB Type-C interface. It addresses contact lifetime and product safety when the USB Type-C cable gets unplugged while high-voltage operation is still enabled. It is applicable for the USB Power Delivery defined Extended Power Range (EPR) voltages (28 V – 48 V) and the Standard Power Range (SPR) at 20 V when supply current is high.		N/A
<b>H.1</b>	<b>Potential for Arcing Damage During Cable Withdrawal</b>		N/A
	The following conditions can result in arcing when the cable is withdrawn:		N/A
	1. Source		N/A
	Voltage regulation when the load is suddenly removed.		N/A
	2. Sink		N/A
	Length of time for the Sink to hold the voltage on its VBUS contact.		N/A
	3. Cable		N/A
	The inductive kick on VBUS occurring in sub-100 ns.		N/A
	Ringings on VBUS occurring in microseconds.		N/A
	The loss of IR voltage drop from the source to the plug due to load removal occurring in 0.1 to 1 $\mu$ s.		N/A
	An arc can be formed when the voltage difference between the Source and Sink across the gap between connector contacts is as low as 12 volts. The arcing voltage of 12 volts only applies within a gap distance of less than 7.5 – 10 $\mu$ m at normal atmospheric pressures. Above this gap distance, the arcing voltage increases significantly. Assuming 12 volts across the entire range provides significant margin for analysis and application.		N/A
<b>H.2</b>	<b>Arcing During USB Type-C Cable Withdrawal</b>		N/A
	There are two separate mechanisms that can create the voltage differential necessary to arc and with enough current can potentially damage contacts through excessive heating.		N/A
	1. Inductive kickback		N/A
	2. Sink discharge		N/A
	Even before either of these mechanisms occur, there is initial heating because of all the current being channeled through a very small contact		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	point where the power density creates enough heat to potentially melt metal.		
	Inductive Kickback		N/A
	The first arcing mechanism is due to inductive kickback which can readily create a voltage delta of 12 volts or more. This event starts at contact break and lasts less than approximately 100 ns. Inductive kickback induced arcing occurs at any VBUS voltage – it happens regardless of the starting DC voltage on VBUS. This arcing has not been seen to cause long term damage to USB Type-C cables in the past as the current is likely too low to super heat the metal (beyond forming a temporary micron-sized molten bridge) to a point where it is permanently destructive. Calculating the energy of the inductive arc as $\frac{1}{2} Li^2$ results in approximately 5 $\mu$ joules which is too low of an energy to damage the metal and correlates well with observation over the lifetime of USB Type-C connections in practice.		N/A
	Sink Discharge		N/A
	The second mechanism creating a voltage differential that can result in arcing is due to the discharge of the voltage at the Sink-side VBUS contact while the Source-side VBUS contact remains high. This arcing mechanism is the one with the most potential to create and sustain an arc at high enough current to heat and damage the connector contacts.		N/A
	This analysis will assume that the disconnect occurs at the Sink end of a cable, but a disconnect at the Source end has the same effect.		N/A
	When the disconnect occurs, the Source will continue to supply power until it detects that the Sink has been disconnected which may take up to 650 ms (tVBUSOFF). The VBUS contact voltage on the Source-side may quickly ( $\sim 1 \mu$ s) step up in voltage due to load regulation and the elimination of any IR voltage drop through the cable. At the same time, the Sink-side contact voltage will discharge due to the load current until the Sink detects the disconnect and removes the load. This creates a voltage difference that is increasing in time.		N/A
	The withdrawal velocity is a factor in whether an arc will occur or not. If it is fast enough, then there is insufficient time to reach the voltage differential needed to form an arc. In practice, the withdrawal rate may not always be fast enough to keep the differential voltage below the threshold of arcing. In essence, there is a race between the contacts reaching a safe distance such that arcing will not occur at the		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	voltages within the USB Type-C range and the voltage differential between the pins reaching the arcing voltage of 12 V.		
	In Figure H-2, the graph shows the voltage difference $V_P - V_R$ reaching the potential arcing voltage $V_{Arc}$ before the contact separation $d_S$ reaches the safe distance $d_{Safe}$ . This would result in an arc forming and damaging the pins if the current is sufficient.		N/A
	The calculated energy of this event if $V_{Arc}$ is 15 Volts for example for 1 ms would result in 75 milli-joules which will boil the surface of the contacts resulting in significant damage.		N/A
<b>H.3</b>	<b>Mitigating Arcing Damage During Cable Withdrawal Due to Sink Discharge</b>		N/A
	The goal of arcing mitigation is not necessarily to entirely prevent arcing but to prevent damage to the connector pins due to arcing that may still occur. An arc may occur without damaging the connector pins if the energy of the arcing is sufficiently low. Experimental data suggests that arcing with a current less than 1 A does not generate enough heat to damage the connector pins.		N/A
	To mitigate arcing damage due to Sink discharge, the voltage between the disconnected contacts must not reach the arcing voltage of 12 volts until the distance between the contacts reaches a safe distance or the current sinking capability of the Sink must be sufficiently low at the time of arcing. The actual arcing voltage increases significantly as the gap distance increases and is not constant and has been seen to range from 12 volts at 0 $\mu\text{m}$ gap distance to as high as 300 volts with a gap distance of 7.5 – 10 $\mu\text{m}$ . Assuming the minimum of 12 volts throughout gives margin and is a practical design target. Likewise, the safe distance is somewhere between 7.5 – 10 $\mu\text{m}$ therefore assuming 20 $\mu\text{m}$ for the following analyses gives plenty of margin.		N/A
	To help mitigate arcing due to Sink discharge, the Sink should manage the discharge slew rate in combination with detecting the disconnection and internally disconnecting its load. Given that it is practical, a Sink design could solely focus on limiting the slew rate to a safe level versus designing with a functional balance between the load capacitance and the time needed to detect the disconnect and remove the device's primary load. However, unplug speed and resulting distance by a human is statistical. This means that the extraction speed has a statistical chance to be very slow relative to the discharge time and has		N/A



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Clause	Requirement + Test	Result - Remark	Verdict
	a statistical chance to stop at an unsafe distance. This means that there will always be observed arcing with enough unplug events.		
	The best approach is to limit the Sink discharge rate so that an arcing voltage will not be reached. While limiting the discharge speed in the Sink does mitigate the chance of an arc by itself, it should be used in conjunction with removing the load current. Both approaches are discussed in the follow examples.		N/A
<b>H.3.1</b>	<b>Limiting Sink Discharge Rate</b>		N/A
	The slew rate of the Sink VBUS discharge is set by the max load current in the Sink and the bulk capacitance on VBUS in the Sink. Increasing the bulk capacitance slows the discharge rate. With some limited testing, the disconnect velocity of a properly designed USB Type-C connector with retention springs has been observed to be as slow as 90 mm/s. It is assumed that there will be little degradation over lifetime due to the required minimum breaking force of the connector. The time to reach the safe distance $d_S$ of 20 $\mu\text{m}$ with a breaking velocity of 90 mm/s is 220 $\mu\text{s}$ . For the timing requirement in Section 4.6.2.6, 250 $\mu\text{s}$ is specified therefore in this analysis, the Sink must not discharge at a rate such that 12 V is reached before 250 $\mu\text{s}$ after disconnect.		N/A
	In this second example, the Sink Bulk Capacitance to prevent the arcing voltage from being reached before the contacts are at a safe distance is 194 $\mu\text{F}$ .		N/A
	Note, due to the nature of USB PD contracts, the starting differential voltage between the contacts $V_{Dis}$ at disconnect increases with increasing nominal or variable contract. This results in the $dV_{max}$ being lower as contract voltage gets higher. Thus, higher contract voltages will need to slow down the slew rate with higher $C_{Bulk}$ or lower $I_{Load}$ .		N/A
<b>H.3.2</b>	<b>Load Removal</b>		N/A
	Quickly detecting the disconnect and reducing the Sink's primary load is an alternative to simply relying on managing the slew rate via adjusting the load capacitance. Based on the Sink requirements given in Section 4.6.2.6, the method analysis that follows is for detecting disconnect by the Sink based on monitoring the VBUS voltage for a drop to below the defined value for $v_{SinkDisconnectPD}$ and disconnecting the Sink's primary load to reduce the current that flows through the arc if an arc occurs.		N/A
	In this example, three timings are introduced. $t_{Det}$ is the time from disconnect to reaching the		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	minimum detection voltage. $t_{Dis}$ is the remaining time for the Sink VBUS to discharge after reaching the minimum detection voltage $t_{Det}$ . The sink must remove the load current within $t_{Dis}$ to stop the discharge before the differential voltage between the contacts reaches $V_{Arc}$ . $t_{Hold}$ is the remaining time the discharge of VBUS must be halted or reduced such that $V_{Arc}$ is not reached until $t_{Safe}$ has expired.		
	In this case, $C_{Bulk}$ is chosen to be lower than the previously calculated minimum bulk capacitance to prevent arcing by slow discharge.		N/A
	Based on this maximum slew rate, the sum of ( $t_{Det} + t_{Dis}$ ) can be calculated. The voltage detector and load disconnect switch can vary by implementation but the sum of these two processes need to occur within this calculated total.		N/A
	In this example, to prevent arcing when the bulk capacitance is 20 $\mu F$ , which is not enough to keep the differential voltage between the contacts from reaching the arcing voltage $V_{Arc}$ before the contacts reach a safe distance, the load must be removed within 33 $\mu s$ after VBUS contacts start to disconnect and must be held from reaching the arcing voltage for another 217 $\mu s$ .		N/A
	B. Example of preventing arcing by load removal for a USB PD EPR 48V contract operating at 48 V with a max 5 A load current:		N/A
	In this example, the analysis is essentially the same as the first example but using the highest voltage request for the given EPR voltage range, in this case 48 volts. In this example, the bulk capacitance used has been increased to better illustrate balancing the mitigation approach between limiting Sink discharge rate and Sink load removal.		N/A
	With all other parameters and assumptions remaining the same, the follow adjustments are made:		N/A
	The slew rate in this example assumes the bulk capacitance is 100 $\mu F$ resulting in the load removal to be completed within 109.0 $\mu s$ and the needed hold time of 141.0 $\mu s$ .		N/A
	If the bulk capacitance were to be increased to 194 $\mu F$ as calculated in the limiting Sink discharge rate Example B in Section H.3.1, the slew rate would decrease to 25.8 mV/ $\mu s$ resulting in the load removal needing to be completed within 211.2 $\mu s$ and the hold time decreased to 38.8 $\mu s$ .		N/A
<b>H.3.3</b>	<b>Limiting Source Current Capability</b>		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	To further aid in mitigating the chance of damage from an arc, the Source should monitor for disconnect and remove the sourcing capability as well as source bulk capacitance as quickly as possible. Since the source does not have a mechanism to see the sink-side voltage, it has no direct way to determine when it should have the source and bulk capacitance disconnected from VBUS. The faster the removal of the source and bulk capacitance, the less chance there is for damage from an arc.		N/A
	The simplest mechanism for detecting the disconnect is the defined monitoring of the CC voltage. Note, when the source is transmitting USB PD traffic, it cannot detect the disconnect with the CC voltage until the transmitted packet is finished. USB PD transmission from the source should be a relatively low percentage of connect time resulting in a statistically low chance of hitting this scenario. Combined with the Sink properly removing the load current for arc mitigation further reduces the chance. Another mechanism for detecting disconnect would be to monitor the load drop on VBUS. A disconnect load drop is much faster than the allowed load step from a sink defined in USB PD. Detection circuitry can be added that distinguishes the faster load drop such that the disconnect can be detected during USB PD traffic transmission.		N/A

## **GRL-USB-PD Compliance Test Solution**

### **DUT Information**

**Manufacturer** : Shenzhen Huafurui Technology Co., Ltd.  
**Model** : KINGKONG POWER 5  
**Serial No.** :

### **Test Information**

**Test Lab** : Shenzhen TCT Testing Technology Co., Ltd.  
**Test\_Engineer** : Kevin Li  
**Remarks** : Remarks  
**Date** : 2025\_02\_14

### **Environment Information**

Parameter	Value
GRL_USB_PD_Controller_Serial_No	GRL-C2-EPR-2022070
GRL_USB_PD_Software_Version	1.6.27.0
GRL_USB_PD_Firmware_Version	1.2.61
GRL USB-PD Ethernet Buffer Size	62K
GRL USB-PD Eload Firmware Version	1.5 / 1.5
GRL USB-PD PPS Firmware Version	4.0 / 4.0
Board Calibration	Calibration Success
RX mask Power selection	Neutral Power
Device_Type	DRP

Parameter	Value
Cable Type	GRL_SPL_EPR_CABLE_1
Impedance (milli ohm)	1
PD_Merged CTS Version	v.Q4-2024
FUNCTIONAL_TESTS CTS Version	v0.90
VIF_File_Name	AWINIC_AW35615PFCR_REV-1.0_1.0_DRP(1).xml
Noise Pattern Generation:	Two-Tone Noise
Application mode	Compliance

### **Power Delivery 3.1 Tests Information**

Parameter	Value
Connect EPR Test Fixture	False
FR_Swap AUTO Box Connected	False

### **USB-C Functional Tests Information**

Parameter	Value	Parameter
Connect EPR Test Fixture	False	
FR_Swap AUTO Box Connected	False	
Enable USB Data validation	Enabled	
Is Dead Battery connected to PUT	Enabled	
Number of USB Type-C Ports	0	
Number of USB Type-B or Micro-B Ports or Type-A plug	0	
Connected Hub is Embedded	Disabled	



**Device Info Capabilities**

Parameter	Vendor Info File	Get Capabilities
Port_Label	0	
Connector_Type	Type-C	
USB4_Supported	NO	
USB_PD_Support	YES	
PD_Port_Type	DRP	
Type_C_State_Machine	DRP	
Port_Battery_Powered	YES	
BC_1_2_Support	Portable Device	
Captive_Cable	NO	
PD_Spec_Revision_Major	3	
PD_Spec_Revision_Minor	1	
PD_Spec_Version_Major	1	
PD_Spec_Version_Minor	8	
PD_Specification_Revision	Revision 3	
SOP_Capable	YES	
SOP_P_Capable	NO	
SOP_PP_Capable	NO	
SOP_P_Debug_Capable	NO	
SOP_PP_Debug_Capable	NO	
Manufacturer_Info_Supported_Port	YES	
Manufacturer_Info_VID_Port	29CF	
Manufacturer_Info_PID_Port	5081	
Chunking_Implemented_SOP	YES	
Unchunked_Extended_Messages_Supported	NO	
Security_Msgs_Supported_SOP	NO	
Unconstrained_Power	NO	
Num_Fixed_Batteries	1	
Num_Swappable_Battery_Slots	0	
ID_Header_Connector_Type_SOP	USB Type-C Receptacle	
USB_Comms_Capable	YES	
DR_Swap_To_DFP_Supported	YES	

Parameter	Vendor Info File	Get Capabilities
DR_Swap_To_UFP_Supported	YES	
VCONN_Swap_To_On_Supported	NO	
VCONN_Swap_To_Off_Supported	NO	
Responds_To_Discov_SOP_UFP	YES	
Responds_To_Discov_SOP_DFP	YES	
Attempts_Discov_SOP	YES	
Power_Interruption_Available	No Interruption Possible	
Data_Reset_Supported	NO	
Enter_USB_Supported	NO	
Type_C_Can_Act_As_Host	YES	
Type_C_Can_Act_As_Device	YES	
Type_C_Implements_Try_SRC	NO	
Type_C_Implements_Try_SNK	YES	
Type_C_Supports_Audio_Accessory	NO	
Type_C_Is_VCONN_Powered_Accessory	NO	
Type_C_Is_Debug_Target_SRC	YES	
Type_C_Is_Debug_Target_SNK	YES	
RP_Value	Default	
Type_C_Port_On_Hub	NO	
Type_C_Power_Source	Both	
Type_C_Sources_VCONN	NO	
Type_C_Is_Alt_Mode_Controller	NO	
Type_C_Is_Alt_Mode_Adapter	NO	
Product_Total_Source_Power_mW	5000	
Port_Source_Power_Type	Assured	
Host_Supports_USB_Data	YES	
Host_Speed	USB 2	
Host_Contains_Captive_Retimer	NO	
Host_Is_Embedded	YES	
Host_Suspend_Supported	NO	
Is_DFP_On_Hub	NO	
Device_Supports_USB_Data	1	
Device_Speed	USB 2	
Device_Max_USB2_Speed	High Speed	

Parameter	Vendor Info File	Get Capabilities
Device_Contains_Captive_Retimer	NO	
EPR_Supported_As_Src	NO	
FR_Swap_Type_C_Current_Capability_As_Initial_Sink	FR_Swap not supported	
Master_Port	YES	
Has_Invariant_PDOs	YES	
Port_Managed_Guaranteed_Type	Guaranteed Capability	
EPR_Supported_As_Snk	NO	
Accepts_PR_Swap_As_Src	YES	
Accepts_PR_Swap_As_Snk	YES	
Requests_PR_Swap_As_Src	NO	
Requests_PR_Swap_As_Snk	NO	
FR_Swap_Supported_As_Initial_Sink	NO	
XID_SOP	0	
Data_Capable_As_USB_Host_SOP	YES	
Data_Capable_As_USB_Device_SOP	YES	
Product_Type_UFP_SOP	PDUSB Peripheral	
Product_Type_DFP_SOP	PDUSB Host	
DFP_VDO_Port_Number	0	
Modal_Operation_Supported_SOP	NO	
USB_VID_SOP	344F	
PID_SOP	0000	
bcdDevice_SOP	0000	
PD_Power_As_Source	5000	
USB_Suspend_May_Be_Cleared	YES	
Sends_Pings	NO	
Num_Src_PDOs	1 Src PDO	
PD_OC_Protection	NO	
PD_Power_As_Sink	27000	
No_USB_Suspend_May_Be_Set	YES	
GiveBack_May_Be_Set	NO	
Higher_Capability_Set	NO	
FR_Swap_Reqd_Type_C_Current_As_Initial_Source	FR_Swap not supported	
Num_Snk_PDOs	3 Snk PDOs	
Src_PDO_Supply_Type #1	Fixed	

Parameter	Vendor Info File	Get Capabilities
Src_PDO_Peak_Current #1	100% IOC	
Src_PDO_Voltage #1	5000 mV	
Src_PDO_Max_Current #1	1000 mA	
Snk_PDO_Supply_Type #1	Fixed	
Snk_PDO_Voltage #1	5000 mV	
Snk_PDO_Op_Current #1	1300 mA	
Snk_PDO_Supply_Type #2	Fixed	
Snk_PDO_Voltage #2	9000 mV	
Snk_PDO_Op_Current #2	1500 mA	
Snk_PDO_Supply_Type #3	Augmented	
Snk_PDO_APDO_Type #3	Programmable Power Supply (SPR)	
Snk_PDO_Min_Voltage #3	5000 mV	
Snk_PDO_Max_Voltage #3	9000 mV	
Snk_PDO_Op_Current #3	3000 mA	

### **PD\_Merged Result**

SI No	Test ID	Test Name	Test Result
1	TEST.PD.PHY.ALL.1	TEST.PD.PHY.ALL.1 Transmit Bit Rate and the Drift	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet16	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet18	PASS
		Rev3ChkdSnk	PASS
		fBitRateMeas - TEST.PD.PHY.ALL.1#1 >Could find BIST response pattern from UUT.	PASS
		pBitRateMeas - TEST.PD.PHY.ALL.1#2 >Could find BIST response pattern from UUT.	PASS
		tBISTContMode Limits validation - TEST.PD.PHY.ALL.1#3 >Could find BIST response pattern from UUT.	PASS

SI No	Test ID	Test Name	Test Result
		--- 1/1 captures completed	
2	TEST.PD.PHY.ALL.2	TEST.PD.PHY.ALL.2 Transmitter Eye Diagram	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet17	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet19	PASS
		Rev3ChkdSnk	PASS
		fBitRateMeas - TEST.PD.PHY.ALL.2#1	PASS
		Eye diagram-1 >>Valid Protocol response for BIST Request	PASS
		Eye diagram-2 >>Valid BIST response pattern	PASS
		Eye diagram-3 >>Eye diagram plot passed at Mid Crossing Level.	PASS
		pBitRateMeas - TEST.PD.PHY.ALL.2#2	PASS
		Eye diagram-4 >>BIST pattern duration 34.6668586 mS [Limit : (30 ~ 60)ms]	PASS
		BMC_PHY_TX_EYE_5 >>Rise time: Average value = 397.428670 nS Minimum value = 388.373584 nS Maximum value = 404.723317 nS Minimum Limit = 300 ns  Fall time: Average value = 408.557551 nS Minimum value = 401.967286 nS Maximum value = 415.759157 nS Minimum Limit = 300 ns	PASS
		--- 1/1 captures completed	
3	TEST.PD.PHY.ALL.3	TEST.PD.PHY.ALL.3 Collision Avoidance	PASS
		COMMON.PROC.BU.2	PASS

SI No	Test ID	Test Name	Test Result
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet16	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet18	PASS
		Rev3ChkdSnk	PASS
		Alternating 0's and 1's for 200us - TEST.PD.PHY.ALL.3#1	PASS
		Continuous 0's for 195us - TEST.PD.PHY.ALL.3#2	PASS
		--- 1/2 captures completed Please run the test case again	
4	TEST.PD.PHY.ALL.4	TEST.PD.PHY.ALL.4 Bus Idle Detection	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet17	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet19	PASS
		Rev3ChkdSnk	PASS
		Check BusIdle - TEST.PD.PHY.ALL.4#1	PASS
		--- 1/1 captures completed	
5	TEST.PD.PHY.ALL.5	TEST.PD.PHY.ALL.5 Receiver Interference Rejection	PASS
		--- 1/4 captures completed occured while executing test case. Please verify the signal capture and PD messages	
6	TEST.PD.PHY.ALL.6	TEST.PD.PHY.ALL.6 Invalid SOP*	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet17	PASS



SI No	Test ID	Test Name	Test Result
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet19	PASS
		Rev3ChkdSnk	PASS
		Check DUT Response - TEST.PD.PHY.ALL.6#1	PASS
7	TEST.PD.PHY.ALL.7	TEST.PD.PHY.ALL.7 Valid SOP*	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet16	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet18	PASS
		Rev3ChkdSnk >> Check the Test_CheckID 8 assertion in the protocol trace	PASS
		Check BIST Response for SOP - TEST.PD.PHY.ALL.7#2	PASS
		Check BIST Response for SOP1 - TEST.PD.PHY.ALL.7#3	PASS
		Check BIST Response for SOP2 - TEST.PD.PHY.ALL.7#5	PASS
		Check BIST Response for SOP1_Debug - TEST.PD.PHY.ALL.7#7 >UUT went to Detach state.	PASS
8	TEST.PD.PHY.ALL.8	TEST.PD.PHY.ALL.8 Incorrect CRC	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet16	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet18	PASS
		Rev3ChkdSnk >> Check the Test_CheckID 1 assertion in the protocol trace	PASS
		Check Flip 0 on CRC before 4b5b encoding - TEST.PD.PHY.ALL.8#2	PASS
		Check Flip 0 on CRC after 4b5b encoding - TEST.PD.PHY.ALL.8#2	PASS
		Check Flip 0 on payload before 4b5b encoding - TEST.PD.PHY.ALL.8#2	PASS
		Check Flip 0 on payload after 4b5b encoding - TEST.PD.PHY.ALL.8#2	PASS
		Check replace third 5b symbol - TEST.PD.PHY.ALL.8#2	PASS
9	TEST.PD.PHY.ALL.9	TEST.PD.PHY.ALL.9 Receiver Input Impedance	PASS
		COMMON.PROC.BU.2	PASS

SI No	Test ID	Test Name	Test Result
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet16	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet18	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet70	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet72	PASS
		Rev3ChkdSnk	PASS
		Sink UUT voltage on the CC line - TEST.PD.PHY.ALL.9#1 >>CC-line voltage is 1.073V at time 2.40954822s	PASS
		Source UUT voltage on the CC line - TEST.PD.PHY.ALL.9#2	PASS
		Cable Plug voltage on the CC line - TEST.PD.PHY.ALL.9#3	PASS
		Rev3ChkdSnk >> Check the Test_CheckID 4 assertion in the protocol trace	PASS
		Cable Plug voltage on the CC line [Without VCONN or VBUS] - TEST.PD.PHY.ALL.9#5	PASS
10	TEST.PD.PHY.PORT.1	TEST.PD.PHY.PORT.1 Invalid Reset Signals	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet16	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet18	PASS
		Rev3ChkdSnk	PASS
		Check Response message - TEST.PD.PHY.PORT.1#1	PASS
		Check Response message - TEST.PD.PHY.PORT.1#2	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 15.596s and Sourcecap time: 15.776s [PASS] Max = 250ms. Obtained time difference is 179.149ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet189	PASS

SI No	Test ID	Test Name	Test Result
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 38.602ms Packet 191	PASS
		Rev3ChkdSrc	PASS
		Check Response message - TEST.PD.PHY.PORT.1#1	PASS
		Check Response message - TEST.PD.PHY.PORT.1#2	PASS
11	TEST.PD.PROT.ALL.1	TEST.PD.PROT.ALL.1 Corrupted GoodCRC	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk >>SourceCap Packet14	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet16	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet98	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet100	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src	PASS
		First source capability timer - COMMON.PROC.BU.1#1	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3	PASS
		Rev2Snk	PASS
		GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.1#2	PASS
		SinkCap retransmit check - TEST.PD.PROT.ALL.1#5	PASS

SI No	Test ID	Test Name	Test Result
		GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.1#7	PASS
		SinkCap retransmit check - TEST.PD.PROT.ALL.1#10	PASS
		SinkCap retransmit messageID check - TEST.PD.PROT.ALL.1#11 >>Tester sent Get_Sink_Cap message Packet 74 Tester sent Get_Source_Cap message Packet 78	PASS
		UUT SoftReset Check - TEST.PD.PROT.ALL.1#12	PASS
		Rev3ChkdSnk >> Check the Test_CheckID 1 assertion in the protocol trace	PASS
		Rev2Src >> Check the Test_CheckID 1 assertion in the protocol trace	PASS
		Rev3ChkdSrc	PASS
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.1#3	PASS
		SinkCap retransmit check - TEST.PD.PROT.ALL.1#5	PASS
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.1#8	PASS
		SinkCap retransmit check - TEST.PD.PROT.ALL.1#10	PASS
		SinkCap retransmit messageID check - TEST.PD.PROT.ALL.1#11 >>Tester sent Get_Sink_Cap message Packet 74 Tester sent Get_Source_Cap message Packet 78	PASS
		UUT SoftReset Check - TEST.PD.PROT.ALL.1#12	PASS
12	TEST.PD.PROT.ALL.2	TEST.PD.PROT.ALL.2 Soft Reset and Hard Reset	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk >>SourceCap Packet14	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet16	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet113	PASS

SI No	Test ID	Test Name	Test Result
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet115	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION 2 0 Rev2Src	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 17.317s and Sourcecap time: 17.499s [PASS] Max = 250ms. Obtained time difference is 181.649ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet244	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 39.23ms Packet 246	PASS
		COMMON.PROC.BU.1 - REVISION 3 0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 23.802s and Sourcecap time: 23.981s [PASS] Max = 250ms. Obtained time difference is 178.316ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet331	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 39.31ms Packet 333	PASS
		Rev2Snk	PASS
		GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.2#2 >UUT to respond for Get_Sink_Capability message at protocol index 61	PASS
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.2#3	PASS
		GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.2#12 >UUT to respond for Get_Sink_Capability message at protocol index 89	PASS
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.2#13	PASS
		Rev3ChkdSnk	PASS
		GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.2#2 >>UUT sent SinkCap at protocol index#155	PASS
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.2#3	PASS

SI No	Test ID	Test Name	Test Result
		UUT retransmit check - TEST.PD.PROT.ALL.2#5	PASS
		SoftReset from UUT - TEST.PD.PROT.ALL.2#7	PASS
		UUT Response check - TEST.PD.PROT.ALL.2#8 >>UUT sent Request message at protocol index : 167	PASS
		GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.2#12 >>UUT sent SinkCap at protocol index#196	PASS
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.2#13	PASS
		UUT retransmit check - TEST.PD.PROT.ALL.2#15	PASS
		SoftReset from UUT - TEST.PD.PROT.ALL.2#17	PASS
		UUT retransmit check - TEST.PD.PROT.ALL.2#18	PASS
		UUT Hard Reset message check - TEST.PD.PROT.ALL.2#19 >>UUT sent Hard_Reset message Packet 204 [PASS] Max = 6.1ms. Obtained time difference is 1.777ms	PASS
		Rev2Src	PASS
		GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.2#2	PASS
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.2#3 >>UUT is a DRP and sent SinkCap at the protocol index 263	PASS
		UUT retransmit check - TEST.PD.PROT.ALL.2#5	PASS
		SoftReset from UUT - TEST.PD.PROT.ALL.2#9	PASS
		UUT Response check - TEST.PD.PROT.ALL.2#10 >>UUT sent Request message at protocol index : 273	PASS
		GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.2#12	PASS
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.2#13 >>UUT is a DRP and sent SinkCap at the protocol index 282	PASS
		UUT retransmit check - TEST.PD.PROT.ALL.2#15	PASS
		SoftReset from UUT - TEST.PD.PROT.ALL.2#17	PASS
		UUT retransmit check - TEST.PD.PROT.ALL.2#18	PASS
		UUT Hard Reset message check - TEST.PD.PROT.ALL.2#19 >>UUT sent Hard_Reset message Packet 290 Hard_Reset [PASS] Should be obtained between 0 ms 6.1 ms. Obtained time difference is 1.1912 ms	PASS



SI No	Test ID	Test Name	Test Result
		Rev3ChkdSrc	PASS
		GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.2#2	PASS
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.2#3 >>UUT is a DRP and sent SinkCap at the protocol index 350	PASS
		UUT retransmit check - TEST.PD.PROT.ALL.2#5	PASS
		SoftReset from UUT - TEST.PD.PROT.ALL.2#9	PASS
		UUT Response check - TEST.PD.PROT.ALL.2#10 >>UUT sent Request message at protocol index : 359	PASS
		GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.2#12	PASS
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.2#13 >>UUT is a DRP and sent SinkCap at the protocol index 368	PASS
		UUT retransmit check - TEST.PD.PROT.ALL.2#15	PASS
		SoftReset from UUT - TEST.PD.PROT.ALL.2#17	PASS
		UUT retransmit check - TEST.PD.PROT.ALL.2#18	PASS
		UUT Hard Reset message check - TEST.PD.PROT.ALL.2#19 >>UUT sent Hard_Reset message	PASS
		Packet 374 [PASS] Max = 6.1ms. Obtained time difference is 5.879ms	
13	TEST.PD.PROT.ALL.3	TEST.PD.PROT.ALL.3 Soft Reset response	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk >>SourceCap Packet14	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet16	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet124	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet126	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 10.629s and Sourcecap time: 10.807s [PASS] Max = 250ms. Obtained time difference is 178.316ms	PASS

SI No	Test ID	Test Name	Test Result
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet288	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 39.814ms Packet 290	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 15.141s and Sourcecap time: 15.318s [PASS] Max = 250ms. Obtained time difference is 177.482ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet366	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 43.715ms Packet 368	PASS
		Rev2Snk	PASS
		GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.3#2 >>UUT is a DRP and it sent SinkCap message at the protocol index 43	PASS
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.3#3	PASS
		Soft Reset message validation - TEST.PD.PROT.ALL.3#4	PASS
		UUT Request message check - TEST.PD.PROT.ALL.3#5 >>DUT sent Request message at protocol index: 82	PASS
		Source Capabilities message validation - TEST.PD.PROT.ALL.3#6	PASS
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.3#8 >DUT to respond to Get_Sink_Cap	PASS
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.3#9 >DUT to respond to Get_Sink_Cap	PASS
		Rev3ChkdSnk	PASS
		GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.3#2 >>UUT is a DRP and it sent SinkCap message at the protocol index 162	PASS
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.3#3	PASS
		Soft Reset message validation - TEST.PD.PROT.ALL.3#4	PASS
		UUT Request message check - TEST.PD.PROT.ALL.3#5 >>DUT sent Request message at protocol index: 228	PASS
		Source Capabilities message validation - TEST.PD.PROT.ALL.3#6	PASS

SI No	Test ID	Test Name	Test Result
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.3#8 >>DUT responded with SinkCap to Get_Sink_Cap at protocol index : 261	PASS
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.3#9	PASS
		Rev2Src	PASS
		GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.3#2	PASS
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.3#3 >>UUT is a DRP and it sent SinkCap message at the protocol index 307	PASS
		Soft Reset message validation - TEST.PD.PROT.ALL.3#4	PASS
		UUT Request message check - TEST.PD.PROT.ALL.3#5	PASS
		Source Capabilities message validation - TEST.PD.PROT.ALL.3#6 >>SourceCap message at protocol index: 333 received within the 250ms	PASS
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.3#8	PASS
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.3#9 >>DUT responded with SinkCap to Get_Sink_Cap at protocol index : 344	PASS
		Rev3ChkdSrc	PASS
		GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.3#2	PASS
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.3#3 >>UUT is a DRP and it sent SinkCap message at the protocol index 385	PASS
		Soft Reset message validation - TEST.PD.PROT.ALL.3#4	PASS
		UUT Request message check - TEST.PD.PROT.ALL.3#5	PASS
		Source Capabilities message validation - TEST.PD.PROT.ALL.3#6 >>SourceCap message at protocol index: 411 received within the 250ms	PASS
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.3#8	PASS
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.3#9 >>DUT responded with SinkCap to Get_Sink_Cap at protocol index : 422	PASS
14	TEST.PD.PROT.ALL.4	TEST.PD.PROT.ALL.4 Reset Signals and MessageID	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk >>SourceCap Packet14	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet16	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet102	PASS

SI No	Test ID	Test Name	Test Result
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet104	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 10.667s and Sourcecap time: 10.842s [PASS] Max = 250ms. Obtained time difference is 174.983ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet256	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 38.939ms Packet 258	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 15.327s and Sourcecap time: 15.498s [PASS] Max = 250ms. Obtained time difference is 171.649ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet351	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 42.683ms Packet 353	PASS
		Rev2Snk >> Tester sent Hard_Reset message Packet 65	PASS
		Get Sink Cap response check - TEST.PD.PROT.ALL.4#2 >>UUT initiated SinkCap for tester initiated Get_Sink_Capability, at protocol index 47	PASS
		UUT Request check - TEST.PD.PROT.ALL.4#4 >>UUT Responded with Request message at protocol index 69	PASS
		Get Sink Cap response check - TEST.PD.PROT.ALL.4#9 >>UUT initiated SinkCap for tester initiated Get_Sink_Capability, at protocol index 78	PASS
		Get Sink Cap response check - TEST.PD.PROT.ALL.4#11 >>UUT ignored tester initiated Get_Sink_Capability at protocol index 81	PASS

SI No	Test ID	Test Name	Test Result
		Get Sink Cap response check - TEST.PD.PROT.ALL.4#13 >>UUT initiated SinkCap for tester initiated Get_Sink_Capability, at protocol index 86	PASS
		Rev3ChkdSnk >> Tester sent Hard_Reset message Packet 190	PASS
		Get Sink Cap response check - TEST.PD.PROT.ALL.4#2 >>UUT initiated SinkCap for tester initiated Get_Sink_Capability, at protocol index 149	PASS
		UUT Request check - TEST.PD.PROT.ALL.4#4 >>UUT Responded with Request message at protocol index 197	PASS
		Get Sink Cap response check - TEST.PD.PROT.ALL.4#9 >>UUT initiated SinkCap for tester initiated Get_Sink_Capability, at protocol index 211	PASS
		Get Sink Cap response check - TEST.PD.PROT.ALL.4#11 >>UUT ignored tester initiated Get_Sink_Capability at protocol index 219	PASS
		Get Sink Cap response check - TEST.PD.PROT.ALL.4#13 >>UUT initiated SinkCap for tester initiated Get_Sink_Capability, at protocol index 229	PASS
		Rev2Src >> Tester sent Hard_Reset message Packet 297	PASS
		Get Sink Cap response check - TEST.PD.PROT.ALL.4#3 >>UUT is a DRP and sent SinkCap at the protocol index 279	PASS
		HardReset response check - TEST.PD.PROT.ALL.4#5	PASS
		Source Capability timing check - TEST.PD.PROT.ALL.4#6 >>DUT initiate first source cap within 250ms. Obtained time difference is 155.817750000001ms	PASS
		Get Sink Cap response check - TEST.PD.PROT.ALL.4#10 >>UUT is a DRP and sent SinkCap at the protocol index 321	PASS
		Get Sink Cap response check - TEST.PD.PROT.ALL.4#11 >>UUT ignored tester initiated Get_Sink_Capability at protocol index 324	PASS
		Get Sink Cap response check - TEST.PD.PROT.ALL.4#14 >>UUT is a DRP and sent SinkCap at the protocol index 329	PASS

SI No	Test ID	Test Name	Test Result
		Rev3ChkdSrc >> Tester sent Hard_Reset message Packet 392	PASS
		Get Sink Cap response check - TEST.PD.PROT.ALL.4#3 >>UUT is a DRP and sent SinkCap at the protocol index 374	PASS
		HardReset response check - TEST.PD.PROT.ALL.4#5	PASS
		Source Capability timing check - TEST.PD.PROT.ALL.4#6 >>DUT initiate first source cap within 250ms. Obtained time difference is 159.984000000001ms	PASS
		Get Sink Cap response check - TEST.PD.PROT.ALL.4#10 >>UUT is a DRP and sent SinkCap at the protocol index 416	PASS
		Get Sink Cap response check - TEST.PD.PROT.ALL.4#11 >>UUT ignored tester initiated Get_Sink_Capability at protocol index 419	PASS
		Get Sink Cap response check - TEST.PD.PROT.ALL.4#14 >>UUT is a DRP and sent SinkCap at the protocol index 424	PASS
15	TEST.PD.PROT.ALL.5	TEST.PD.PROT.ALL.5 Unrecognized Message	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk >>SourceCap Packet14	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet16	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk	PASS
		UUT should respond with request - COMMON.PROC.BU.2#1	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src	PASS
		First source capability timer - COMMON.PROC.BU.1#1	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS



SI No	Test ID	Test Name	Test Result
		First source capability timer - COMMON.PROC.BU.1#1	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3	PASS
		Rev2Snk >> Check the Test_CheckID 1 assertion in the protocol trace	PASS
		Rev3ChkdSnk >> Check the Test_CheckID 1 assertion in the protocol trace	PASS
		Rev2Src >> Check the Test_CheckID 1 assertion in the protocol trace	PASS
		Rev3ChkdSrc >> Check the Test_CheckID 1 assertion in the protocol trace	PASS
16	TEST.PD.PROT.ALL3.1	TEST.PD.PROT.ALL3.1 Get_Status Response	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet15	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet17	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3UnchkdSnk	PASS
		UUT should respond with request - COMMON.PROC.BU.2#1	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1	PASS

SI No	Test ID	Test Name	Test Result
		DUT responded with accept message - COMMON.PROC.BU.1#2	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3	PASS
		Rev3ChkdSnk	PASS
		Get_Status message response check - TEST.PD.PROT.ALL3.1#3 >>Check the Test_CheckID 2 assertion in the protocol trace	PASS
		Status message field check - TEST.PD.PROT.ALL3.1#4	PASS
		Rev3UnchkdSnk	PASS
		Get_Status message response check - TEST.PD.PROT.ALL3.1#3 >>Check the Test_CheckID 2 assertion in the protocol trace	PASS
		Status message field check - TEST.PD.PROT.ALL3.1#4	PASS
		Rev3ChkdSrc	PASS
		Get_Status message response check - TEST.PD.PROT.ALL3.1#3 >>Check the Test_CheckID 2 assertion in the protocol trace	PASS
		Status message field check - TEST.PD.PROT.ALL3.1#4	PASS
		Rev3UnchkdSrc	PASS
		Get_Status message response check - TEST.PD.PROT.ALL3.1#3 >>Check the Test_CheckID 2 assertion in the protocol trace	PASS
		Status message field check - TEST.PD.PROT.ALL3.1#4	PASS
17	TEST.PD.PROT.ALL3.2	TEST.PD.PROT.ALL3.2 Get_Manufacturer_Info Response	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet15	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet17	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3UnchkdSnk >>SourceCap Packet99	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet101	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS

SI No	Test ID	Test Name	Test Result
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 9.355s and Sourcecap time: 9.53s [PASS] Max = 250ms. Obtained time difference is 174.983ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet183	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 39.92ms Packet 185	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 11.876s and Sourcecap time: 12.055s [PASS] Max = 250ms. Obtained time difference is 179.149ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet224	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 38.841ms Packet 226	PASS
		Rev3ChkdSnk	PASS
		Response Check - TEST.PD.PROT.ALL3.2#2	PASS
		VIF Check - TEST.PD.PROT.ALL3.2#3	PASS
		Rev3UnchkdSnk	PASS
		Response Check - TEST.PD.PROT.ALL3.2#2	PASS
		VIF Check - TEST.PD.PROT.ALL3.2#3 >>DUT responded with Not_Supported message	NA
		Rev3ChkdSrc	PASS
		Response Check - TEST.PD.PROT.ALL3.2#2	PASS
		VIF Check - TEST.PD.PROT.ALL3.2#3 >>DUT responded with Not_Supported message	NA

SI No	Test ID	Test Name	Test Result
		Rev3UnchkdSrc	PASS
		Response Check - TEST.PD.PROT.ALL3.2#2	PASS
		VIF Check - TEST.PD.PROT.ALL3.2#3 >>DUT responded with Not_Supported message	NA
18	TEST.PD.PROT.ALL3.3	TEST.PD.PROT.ALL3.3 Invalid Manufacturer Info Target	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet15	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet17	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3UnchkdSnk >>SourceCap Packet94	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet96	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 8.355s and Sourcecap time: 8.533s [PASS] Max = 250ms. Obtained time difference is 178.316ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet159	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 38.53ms Packet 161	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 10.897s and Sourcecap time: 11.073s [PASS] Max = 250ms. Obtained time difference is 176.649ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet200	PASS

SI No	Test ID	Test Name	Test Result
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 40.044ms Packet 202	PASS
		Rev3ChkdSnk	PASS
		Response Check - TEST.PD.PROT.ALL3.3#2 >DUT packet Getting_Manufacturer_Information, verify the AMS/Protocol capture and confirm at AMS Index #3.	PASS
		Manufacturer String Check - TEST.PD.PROT.ALL3.3#3	PASS
		Rev3UnchkdSnk	PASS
		Response Check - TEST.PD.PROT.ALL3.3#2 >>DUT sent Not_Supported message for the Get_Manufacturer_Info at protocol index #131	PASS
		Manufacturer String Check - TEST.PD.PROT.ALL3.3#3 >>DUT response Not_supported message to the Get_Manufacturer_Info	PASS
		Rev3ChkdSrc	PASS
		Response Check - TEST.PD.PROT.ALL3.3#2 >>DUT sent Not_Supported message for the Get_Manufacturer_Info at protocol index #178	PASS
		Manufacturer String Check - TEST.PD.PROT.ALL3.3#3 >>DUT response Not_supported message to the Get_Manufacturer_Info	PASS
		Rev3UnchkdSrc	PASS
		Response Check - TEST.PD.PROT.ALL3.3#2 >>DUT sent Not_Supported message for the Get_Manufacturer_Info at protocol index #219	PASS
		Manufacturer String Check - TEST.PD.PROT.ALL3.3#3 >>DUT response Not_supported message to the Get_Manufacturer_Info	PASS
19	TEST.PD.PROT.ALL3.4	TEST.PD.PROT.ALL3.4 Invalid Manufacturer Info Ref	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet19	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet21	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3UnchkdSnk >>SourceCap Packet87	PASS

SI No	Test ID	Test Name	Test Result
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet89	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION 3 0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 8.356s and Sourcecap time: 8.532s [PASS] Max = 250ms. Obtained time difference is 175.816ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet174	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 39.374ms Packet 176	PASS
		COMMON.PROC.BU.1 - REVISION 3 0 Rev3UnchkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 10.906s and Sourcecap time: 11.084s [PASS] Max = 250ms. Obtained time difference is 177.482ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet215	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 41.969ms Packet 217	PASS
		Rev3ChkdSnk	PASS
		Response Check - TEST.PD.PROT.ALL3.4#2 >>DUT sent Not_Supported message for the Get_Manufacturer_Info	PASS
		Manufacturer String Check - TEST.PD.PROT.ALL3.4#3	PASS
		Rev3UnchkdSnk	PASS
		Response Check - TEST.PD.PROT.ALL3.4#2 >>DUT sent Not_Supported message for the Get_Manufacturer_Info	PASS
		Manufacturer String Check - TEST.PD.PROT.ALL3.4#3	PASS
		Rev3ChkdSrc	PASS
		Response Check - TEST.PD.PROT.ALL3.4#2 >>DUT sent Not_Supported message for the Get_Manufacturer_Info	PASS
		Manufacturer String Check - TEST.PD.PROT.ALL3.4#3	PASS
		Rev3UnchkdSrc	PASS



SI No	Test ID	Test Name	Test Result
		Response Check - TEST.PD.PROT.ALL3.4#2 >>DUT sent Not_Supported message for the Get_Manufacturer_Info	PASS
		Manufacturer String Check - TEST.PD.PROT.ALL3.4#3	PASS
20	TEST.PD.PROT.ALL3.5	TEST.PD.PROT.ALL3.5 Chunked Extended Message Response	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet16	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet18	PASS
		Rev3ChkdSnk	PASS
		Chunk Response - TEST.PD.PROT.ALL3.5#2 >>Check the Test_CheckID 1 assertion in the protocol trace	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3	PASS
		Rev3ChkdSrc	PASS
		Chunk Response - TEST.PD.PROT.ALL3.5#2	PASS
21	TEST.PD.PROT.ALL3.6	TEST.PD.PROT.ALL3.6 ChunkSenderResponseTimer Timeout	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet15	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet17	PASS
		Rev3ChkdSnk	PASS

SI No	Test ID	Test Name	Test Result
		Chunk Response - TEST.PD.PROT.ALL3.6#2 >>UUT respond with Reserved message for the Tester initiated Chunk extended message at protocol index: 52 [PASS] UUT sent request for Data block Obtained time difference is 3.226ms, Expected time limit 0ms to 15ms	PASS
		Chunk message field check - TEST.PD.PROT.ALL3.6#3 >>DUT responded with Reserved message for Reserved message. Actual time interval is: 0.633ms	PASS
		Response Check - TEST.PD.PROT.ALL3.6#5 >>DUT responded with Reserved message for Reserved message. Actual time interval is: 8.693ms	PASS
		Message Header and Extended Message Header - TEST.PD.PROT.ALL3.6#6	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 4.058s and Sourcecap time: 4.234s [PASS] Max = 250ms. Obtained time difference is 175.816ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet155	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 38.942ms Packet 157	PASS
		Rev3ChkdSrc	PASS
		Chunk Response - TEST.PD.PROT.ALL3.6#2 >>UUT respond with Reserved message for the Tester initiated Chunk extended message at protocol index: 174 [PASS] UUT sent request for Data block Obtained time difference is 2.529ms, Expected time limit 0ms to 15ms	PASS
		Chunk message field check - TEST.PD.PROT.ALL3.6#3 >>DUT responded with Reserved message for Reserved message. Actual time interval is: 0.633ms	PASS

SI No	Test ID	Test Name	Test Result
		Response Check - TEST.PD.PROT.ALL3.6#5 >>DUT responded with Reserved message for Reserved message. Actual time interval is: 8.693ms	PASS
		Message Header and Extended Message Header - TEST.PD.PROT.ALL3.6#6	PASS
22	TEST.PD.PROT.ALL3.7	TEST.PD.PROT.ALL3.7 Security Messages Supported	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet16	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet18	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3UnchkdSnk >>SourceCap Packet94	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet96	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 9.054s and Sourcecap time: 9.237s [PASS] Max = 250ms. Obtained time difference is 182.482ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet184	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 40.045ms Packet 186	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 12.132s and Sourcecap time: 12.31s [PASS] Max = 250ms. Obtained time difference is 177.482ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet225	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 40.887ms Packet 227	PASS

SI No	Test ID	Test Name	Test Result
		Rev3ChkdSnk	PASS
		Security Request message response check - TEST.PD.PROT.ALL3.7#1 >>VIF field Security_Msgs_Supported_SOP is No. and UUT respond with Not_Supported message at protocol index 53	PASS
		Rev3UnchkdSnk	PASS
		Security Request message response check - TEST.PD.PROT.ALL3.7#1 >>VIF field Security_Msgs_Supported_SOP is No. and UUT respond with Not_Supported message at protocol index 137	PASS
		Rev3ChkdSrc	PASS
		Security Request message response check - TEST.PD.PROT.ALL3.7#1 >>VIF field Security_Msgs_Supported_SOP is No. and UUT respond with Not_Supported message at protocol index 203	PASS
		Rev3UnchkdSrc	PASS
		Security Request message response check - TEST.PD.PROT.ALL3.7#1 >>VIF field Security_Msgs_Supported_SOP is No. and UUT respond with Not_Supported message at protocol index 244	PASS
23	TEST.PD.PROT.ALL3.8	TEST.PD.PROT.ALL3.8 Get Revision Response	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet19	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet21	PASS
		Rev3ChkdSnk > Check the Test_CheckID 1 assertion in the protocol trace	PASS
		Get_Revision response check - TEST.PD.PROT.ALL3.8#1	PASS
		Revision message details check - TEST.PD.PROT.ALL3.8#2	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2	PASS

SI No	Test ID	Test Name	Test Result
		tSrcTransReq timer check - COMMON.PROC.BU.1#3	PASS
		Rev3ChkdSrc > Check the Test_CheckID 1 assertion in the protocol trace	PASS
		Get_Revision response check - TEST.PD.PROT.ALL3.8#1	PASS
		Revision message details check - TEST.PD.PROT.ALL3.8#2	PASS
24	TEST.PD.PROT.PORT3.1	TEST.PD.PROT.PORT3.1 Get Battery Status Response	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet16	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet18	PASS
		Rev3ChkdSnk >> Check the Test_CheckID 2 assertion in the protocol trace Check the Test_CheckID 2 assertion in the protocol trace Check the Test_CheckID 2 assertion in the protocol trace Check the Test_CheckID 2 assertion in the protocol trace Check the Test_CheckID 2 assertion in the protocol trace	PASS
		Get_Sink_Cap_Ext response check - TEST.PD.PROT.PORT3.1#1 >UUT respond Supported to Get_Sink_Cap_Ext message	PASS
		Get_Battery_Status response check - TEST.PD.PROT.PORT3.1#2 >UUT respond _Supported PD Message.Packet64 UUT responded with incorrect message to Get_Battery_Status message Check the Tester initiated Get_Battery_Status AMS and confirm Check the Tester initiated Get_Battery_Status AMS and confirm Check the Tester initiated Get_Battery_Status AMS and confirm Check the Tester initiated Get_Battery_Status AMS and confirm Check the Tester initiated Get_Battery_Status AMS and confirm	PASS

SI No	Test ID	Test Name	Test Result
		Not_Supported message check - TEST.PD.PROT.PORT3.1#3 >>[PASS]The values of VIF fields Num_Fixed_Batteries(Expected) : 1, Fixed_Batteries(Obtained) : 0 Num_Swappable_Battery_Slots(Expected) : 0, Hot_Swap_Batteries(Obtained) : 0	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 4.5s and Sourcecap time: 4.675s [PASS] Max = 250ms. Obtained time difference is 174.983ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet112	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 38.952ms Packet 115	PASS
		Rev3ChkdSrc	PASS
		Get_SourceCap_Extended response check - TEST.PD.PROT.PORT3.1#1 >>UUT respond Not_Supported to Get_SourceCap_Extended message	PASS
		Get_Battery_Status response check - TEST.PD.PROT.PORT3.1#2 >>UUT respond Battery_Status PD Message.Packet136 UUT respond Battery_Status PD Message.Packet141 UUT respond Battery_Status PD Message.Packet146 UUT respond Battery_Status PD Message.Packet151 UUT respond Battery_Status PD Message.Packet156 UUT respond Battery_Status PD Message.Packet161 UUT respond Battery_Status PD Message.Packet166 UUT respond Battery_Status PD Message.Packet171	PASS



[illegible]

SI No	Test ID	Test Name	Test Result
25	TEST.PD.PROT.PORT3.2	TEST.PD.PROT.PORT3.2 Invalid Battery Status	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet15	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet17	PASS
		Rev3ChkdSnk >> Check the Test_CheckID 1 assertion in the protocol trace Check the Test_CheckID 2 assertion in the protocol trace	PASS
		Get_Sink_Cap_Ext response check - TEST.PD.PROT.PORT3.2#1	PASS
		Get_Battery_Status response check - TEST.PD.PROT.PORT3.2#2	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3	PASS
		Rev3ChkdSrc >> Check the Test_CheckID 1 assertion in the protocol trace Check the Test_CheckID 2 assertion in the protocol trace	PASS
		Get_SourceCap_Extended response check - TEST.PD.PROT.PORT3.2#1	PASS
		Get_Battery_Status response check - TEST.PD.PROT.PORT3.2#2	PASS
26	TEST.PD.PROT.PORT3.3	TEST.PD.PROT.PORT3.3 Get Battery Cap Response	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet15	PASS

SI No	Test ID	Test Name	Test Result
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet17	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3UnchkdSnk >>SourceCap Packet239	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet241	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 15.71s and Sourcecap time: 15.894s [PASS] Max = 250ms. Obtained time difference is 184.148ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet465	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 51.155ms Packet 467	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 20.632s and Sourcecap time: 20.809s [PASS] Max = 250ms. Obtained time difference is 177.482ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet546	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 43.188ms Packet 548	PASS
		Rev3ChkdSnk	PASS
		Get_Sink_Cap_Ext check - TEST.PD.PROT.PORT3.3#1 >UUT respond_Supported to Get_Sink_Cap_Ext message	PASS
		Get_Battery_Cap check - TEST.PD.PROT.PORT3.3#2	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#0 - TEST.PD.PROT.PORT3.3#2 >UUT respond_Supported to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS

SI No	Test ID	Test Name	Test Result
		Get_Battery_Cap check for Battery_Cap_Ref_#1 - TEST.PD.PROT.PORT3.3#2 >UUT respond to Get_Battery_Cap message at protocol index 75	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#2 - TEST.PD.PROT.PORT3.3#2 >UUT respond to Get_Battery_Cap message at protocol index 109	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#3 - TEST.PD.PROT.PORT3.3#2 >UUT respond _Supported to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#4 - TEST.PD.PROT.PORT3.3#2 >UUT respond _Supported to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#5 - TEST.PD.PROT.PORT3.3#2 >UUT respond _Supported to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#6 - TEST.PD.PROT.PORT3.3#2 >UUT respond _Supported to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#7 - TEST.PD.PROT.PORT3.3#2 >UUT respond _Supported to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Rev3UnchkdSnk	PASS

SI No	Test ID	Test Name	Test Result
		Get_Sink_Cap_Ext check - TEST.PD.PROT.PORT3.3#1 >UUT respond_Supported to Get_Sink_Cap_Ext message	PASS
		Get_Battery_Cap check - TEST.PD.PROT.PORT3.3#2	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#0 - TEST.PD.PROT.PORT3.3#2 >UUT respond_Supported to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#1 - TEST.PD.PROT.PORT3.3#2 >UUT respond to Get_Battery_Cap message at protocol index 308	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#2 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Not_Supported to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#3 - TEST.PD.PROT.PORT3.3#2 >UUT respond to Get_Battery_Cap message at protocol index 339	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#4 - TEST.PD.PROT.PORT3.3#2 >UUT respond to Get_Battery_Cap message at protocol index 353	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#5 - TEST.PD.PROT.PORT3.3#2 >UUT respond_Supported to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#6 - TEST.PD.PROT.PORT3.3#2 >UUT respond to Get_Battery_Cap message at protocol index 388	PASS

SI No	Test ID	Test Name	Test Result
		Get_Battery_Cap check for Battery_Cap_Ref_#7 - TEST.PD.PROT.PORT3.3#2 >UUT respond _Supported to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Rev3ChkdSrc	PASS
		Get_SourceCap_Extended check - TEST.PD.PROT.PORT3.3#1 >UUT respond _Supported to Get_SourceCap_Extended message	PASS
		Get_Battery_Cap check - TEST.PD.PROT.PORT3.3#2	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#0 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#1 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#2 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#3 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#4 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS



SI No	Test ID	Test Name	Test Result
		Get_Battery_Cap check for Battery_Cap_Ref_#5 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#6 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#7 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Battery_Capabilities check - TEST.PD.PROT.PORT3.3#3	PASS
		Battery_Capabilities check for Battery_Cap_Ref_#0 - TEST.PD.PROT.PORT3.3#3 >>Invalid Battery Reference not matched with Number of Batteries field, Obtained Invalid Battery Reference value : 1, Obtained number of batteries/slots : 1 at protocol index 489 Battery type bit[1..7] is 489	PASS
		Battery_Capabilities check for Battery_Cap_Ref_#1 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 1 at protocol index 494 Battery type bit[1..7] is zero	PASS
		Battery_Capabilities check for Battery_Cap_Ref_#2 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 1 at protocol index 499 Battery type bit[1..7] is zero	PASS
		Battery_Capabilities check for Battery_Cap_Ref_#3 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 1 at protocol index 504 Battery type bit[1..7] is zero	PASS

SI No	Test ID	Test Name	Test Result
		Battery_Capabilities check for Battery_Cap_Ref_#4 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 1 at protocol index 509 Battery type bit[1..7] is zero	PASS
		Battery_Capabilities check for Battery_Cap_Ref_#5 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 1 at protocol index 514 Battery type bit[1..7] is zero	PASS
		Battery_Capabilities check for Battery_Cap_Ref_#6 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 1 at protocol index 519 Battery type bit[1..7] is zero	PASS
		Battery_Capabilities check for Battery_Cap_Ref_#7 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 1 at protocol index 524 Battery type bit[1..7] is zero	PASS
		Rev3UnchkdSrc	PASS
		Get_SourceCap_Extended check - TEST.PD.PROT.PORT3.3#1 >UUT respond Supported to Get_SourceCap_Extended message	PASS
		Get_Battery_Cap check - TEST.PD.PROT.PORT3.3#2	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#0 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#1 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS

SI No	Test ID	Test Name	Test Result
		Get_Battery_Cap check for Battery_Cap_Ref_#2 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#3 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#4 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#5 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#6 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#7 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Battery_Capabilities check - TEST.PD.PROT.PORT3.3#3	PASS

SI No	Test ID	Test Name	Test Result
		Battery_Capabilities check for Battery_Cap_Ref_#0 - TEST.PD.PROT.PORT3.3#3 >>Invalid Battery Reference not matched with Number of Batteries field, Obtained Invalid Battery Reference value : 1, Obtained number of batteries/slots : 1 at protocol index 570 Battery type bit[1..7] is 570	PASS
		Battery_Capabilities check for Battery_Cap_Ref_#1 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 1 at protocol index 575 Battery type bit[1..7] is zero	PASS
		Battery_Capabilities check for Battery_Cap_Ref_#2 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 1 at protocol index 580 Battery type bit[1..7] is zero	PASS
		Battery_Capabilities check for Battery_Cap_Ref_#3 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 1 at protocol index 585 Battery type bit[1..7] is zero	PASS
		Battery_Capabilities check for Battery_Cap_Ref_#4 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 1 at protocol index 590 Battery type bit[1..7] is zero	PASS
		Battery_Capabilities check for Battery_Cap_Ref_#5 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 1 at protocol index 595 Battery type bit[1..7] is zero	PASS
		Battery_Capabilities check for Battery_Cap_Ref_#6 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 1 at protocol index 600 Battery type bit[1..7] is zero	PASS
		Battery_Capabilities check for Battery_Cap_Ref_#7 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 1 at protocol index 605 Battery type bit[1..7] is zero	PASS

SI No	Test ID	Test Name	Test Result
27	TEST.PD.PROT.PORT3.4	TEST.PD.PROT.PORT3.4 Invalid Battery Capabilities Reference	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet15	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet17	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3UnchkdSnk >>SourceCap Packet113	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet115	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 8.373s and Sourcecap time: 8.546s [PASS] Max = 250ms. Obtained time difference is 173.316ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet170	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 39.576ms Packet 172	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 11.197s and Sourcecap time: 11.375s [PASS] Max = 250ms. Obtained time difference is 177.482ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet216	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 39.406ms Packet 218	PASS
		Rev3ChkdSnk	PASS
		Get_Sink_Cap_Ext check - TEST.PD.PROT.PORT3.4#1 >UUT respond to Get_Sink_Cap_Ext message	PASS
		Get_Battery_Cap check - TEST.PD.PROT.PORT3.4#2 >UUT respond to Get_Battery_Cap message	PASS

SI No	Test ID	Test Name	Test Result
		Rev3UnchkdSnk	PASS
		Get_Sink_Cap_Ext check - TEST.PD.PROT.PORT3.4#1 >UUT respond_Supported to Get_Sink_Cap_Ext message	PASS
		Get_Battery_Cap check - TEST.PD.PROT.PORT3.4#2 >UUT respond_Supported message	PASS
		Rev3ChkdSrc	PASS
		Get_SourceCap_Extended check - TEST.PD.PROT.PORT3.4#1 >UUT respond_Supported to Get_SourceCap_Extended message	PASS
		Get_Battery_Cap check - TEST.PD.PROT.PORT3.4#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message	PASS
		Battery_Capabilities check - TEST.PD.PROT.PORT3.4#3 >>[15:0] Vendor_ID field Exp:0xFFFF but Obt:0 [Bit 0]:Invalid battery reference field is 1 [Bit 1..7]:Battery type bit is 1	PASS
		Rev3UnchkdSrc	PASS
		Get_SourceCap_Extended check - TEST.PD.PROT.PORT3.4#1 >>UUT respond Not_Supported to Get_SourceCap_Extended message	PASS
		Get_Battery_Cap check - TEST.PD.PROT.PORT3.4#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message	PASS
		Battery_Capabilities check - TEST.PD.PROT.PORT3.4#3 >>[15:0] Vendor_ID field Exp:0xFFFF but Obt:0 [Bit 0]:Invalid battery reference field is 1 [Bit 1..7]:Battery type bit is 1	PASS
28	TEST.PD.PROT.PORT3.5	TEST.PD.PROT.PORT3.5 Get Country Codes Response	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet15	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet17	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3UnchkdSnk >>SourceCap Packet114	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet116	PASS
		COMMON.PROC.BU.1	PASS



SI No	Test ID	Test Name	Test Result
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 9.229s and Sourcecap time: 9.409s [PASS] Max = 250ms. Obtained time difference is 179.982ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet160	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 38.977ms Packet 162	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 12.007s and Sourcecap time: 12.187s [PASS] Max = 250ms. Obtained time difference is 179.982ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet201	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 40.472ms Packet 203	PASS
		Rev3ChkdSnk	PASS
		Country_Codes check - TEST.PD.PROT.PORT3.5#1 >UUT respond to Get_Country_Codes message	PASS
		Rev3UnchkdSnk	PASS
		Country_Codes check - TEST.PD.PROT.PORT3.5#1 >>UUT respond Not_Supported to Get_Country_Codes message	PASS
		Rev3ChkdSrc	PASS
		Country_Codes check - TEST.PD.PROT.PORT3.5#1 >>UUT respond Not_Supported to Get_Country_Codes message	PASS
		Rev3UnchkdSrc	PASS
		Country_Codes check - TEST.PD.PROT.PORT3.5#1 >>UUT respond Not_Supported to Get_Country_Codes message	PASS
29	TEST.PD.PROT.PORT3.6	TEST.PD.PROT.PORT3.6 Get Country Info Response	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet15	PASS

SI No	Test ID	Test Name	Test Result
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet17	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3UnchkdSnk >>SourceCap Packet75	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet77	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 6.879s and Sourcecap time: 7.052s [PASS] Max = 250ms. Obtained time difference is 173.316ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet141	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 43.078ms Packet 143	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 9.694s and Sourcecap time: 9.872s [PASS] Max = 250ms. Obtained time difference is 177.482ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet182	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 41.816ms Packet 184	PASS
		Rev3ChkdSnk	PASS
		Country_Codes check - TEST.PD.PROT.PORT3.6#1 >>UUT respond Not_Supported to Get_Country_Codes message	PASS
		Rev3UnchkdSnk	PASS
		Country_Codes check - TEST.PD.PROT.PORT3.6#1 >>UUT respond Not_Supported to Get_Country_Codes message	PASS
		Rev3ChkdSrc	PASS
		Country_Codes check - TEST.PD.PROT.PORT3.6#1 >>UUT respond Not_Supported to Get_Country_Codes message	PASS

SI No	Test ID	Test Name	Test Result
		Rev3UnchkdSrc	PASS
		Country_Codes check - TEST.PD.PROT.PORT3.6#1 >>UUT respond Not Supported to Get_Country_Codes message	PASS
30	TEST.PD.PROT.PORT3.7	TEST.PD.PROT.PORT3.7 Unchunked Extended Message Supported	NA
		--- In VIF Unchunked_Extended_Messages_Supported field is NO	
31	TEST.PD.PROT.SRC.1	TEST.PD.PROT.SRC.1 Get_Source_Cap Response	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.257s and Sourcecap time: 1.434s [PASS] Max = 250ms. Obtained time difference is 177.482ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet21	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 42.441ms Packet 23	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 4.344s and Sourcecap time: 4.524s [PASS] Max = 250ms. Obtained time difference is 179.982ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet68	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 41.142ms Packet 70	PASS
		Rev2Src	PASS
		Source_Cap message check - TEST.PD.PROT.SRC.1#1 >>UUT is successfully respond to Get_Source_Cap message.Protocol index #40	PASS
		Rev3ChkdSrc	PASS
		Source_Cap message check - TEST.PD.PROT.SRC.1#1 >>UUT is successfully respond to Get_Source_Cap message.Protocol index #87	PASS
32	TEST.PD.PROT.SRC.2	TEST.PD.PROT.SRC.2 Get_Source_Cap No Request	PASS

SI No	Test ID	Test Name	Test Result
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.192s and Sourcecap time: 1.37s [PASS] Max = 250ms. Obtained time difference is 178.316ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet21	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 42.447ms Packet 23	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 5.703s and Sourcecap time: 5.88s [PASS] Max = 250ms. Obtained time difference is 177.482ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet84	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 39.281ms Packet 86	PASS
		Rev2Src	PASS
		Source_Cap message check - TEST.PD.PROT.SRC.2#1 >>UUT successfully respond to Get_Source_Cap message.Protocol index #40	PASS
		Hard_Reset message check - TEST.PD.PROT.SRC.2#2 >UUT to respond Hard_Reset within 0.024~0.03s..Obtained interval is 0.0255s.Protocol index #42	PASS
		Rev3ChkdSrc	PASS
		Source_Cap message check - TEST.PD.PROT.SRC.2#1 >>UUT successfully respond to Get_Source_Cap message.Protocol index #103	PASS
		Hard_Reset message check - TEST.PD.PROT.SRC.2#2 >>UUT responded with Hard_Reset within 0.027~0.033s..Obtained interval is 0.0316s.Protocol index #105	PASS
33	TEST.PD.PROT.SRC.3	TEST.PD.PROT.SRC.3 Sender Response Timer Deadline	PASS

SI No	Test ID	Test Name	Test Result
		Rev2Src	PASS
		tFirstSourceCap timer check - TEST.PD.PROT.SRC.3#1 >>start time: 1.51959565 VBusUp time: 1.34294665s Obt time:0.1766s [PASS] Max = 250ms. Obtained time difference is 176.649ms	PASS
		Request message response check - TEST.PD.PROT.SRC.3#2 >>UUT respond Accept to Request message	PASS
		Rev3ChkdSrc	PASS
		tFirstSourceCap timer check - TEST.PD.PROT.SRC.3#1 >>start time: 4.50385811 VBusUp time: 4.32970886s Obt time:0.1741s [PASS] Max = 250ms. Obtained time difference is 174.149ms	PASS
		Request message response check - TEST.PD.PROT.SRC.3#2 >>UUT respond Accept to Request message	PASS
34	TEST.PD.PROT.SRC.4	TEST.PD.PROT.SRC.4 Reject Request	PASS
		Rev2Src	PASS
		PDO#1	PASS
		tFirstSourceCap timer check - TEST.PD.PROT.SRC.4#1 >>start time: 1.40426394 VBusUp time: 1.23428094s Obt time:0.17s [PASS] Max = 250ms. Obtained time difference is 169.983ms	PASS
		Reject check - TEST.PD.PROT.SRC.4#2 >>UUT sent Reject message at Protocol index 24	PASS
		Rev3ChkdSrc	PASS
		PDO#1	PASS
		tFirstSourceCap timer check - TEST.PD.PROT.SRC.4#1 >>start time: 6.38843156 VBusUp time: 6.21928181s Obt time:0.1691s [PASS] Max = 250ms. Obtained time difference is 169.15ms	PASS
		Reject check - TEST.PD.PROT.SRC.4#2 >>UUT sent Reject message at Protocol index 49	PASS
35	TEST.PD.PROT.SRC.5	TEST.PD.PROT.SRC.5 Reject Request Invalid Object Position	PASS
		Rev2Src	PASS
		Source_Cap check - TEST.PD.PROT.SRC.5#1 >>start time: 1.43796832 VBusUp time: 1.26965182s Obt time:0.1683s [PASS] Max = 250ms. Obtained time difference is 168.317ms	PASS
		Reject check - TEST.PD.PROT.SRC.5#2 >>UUT sent Reject message at protocol index 24	PASS

SI No	Test ID	Test Name	Test Result
		Rev3ChkdSrc	PASS
		Source_Cap check - TEST.PD.PROT.SRC.5#1 >>start time: 6.42848223 VBusUp time: 6.25349973s Obt time:0.175s [PASS] Max = 250ms. Obtained time difference is 174.983ms	PASS
		Reject check - TEST.PD.PROT.SRC.5#2 >>UUT sent Reject message at protocol index 49	PASS
36	TEST.PD.PROT.SRC.6	TEST.PD.PROT.SRC.6 Atomic Message Sequence – Request	PASS
		Rev2Src	PASS
		tFirstSourceCap timer check - TEST.PD.PROT.SRC.6#1 >>start time: 1.38202916 VBusUp time: 1.20871316s Obt time:0.1733s [PASS] Max = 250ms. Obtained time difference is 173.316ms	PASS
		tProtErrSoftReset timer check - TEST.PD.PROT.SRC.6#2 >>UUT sent SoftReset message received within tSoftReset_Max 0.015s.Protocol index #24	PASS
		tTypeCSinkWaitCap_Max check - TEST.PD.PROT.SRC.6#3 >>UUT sent Source_Cap message after Soft_Reset within tTypeCSinkWaitCap_Max 0.62s.Protocol index #28 Tester sent Accept message	PASS
		Rev3ChkdSrc	PASS
		tFirstSourceCap timer check - TEST.PD.PROT.SRC.6#1 >>start time: 4.37813954 VBusUp time: 4.20399029s Obt time:0.1741s [PASS] Max = 250ms. Obtained time difference is 174.149ms	PASS
		tProtErrSoftReset timer check - TEST.PD.PROT.SRC.6#2 >>UUT sent SoftReset message received within tSoftReset_Max 0.015s.Protocol index #69	PASS
		tTypeCSinkWaitCap_Max check - TEST.PD.PROT.SRC.6#3 >>UUT sent Source_Cap message after Soft_Reset within tTypeCSinkWaitCap_Max 0.62s.Protocol index #73 Tester sent Accept message	PASS
37	TEST.PD.PROT.SRC.7	TEST.PD.PROT.SRC.7 DR_Swap	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src	PASS



SI No	Test ID	Test Name	Test Result
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.303s and Sourcecap time: 1.48s [PASS] Max = 250ms. Obtained time difference is 176.649ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet21	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 39.809ms Packet 23	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 7.776s and Sourcecap time: 7.952s [PASS] Max = 250ms. Obtained time difference is 175.816ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet67	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 41.756ms Packet 69	PASS
		Rev2Src	PASS
		DR_Swap Response Check - TEST.PD.PROT.SRC.7#1 >>UUT respond Accept to DR_Swap message and DR_Swap_To_UFP_Supported field is Yes	PASS
		DR_Swap Response Check - TEST.PD.PROT.SRC.7#2 >>UUT respond Accept to DR_Swap message and DR_Swap_To_DFP_Supported field is Yes	PASS
		Rev3ChkdSrc	PASS
		DR_Swap Response Check - TEST.PD.PROT.SRC.7#1 >>UUT respond Accept to DR_Swap message and DR_Swap_To_UFP_Supported field is Yes	PASS
		DR_Swap Response Check - TEST.PD.PROT.SRC.7#2 >>UUT respond Accept to DR_Swap message and DR_Swap_To_DFP_Supported field is Yes	PASS
38	TEST.PD.PROT.SRC.8	TEST.PD.PROT.SRC.8 VCONN_Swap Response	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src	PASS

SI No	Test ID	Test Name	Test Result
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.223s and Sourcecap time: 1.401s [PASS] Max = 250ms. Obtained time difference is 178.316ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet21	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 50.328ms Packet 23	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 5.731s and Sourcecap time: 5.905s [PASS] Max = 250ms. Obtained time difference is 174.149ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet63	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 39.577ms Packet 65	PASS
		Rev2Src	PASS
		VCONN_Swap response check - TEST.PD.PROT.SRC.8#1 >>UUT respond Reject to VCONN_Swap message at protocol index 40 and VCONN_Swap_To_Off_Supported field is NO	PASS
		tVONNSourceOff timer check - TEST.PD.PROT.SRC.8#2	NA
		Second VCONN_Swap response check - TEST.PD.PROT.SRC.8#3	NA
		PS_RDY check - TEST.PD.PROT.SRC.8#4	NA
		VCONN present check - TEST.PD.PROT.SRC.8#5	NA
		Third VCONN_Swap response check - TEST.PD.PROT.SRC.8#6	NA
		PS_RDY holding check - TEST.PD.PROT.SRC.8#7	NA
		Rev3ChkdSrc	NA
		VCONN_Swap response check - TEST.PD.PROT.SRC.8#1 >>UUT respond Reject to VCONN_Swap message at protocol index 82 and VCONN_Swap_To_Off_Supported field is NO	NA
		tVONNSourceOff timer check - TEST.PD.PROT.SRC.8#2	NA
		Second VCONN_Swap response check - TEST.PD.PROT.SRC.8#3	NA
		PS_RDY check - TEST.PD.PROT.SRC.8#4	NA

SI No	Test ID	Test Name	Test Result
		VCONN present check - TEST.PD.PROT.SRC.8#5	NA
		Third VCONN_Swap response check - TEST.PD.PROT.SRC.8#6	NA
		PS_RDY holding check - TEST.PD.PROT.SRC.8#7	NA
39	TEST.PD.PROT.SRC.9	TEST.PD.PROT.SRC.9 PR_Swap Response	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.233s and Sourcecap time: 1.412s [PASS] Max = 250ms. Obtained time difference is 178.316ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet21	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 39.61ms Packet 23	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 7.722s and Sourcecap time: 7.899s [PASS] Max = 250ms. Obtained time difference is 177.482ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet137	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 40.43ms Packet 139	PASS
		Rev2Src	PASS
		PR_Swap response check - TEST.PD.PROT.SRC.9#1 >>UUT respond Accept to PR_Swap message.The VIF field PD_Port_Type is DRP.The VIF field Accepts PR_Swap As Src is YES	PASS
		UUT PS_RDY vSafe0V check - TEST.PD.PROT.SRC.9#2 >>UUT respond PS_RDY message to PR_SWAP after VBUS voltage to vSafe0V(0V - 0.8V).The present voltage is 0.207V	PASS

SI No	Test ID	Test Name	Test Result
		tPSSourceOff timer check - TEST.PD.PROT.SRC.9#3 >>UUT respond PS_RDY within tPSSourceOff_Min(750ms) time.The present interval is 0.045s Tester respond PS_RDY message to UUT message within tNewSrc_Max(275ms).The interval is 0.0418s	PASS
		PD contract check - TEST.PD.PROT.SRC.9#4 >>UUT respond Request to Source_Cap message.	PASS
		PR_Swap response check - TEST.PD.PROT.SRC.9#5 >UUT respond to PR_Swap message.	PASS
		Rev3ChkdSrc	PASS
		PR_Swap response check - TEST.PD.PROT.SRC.9#1 >>UUT respond Accept to PR_Swap message.The VIF field PD_Port_Type is DRP.The VIF field Accepts_PR_Swap_As_Src is YES	PASS
		UUT PS_RDY vSafe0V check - TEST.PD.PROT.SRC.9#2 >>UUT respond PS_RDY message to PR_Swap after VBUS voltage to vSafe0V(0V - 0.8V).The present voltage is 0.0944V	PASS
		tPSSourceOff timer check - TEST.PD.PROT.SRC.9#3 >>UUT respond PS_RDY within tPSSourceOff_Min(750ms) time.The present interval is 0.0552s Tester respond PS_RDY message to UUT message within tNewSrc_Max(275ms).The interval is 0.0421s	PASS
		PD contract check - TEST.PD.PROT.SRC.9#4 >>UUT respond Request to Source_Cap message.	PASS
		PR_Swap response check - TEST.PD.PROT.SRC.9#5 >>UUT respond Accept to PR_Swap message.The VIF field Accept_PR_Swap_As_Snk is YES.	PASS
		UUT Rp check - TEST.PD.PROT.SRC.9#6	PASS
		UUT PSRDY vSafe5V check - TEST.PD.PROT.SRC.9#7 >>UUT respond PS_RDY message to Tester message.The present voltage is 5.0619V	PASS
		tPSSourceOn timer check - TEST.PD.PROT.SRC.9#8 >>UUT respond PS_RDY message to Tester message within tPSSourceOn_Min(390ms).The interval is 0.0653s	PASS

SI No	Test ID	Test Name	Test Result
		tFirstSourceCap timer check - TEST.PD.PROT.SRC.9#9 >>[PASS] Min= 20ms - Max = 250ms. Obtained time difference is 198.247ms	PASS
40	TEST.PD.PROT.SRC.10	TEST.PD.PROT.SRC.10 PR_Swap – PSSourceOnTimer Timeout	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.275s and Sourcecap time: 1.453s [PASS] Max = 250ms. Obtained time difference is 177.507ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet21	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 41.305ms Packet 23	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 6.032s and Sourcecap time: 6.208s [PASS] Max = 250ms. Obtained time difference is 176.327ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet102	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 39.829ms Packet 104	PASS
		Rev2Src	PASS
		PR_Swap response check - TEST.PD.PROT.SRC.10#1 >>UUT respond Accept to PR_Swap message.The VIF field PD_Port_Type is set to DRP	PASS
		PS_RDY message check - TEST.PD.PROT.SRC.10#2 >>PS_RDY message recieved at 0.7346 V UUT sent PS_RDY message to PR_Swap response after VBUS voltage is with in vSafe0V(0V-0.8V) UUT sent PS_RDY within tSrcTransition_Max(35ms) + tSrcSwapStdby_Max(650ms) time.The time interval is 0.0542s, start time 2.3611s, stop time 2.4153s	PASS

SI No	Test ID	Test Name	Test Result
		Hard_Reset message check - TEST.PD.PROT.SRC.10#3 >>UUT sent Type-C Error Recovery within tPSSourceOn[390ms - 480ms].The time interval is 0.4529s	PASS
		Rev3ChkdSrc	PASS
		PR_Swap response check - TEST.PD.PROT.SRC.10#1 >>UUT respond Accept to PR_Swap message.The VIF field PD_Port_Type is set to DRP	PASS
		PS_RDY message check - TEST.PD.PROT.SRC.10#2 >PS_RDY message recieved at 0.4762 V UUT sent PS_RDY message to PR_Swap response after VBUS voltage is not with in vSafe0V(0V-0.8V) UUT sent PS_RDY within tSrcTransition_Max(35ms) + tSrcSwapStdby_Max(650ms) time.The time interval is 0.0421s, start time 7.1203s, stop time 7.1624s	PASS
		Hard_Reset message check - TEST.PD.PROT.SRC.10#3 >>UUT sent Type-C Error Recovery within tPSSourceOn[390ms - 480ms].The time interval is 0.4519s	PASS
41	TEST.PD.PROT.SRC.11	TEST.PD.PROT.SRC.11 Unexpected Message Received in Ready State	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.197s and Sourcecap time: 1.375s [PASS] Max = 250ms. Obtained time difference is 178.316ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet21	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 42.851ms Packet 23	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 4.695s and Sourcecap time: 4.867s [PASS] Max = 250ms. Obtained time difference is 171.65ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet72	PASS



SI No	Test ID	Test Name	Test Result
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 40.49ms Packet 74	PASS
		Rev2Src	PASS
		Soft_Reset check - TEST.PD.PROT.SRC.11#1 >>UUT is sent SoftReset message within tProtErrSoftReset_Max(15ms).The obtained interval is 0.0054s.Protocol index #40	PASS
		Soft_Reset check - TEST.PD.PROT.SRC.11#1 >>UUT is sent SoftReset message within tProtErrSoftReset_Max(15ms).The obtained interval is 0.0054s.Protocol index #40	PASS
		Rev3ChkdSrc	PASS
		Soft_Reset check - TEST.PD.PROT.SRC.11#1 >>UUT is sent SoftReset message within tProtErrSoftReset_Max(15ms).The obtained interval is 0.0067s.Protocol index #91	PASS
		Soft_Reset check - TEST.PD.PROT.SRC.11#1 >>UUT is sent SoftReset message within tProtErrSoftReset_Max(15ms).The obtained interval is 0.0067s.Protocol index #91	PASS
42	TEST.PD.PROT.SRC.12	TEST.PD.PROT.SRC.12 Get_Sink_Cap Response	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.196s and Sourcecap time: 1.373s [PASS] Max = 250ms. Obtained time difference is 176.649ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet21	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 38.611ms Packet 23	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS

SI No	Test ID	Test Name	Test Result
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 3.781s and Sourcecap time: 3.96s [PASS] Max = 250ms. Obtained time difference is 179.149ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet62	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 41.391ms Packet 64	PASS
		Rev2Src	PASS
		Get_Sink_Cap response check - TEST.PD.PROT.SRC.12#1 >>UUT respond SinkCap to Get_Sink_Cap message.Protocol index #40	PASS
		Rev3ChkdSrc	PASS
		Get_Sink_Cap response check - TEST.PD.PROT.SRC.12#1 >>UUT respond SinkCap to Get_Sink_Cap message.Protocol index #81	PASS
43	TEST.PD.PROT.SRC.13	TEST.PD.PROT.SRC.13 PR Swap GoodCRC not sent in Response to PS_RDY	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.249s and Sourcecap time: 1.429s [PASS] Max = 250ms. Obtained time difference is 179.982ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet21	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 40.381ms Packet 23	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 6.599s and Sourcecap time: 6.783s [PASS] Max = 250ms. Obtained time difference is 184.148ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet111	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 39.403ms Packet 113	PASS

SI No	Test ID	Test Name	Test Result
		Rev2Src	PASS
		PR_Swap response check - TEST.PD.PROT.SRC.13#1 >>UUT respond Accept to PR_Swap message.The VIF field PD_Port_Type is set to DRP	PASS
		PS_RDY message check - TEST.PD.PROT.SRC.13#2 >>UUT sent PS_RDY message to PR_SWAp response after VBUS voltage to vSafe0V(0V-0.8V).The present voltage is 0.4342V.Protocol index #45 UUT sent PS_RDY within tSrcTransition_Max(35ms) + tSrcSwapStdby_Max(650ms) time.The time interval is 0.0596s.Protocol index #45	PASS
		USB Type-C Error_Recovery check - TEST.PD.PROT.SRC.13#3 >>Expected nRetryCount is 3.Obtained retry count is 3 DUT response time:(0.0388 mS),spec limit time interval is:[<= 15.000000 mS]	PASS
		Rev3ChkdSrc	PASS
		PR_Swap response check - TEST.PD.PROT.SRC.13#1 >>UUT respond Accept to PR_Swap message.The VIF field PD_Port_Type is set to DRP	PASS
		PS_RDY message check - TEST.PD.PROT.SRC.13#2 >>UUT sent PS_RDY message to PR_SWAp response after VBUS voltage to vSafe0V(0V-0.8V).The present voltage is 0.3866V.Protocol index #135  UUT sent PS_RDY within tSrcTransition_Max(35ms) + tSrcSwapStdby_Max(650ms) time.The time interval is 0.0557s.Protocol index #135	PASS
		USB Type-C Error_Recovery check - TEST.PD.PROT.SRC.13#3 >>Expected nRetryCount is 2.Obtained retry count is 2 DUT response time:(13.92023 mS),spec limit time interval is:[<= 15.000000 mS]	PASS
44	TEST.PD.PROT.SRC3.1	TEST.PD.PROT.SRC3.1 SourceCapabilityTimer Timeout	PASS
		Rev3ChkdSrc	PASS
		tFirstSourceCap timer check - TEST.PD.PROT.SRC3.1#1 >>start time: 1.39576642 VBusUp time: 1.22161717s Obt time:0.1741s [PASS] Max = 250ms. Obtained time difference is 174.149ms	PASS

SI No	Test ID	Test Name	Test Result
		tTypeCSendSourceCap timer check - TEST.PD.PROT.SRC3.1#2 >>SourceCap[1-2]:Min= 0ms - Max= 1.295ms.Obtained value 0.9882ms SourceCap[2-3]:Min= 0ms - Max= 1.295ms.Obtained value 0.98841ms SourceCap[3-4]:Min= 100.9ms - Max= 201.1ms.Obtained value 167.77426ms SourceCap[4-5]:Min= 0ms - Max= 1.295ms.Obtained value 0.98901ms	PASS
45	TEST.PD.PROT.SRC3.2	TEST.PD.PROT.SRC3.2 SenderResponseTimer Timeout	PASS
		Rev3ChkdSrc	PASS
		Source_Cap check - TEST.PD.PROT.SRC3.2#1 >>start time: 1.41092837 VBusUp time: 1.24261187s Obt time:0.1683s [PASS] Max = 250ms. Obtained time difference is 168.317ms	PASS
		Hard_Reset check - TEST.PD.PROT.SRC3.2#2 >>DUT sent Hard_Reset message within tSenderResponse Min(27ms) and Max(33ms) timer.The obtained time interval is 0.0288s	PASS
46	TEST.PD.PROT.SRC3.3	TEST.PD.PROT.SRC3.3 Get_Source_Cap_Extended Response	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.217s and Sourcecap time: 1.398s [PASS] Max = 250ms. Obtained time difference is 180.815ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet21	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 41.77ms Packet 23	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 5.726s and Sourcecap time: 5.902s [PASS] Max = 250ms. Obtained time difference is 175.816ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet62	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 43.359ms Packet 64	PASS
		Rev3ChkdSrc	PASS

SI No	Test ID	Test Name	Test Result
		Source_Cap check - [TEST.PD.PROT.SRC3.3#1 >>UUT respond Not_Supported to Get_Source_Cap_Extended message.	PASS
		Rev3UnchkdSrc	PASS
		Source_Cap check - [TEST.PD.PROT.SRC3.3#1 >>UUT respond Not_Supported to Get_Source_Cap_Extended message.	PASS
47	TEST.PD.PROT.SRC3.4	TEST.PD.PROT.SRC3.4 Alert Response Source Input Change	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.271s and Sourcecap time: 1.45s [PASS] Max = 250ms. Obtained time difference is 179.149ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet21	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 38.903ms Packet 23	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 4.766s and Sourcecap time: 4.941s [PASS] Max = 250ms. Obtained time difference is 175.816ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet60	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 40.731ms Packet 62	PASS
		Rev3ChkdSrc >> UUT is not respond to Alert message.	PASS
		Rev3UnchkdSrc >> UUT is not respond to Alert message.	PASS
48	TEST.PD.PROT.SRC3.5	TEST.PD.PROT.SRC3.5 Alert Response Battery Status Change	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS

SI No	Test ID	Test Name	Test Result
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.188s and Sourcecap time: 1.366s [PASS] Max = 250ms. Obtained time difference is 178.316ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet21	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 41.23ms Packet 23	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 4.296s and Sourcecap time: 4.47s [PASS] Max = 250ms. Obtained time difference is 174.149ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet60	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 40.143ms Packet 62	PASS
		Rev3ChkdSrc	PASS
		Get_Battery_Status check - TEST.PD.PROT.SRC3.5#1 >>UUT is not respond to Alert message	PASS
		Rev3UnchkdSrc	PASS
		Get_Battery_Status check - TEST.PD.PROT.SRC3.5#1 >>UUT is not respond to Alert message	PASS
49	TEST.PD.PROT.SRC3.6	TEST.PD.PROT.SRC3.6 Soft_Reset Sent when SinkTxOK	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.239s and Sourcecap time: 1.415s [PASS] Max = 250ms. Obtained time difference is 175.816ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet21	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 42.758ms Packet 23	PASS



SI No	Test ID	Test Name	Test Result
		Rev3ChkdSrc	PASS
		Soft_Reset check - TEST.PD.PROT.SRC3.6#1 >>UUT is respond message within tReceiveMax(1.1ms) + tSoftResetMax(15ms).The interval is 0.0056s	PASS
50	TEST.PD.PROT.SRC3.7	TEST.PD.PROT.SRC3.7 Get_PPS_Status Response	NA
		--- UUT does not support PPS APDO in Source Caps	
51	TEST.PD.PROT.SRC3.8	TEST.PD.PROT.SRC3.8 SourcePPSCCommTimer Deadline	NA
		--- UUT does not support PPS APDO in Source Caps	
52	TEST.PD.PROT.SRC3.9	TEST.PD.PROT.SRC3.9 SourcePPSCCommTimer Timeout	NA
		--- UUT does not support PPS APDO in Source Caps	
53	TEST.PD.PROT.SRC3.10	TEST.PD.PROT.SRC3.10 SourcePPSCCommTimer Stopped	NA
		--- UUT does not support PPS APDO in Source Caps	
54	TEST.PD.PROT.SRC3.11	TEST.PD.PROT.SRC3.11 GoodCRC Specification Revision Compatibility	PASS
		Rev3ChkdSrc	PASS
		1.SourceCap Check - TEST.PD.PROT.SRC3.11#1	PASS
		1.GoodCRC Specification Revision with 00b - TEST.PD.PROT.SRC3.11#2	PASS
		2.SourceCap Check - TEST.PD.PROT.SRC3.11#1	PASS
		2.GoodCRC Specification Revision with 01b - TEST.PD.PROT.SRC3.11#2	PASS
		3.SourceCap Check - TEST.PD.PROT.SRC3.11#1	PASS
		3.GoodCRC Specification Revision with 10b - TEST.PD.PROT.SRC3.11#2	PASS
55	TEST.PD.PROT.SRC3.12	TEST.PD.PROT.SRC3.12 FR Swap Without Signaling	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.265s and Sourcecap time: 1.447s [PASS] Max = 250ms. Obtained time difference is 182.482ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet21	PASS

SI No	Test ID	Test Name	Test Result
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 40.358ms Packet 23	PASS
		Rev3ChkdSrc	PASS
		FR_Swap response check - TEST.PD.PROT.SRC3.12#1 >>DUT respond Not Supported to FR_Swap message	PASS
56	TEST.PD.PROT.SRC3.13	TEST.PD.PROT.SRC3.13 Cable Type Detection	PASS
		Rev3ChkdSrc	PASS
		Source_Cap PDO check - TEST.PD.PROT.SRC3.13#1 >>UUT sent SourceCap message.Protocol index #20 UUT SourceCap message offering current <=3A or voltage <=20V	PASS
		Source_Cap PDO check - TEST.PD.PROT.SRC3.13#2 >>UUT sent SourceCap message.Protocol index #50 UUT SourceCap message offering current <=3A or voltage <=20V	PASS
		Source_Cap PDO check - TEST.PD.PROT.SRC3.13#3 >>UUT sent SourceCap message.Protocol index #80 UUT SourceCap message offering current <=3A or voltage <=20V	PASS
57	TEST.PD.PROT.SRC3.14	TEST.PD.PROT.SRC3.14 Source Info	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.246s and Sourcecap time: 1.417s [PASS] Max = 250ms. Obtained time difference is 170.816ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet21	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 43.388ms Packet 23	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 3.755s and Sourcecap time: 3.933s [PASS] Max = 250ms. Obtained time difference is 178.316ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet62	PASS

SI No	Test ID	Test Name	Test Result
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 42.75ms Packet 64	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 6.301s and Sourcecap time: 6.477s [PASS] Max = 250ms. Obtained time difference is 176.649ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet103	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 41.19ms Packet 105	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 8.853s and Sourcecap time: 9.029s [PASS] Max = 250ms. Obtained time difference is 176.649ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet144	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 39.966ms Packet 146	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 11.391s and Sourcecap time: 11.57s [PASS] Max = 250ms. Obtained time difference is 179.149ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet185	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 43.238ms Packet 187	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 13.97s and Sourcecap time: 14.145s [PASS] Max = 250ms. Obtained time difference is 174.983ms	PASS

SI No	Test ID	Test Name	Test Result
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet226	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 42.304ms Packet 228	PASS
		Rev3ChkdSrc	PASS
		First Source_Info field check - TEST.PD.PROT.SRC3.14#1 >Source_Info message Port Type (B31) does match to the Port_Managed_Guaranteed_Type VIF field	PASS
		First Get_Source_Info response check - TEST.PD.PROT.SRC3.14#2 >>Tester sent Get_Source_Info message Packet 38 UUT respond Source_Info message for Get_Source_Info message at protocol index #40	PASS
		Rev3ChkdSrc	PASS
		Second Get_Source_Info response check - TEST.PD.PROT.SRC3.14#3 >>Tester sent Get_Source_Info message Packet 79 UUT respond Source_Info message for Get_Source_Info message at protocol index #81	PASS
		Second Source_Info field check - TEST.PD.PROT.SRC3.14#4 >Source_Info message Port Type (B31) does match to the Port_Managed_Guaranteed_Type VIF field	PASS
		Rev3ChkdSrc	PASS
		Third Get_Source_Info response check - TEST.PD.PROT.SRC3.14#5 >>Tester sent Get_Source_Info message Packet 120 UUT respond Source_Info message for Get_Source_Info message at protocol index #122	PASS
		Third Source_Info field check - TEST.PD.PROT.SRC3.14#6 >>Source_Info message Port Type (B31) does not match to the Port_Managed_Guaranteed_Type VIF field	PASS
		Rev3UnchkdSrc	PASS

SI No	Test ID	Test Name	Test Result
		First Source_Info field check - TEST.PD.PROT.SRC3.14#1 >Source_Info message Port Type (B31) does match to the Port_Managed_Guaranteed_Type VIF field	PASS
		First Get_Source_Info response check - TEST.PD.PROT.SRC3.14#2 >>Tester sent Get_Source_Info message Packet 161 UUT respond Source_Info message for Get_Source_Info message at protocol index #163	PASS
		Rev3UnchkdSrc	PASS
		Second Get_Source_Info response check - TEST.PD.PROT.SRC3.14#3 >>Tester sent Get_Source_Info message Packet 202 UUT respond Source_Info message for Get_Source_Info message at protocol index #204	PASS
		Second Source_Info field check - TEST.PD.PROT.SRC3.14#4 >>Source_Info message Port Type (B31) does not match to the Port_Managed_Guaranteed_Type VIF field	PASS
		Rev3UnchkdSrc	PASS
		Third Get_Source_Info response check - TEST.PD.PROT.SRC3.14#5 >>Tester sent Get_Source_Info message Packet 243 UUT respond Source_Info message for Get_Source_Info message at protocol index #245	PASS
		Third Source_Info field check - TEST.PD.PROT.SRC3.14#6 >Source_Info message Port Type (B31) does match to the Port_Managed_Guaranteed_Type VIF field	PASS
58	TEST.PD.PROT.SRC3.15	TEST.PD.PROT.SRC3.15 Alert Response Extended Alert	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.219s and Sourcecap time: 1.399s [PASS] Max = 250ms. Obtained time difference is 179.982ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet21	PASS

SI No	Test ID	Test Name	Test Result
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 39.617ms Packet 23	PASS
		Rev3ChkdSrc >> Tester sent Alert message Packet 38	PASS
		Accept message check - TEST.PD.PROT.SRC3.15#1 >>UUT sent Request message Packet 41 UUT responded with Accept at Protocol Index 43	PASS
59	TEST.PD.PROT.SNK.1	TEST.PD.PROT.SNK.1 Get_Sink_Cap Response	NA
60	TEST.PD.PROT.SNK.2	TEST.PD.PROT.SNK.2 Get_Source_Cap Response	NA
61	TEST.PD.PROT.SNK.3	TEST.PD.PROT.SNK.3 SinkWaitCapTimer Deadline	NA
62	TEST.PD.PROT.SNK.4	TEST.PD.PROT.SNK.4 SinkWaitCapTimer Timeout	NA
63	TEST.PD.PROT.SNK.5	TEST.PD.PROT.SNK.5 SenderResponseTimer Deadline	NA
64	TEST.PD.PROT.SNK.6	TEST.PD.PROT.SNK.6 SenderResponseTimer Timeout	NA
65	TEST.PD.PROT.SNK.7	TEST.PD.PROT.SNK.7 PSTransitionTimer Timeout	NA
66	TEST.PD.PROT.SNK.8	TEST.PD.PROT.SNK.8 Atomic Message Sequence – Accept	NA
67	TEST.PD.PROT.SNK.9	TEST.PD.PROT.SNK.9 Atomic Message Sequence – PS_RDY	NA
68	TEST.PD.PROT.SNK.10	TEST.PD.PROT.SNK.10 DR_Swap Request	NA
69	TEST.PD.PROT.SNK.11	TEST.PD.PROT.SNK.11 VCONN_Swap Request	NA
70	TEST.PD.PROT.SNK.12	TEST.PD.PROT.SNK.12 PR_Swap – PSSourceOffTimer Timeout	NA
71	TEST.PD.PROT.SNK.13	TEST.PD.PROT.SNK.13 PR_Swap – Request SenderResponseTimer Timeout	NA
72	TEST.PD.PROT.SNK.14	TEST.PD.PROT.SNK.14 Valid Use of GoodCRC on Power up	NA
73	TEST.PD.PROT.SNK3.1	TEST.PD.PROT.SNK3.1 Get_Source_Cap_Extended	NA
74	TEST.PD.PROT.SNK3.2	TEST.PD.PROT.SNK3.2 Alert Response Source Input Change	NA
75	TEST.PD.PROT.SNK3.3	TEST.PD.PROT.SNK3.3 Alert Response Battery Status Change	NA
76	TEST.PD.PROT.SNK3.4	TEST.PD.PROT.SNK3.4 Soft_Reset Sent Regardless of Rp Value	NA
77	TEST.PD.PROT.SNK3.5	TEST.PD.PROT.SNK3.5 Sink PPS Normal Operation	NA
78	TEST.PD.PROT.SNK3.6	TEST.PD.PROT.SNK3.6 Revision Number Test	NA
79	TEST.PD.PROT.SNK3.7	TEST.PD.PROT.SNK3.7 GoodCRC Specification Revision Compatibility	NA
80	TEST.PD.PROT.SNK3.9	TEST.PD.PROT.SNK3.9 Alert Response Extended Alert	NA
81	TEST.PD.VDM.SNK.1	TEST.PD.VDM.SNK.1 Discovery Process and Enter Mode	NA



SI No	Test ID	Test Name	Test Result
82	TEST.PD.VDM.SNK.2	TEST.PD.VDM.SNK.2 Exit Mode without Entering	NA
83	TEST.PD.VDM.SNK.5	TEST.PD.VDM.SNK.5 DR Swap in Modal Operation	NA
84	TEST.PD.VDM.SNK.6	TEST.PD.VDM.SNK.6 Structured VDM Revision Number Test	NA
85	TEST.PD.VDM.SNK.7	TEST.PD.VDM.SNK.7 Unrecognized VID in Unstructured VDM	NA
86	TEST.PD.VDM.CBL.1	TEST.PD.VDM.CBL.1 Discovery Process and Enter Mode	NA
87	TEST.PD.VDM.SRC.1	TEST.PD.VDM.SRC.1 Discovery Process and Enter Mode	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.246s and Sourcecap time: 1.424s [PASS] Max = 250ms. Obtained time difference is 178.316ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet21	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 42.669ms Packet 23	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 4.415s and Sourcecap time: 4.588s [PASS] Max = 250ms. Obtained time difference is 173.316ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet71	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 42.695ms Packet 73	PASS
		Rev2Src	PASS
		Discover ID Response Check - TEST.PD.VDM.SRC.1#1 >>UUT respond to Discover_ID within the min 24ms and max 30ms.Obtained time difference is 5.66961 ms	PASS
		Discover ID ACK Response Check - TEST.PD.VDM.SRC.1#3	PASS
		Attention Request message - TEST.PD.VDM.SRC.1#4	PASS
		Rev3ChkdSrc	PASS

SI No	Test ID	Test Name	Test Result
		Discover ID Response Check - TEST.PD.VDM.SRC.1#2 >>UUT responds with a "Responder_ACK" message at protocol index 96 and VIF field Responds_To_Discov_SOP_DFP = YES, Responds_To_Discov_SOP_UFP = YES and Attempts_Discov_SOP = YES.	PASS
		Discover ID ACK Check - TEST.PD.VDM.SRC.1#3	PASS
		Data_Capable_as_USB_Host_SOP >>[PASS] B[31] does match VIF field Data_Capable_as_USB_Host VIF data : YES and DUT data : NO	PASS
		Data_Capable_as_USB_Device_SOP >>[PASS] B[30] does match VIF field Data_Capable_as_USB_Device VIF data : YES and DUT data : NO	PASS
		Product_Type_UFP_SOP >>[PASS] B29...27 does match VIF field Product_Type_UFP_SOP VIF data : Peripheral and DUT data : Undefined	PASS
		Modal_Operation_Supported_SOP >>VIF data : NO and DUT data : NO	PASS
		Product_Type_DFP_SOP >>[PASS] B25...23 does match VIF field Product_Type_DFP_SOP VIF data : Host and DUT data : Undefined	PASS
		ID_Header_Connector_Type >>VIF data : USB_Type_C_Receptacle and DUT data : USB_Type_C_Receptacle	PASS
		B20...16 is set to zero	PASS
		USB_VID_SOP >>VIF data : 344F and DUT data : 344F	PASS
		Cert Sat VDO Check >>VIF data : 0 and DUT data : 0	PASS
		Product VDO Check >>VIF data : 0 and DUT data : 0 VIF data : 0 and DUT data : 0	PASS
		Attention Request message - TEST.PD.VDM.SRC.1#4	PASS
88	TEST.PD.VDM.SRC.2	TEST.PD.VDM.SRC.2 Invalid Fields – Discover Identity	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src	PASS

SI No	Test ID	Test Name	Test Result
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.224s and Sourcecap time: 1.402s [PASS] Max = 250ms. Obtained time difference is 177.482ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet21	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 42.341ms Packet 23	PASS
		COMMON.PROC.BU.1 - REVISION 3 0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 4.349s and Sourcecap time: 4.526s [PASS] Max = 250ms. Obtained time difference is 176.649ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet68	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 41.297ms Packet 70	PASS
		Rev2Src	PASS
		Discover_ID Response Check - TEST.PD.VDM.SRC.2#1 >>UUT responded with Responder_NAK at protocol index 46	PASS
		Rev3ChkdSrc	PASS
		Discover_ID Response Check - TEST.PD.VDM.SRC.2#1 >>UUT responded with Responder_NAK at protocol index 93	PASS
89	TEST.PD.VDM.CBL3.1	TEST.PD.VDM.CBL3.1 Revision Number Test	NA
90	TEST.PD.PS.SRC.1	TEST.PD.PS.SRC.1 Multiple Request Messages	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION 2 0 Rev2Src	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.309s and Sourcecap time: 1.484s [PASS] Max = 250ms. Obtained time difference is 175.23ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet21	PASS

SI No	Test ID	Test Name	Test Result
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 43.027ms Packet 23	PASS
		COMMON.PROC.BU.1 - REVISION 3 0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 9.236s and Sourcecap time: 9.413s [PASS] Max = 250ms. Obtained time difference is 177.111ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet129	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 42.627ms Packet 131	PASS
		Rev2Src >> Rev2Src sequence starts from protocol index 5	PASS
		>>PDO : 1 transition with operating current 0	PASS
		>>PDO : 1 transition with operating current 0.25	PASS
		>>PDO : 1 transition with operating current 0.5	PASS
		>>PDO : 1 transition with operating current 0.75	PASS
		>>PDO : 1 transition with operating current 1	PASS
		>>PDO : 1 transition with operating current 0.75	PASS
		>>PDO : 1 transition with operating current 0.5	PASS
		>>PDO : 1 transition with operating current 0.25	PASS
		>>PDO : 1 transition with operating current 0	PASS

SI No	Test ID	Test Name	Test Result
		Transition (no PDO change) - Current Decrease - TEST.PD.PS.SRC.1#1 >>Load set to 0.75A: [PASS] Vbus voltage before load decrease: 4.95V , Limit:[4.75V - 5.5V] at Protocol index : 78. Measurement after timestamp : 5.39512627S] Load set to 0.5A: [PASS] Vbus voltage before load decrease: 5V , Limit:[4.75V - 5.5V] at Protocol index : 86. Measurement after timestamp : 5.99912405S] Load set to 0.25A: [PASS] Vbus voltage before load decrease: 5.05V , Limit:[4.75V - 5.5V] at Protocol index : 94. Measurement after timestamp : 6.60312504S] Load set to 0A: [PASS] Vbus voltage before load decrease: 5.1V , Limit:[4.75V - 5.5V] at Protocol index : 102. Measurement after timestamp : 7.20713565S]	PASS
		Transition (no PDO change) - Current Increase - TEST.PD.PS.SRC.1#2 >>Load set to 0.25A: [PASS] Vbus voltage before load increase: 5.05V , Limit:[4.75V - 5.5V] at Protocol index : 46. Measurement after timestamp : 2.97911911S] Load set to 0.5A: [PASS] Vbus voltage before load increase: 5V , Limit:[4.75V - 5.5V] at Protocol index : 54. Measurement after timestamp : 3.58311692S] Load set to 0.75A: [PASS] Vbus voltage before load increase: 4.95V , Limit:[4.75V - 5.5V] at Protocol index : 62. Measurement after timestamp : 4.18712110S] Load set to 1A: [PASS] Vbus voltage before load increase: 4.9V , Limit:[4.75V - 5.5V] at Protocol index : 70. Measurement after timestamp : 4.79112210S]	PASS
		Transition (PDO change) - TEST.PD.PS.SRC.1#3	PASS
		Vbus transition - Slew measurement - TEST.PD.PS.SRC.1#4	PASS
		VSrcValid limit - TEST.PD.PS.SRC.1#5	PASS
		Vbus voltage measurement - TEST.PD.PS.SRC.1#6	PASS
		Validate PS_RDY before Vbus - TEST.PD.PS.SRC.1#7	PASS
		Vbus voltage measurement - TEST.PD.PS.SRC.1#8	PASS
		PPS Transition - Current Decrease - TEST.PD.PS.SRC.1#9	PASS
		Validate Request Sequence - TEST.PD.PS.SRC.1#10 >>DUT responded with Accept at the protocol index 40	PASS
		Validate PS_RDY message - TEST.PD.PS.SRC.1#11 >>[PASS] Max = 325ms. Obtained time difference is 37.584ms Packet 42	PASS

SI No	Test ID	Test Name	Test Result
		Validate Source_Capability message - TEST.PD.PS.SRC.1#12	PASS
		Validate PS_RDY message - TEST.PD.PS.SRC.1#13	PASS
		Primary Check	PASS
		Load Check >>Configured Eload value is 0.25 A at packet index 52 and measured is 0.2671 A at time 3.03001849s	PASS
		Load Check >>Configured Eload value is 0.5 A at packet index 60 and measured is 0.5169 A at time 3.63119764s	PASS
		Load Check >>Configured Eload value is 0.75 A at packet index 68 and measured is 0.7659 A at time 4.23388552s	PASS
		Load Check >>Configured Eload value is 1 A at packet index 76 and measured is 1.0156 A at time 4.84130761s	PASS
		Load Check >>Configured Eload value is 0.75 A at packet index 82 and measured is 0.7661 A at time 5.40641776s	PASS
		Load Check >>Configured Eload value is 0.5 A at packet index 90 and measured is 0.5169 A at time 6.01062253s	PASS
		Load Check >>Configured Eload value is 0.25 A at packet index 98 and measured is 0.2674 A at time 6.61457062s	PASS
		Rev3ChkdSrc >> Rev3ChkdSrc sequence starts from protocol index 113	PASS
		>>PDO : 1 transition with operating current 0	PASS
		>>PDO : 1 transition with operating current 0.25	PASS
		>>PDO : 1 transition with operating current 0.5	PASS
		>>PDO : 1 transition with operating current 0.75	PASS



SI No	Test ID	Test Name	Test Result
		>>PDO : 1 transition with operating current 1	PASS
		>>PDO : 1 transition with operating current 0.75	PASS
		>>PDO : 1 transition with operating current 0.5	PASS
		>>PDO : 1 transition with operating current 0.25	PASS
		>>PDO : 1 transition with operating current 0	PASS
		Transition (no PDO change) - Current Decrease - TEST.PD.PS.SRC.1#1 >>Load set to 0.75A: [PASS] Vbus voltage before load decrease: 4.95V , Limit:[4.75V - 5.5V] at Protocol index : 186. Measurement after timestamp : 13.3510979S] Load set to 0.5A: [PASS] Vbus voltage before load decrease: 5V , Limit:[4.75V - 5.5V] at Protocol index : 194. Measurement after timestamp : 13.9551021S] Load set to 0.25A: [PASS] Vbus voltage before load decrease: 5.05V , Limit:[4.75V - 5.5V] at Protocol index : 202. Measurement after timestamp : 14.5590999S] Load set to 0A: [PASS] Vbus voltage before load decrease: 5.1V , Limit:[4.75V - 5.5V] at Protocol index : 210. Measurement after timestamp : 15.1631042S]	PASS
		Transition (no PDO change) - Current Increase - TEST.PD.PS.SRC.1#2 >>Load set to 0.25A: [PASS] Vbus voltage before load increase: 5.05V , Limit:[4.75V - 5.5V] at Protocol index : 154. Measurement after timestamp : 10.9350939S] Load set to 0.5A: [PASS] Vbus voltage before load increase: 5V , Limit:[4.75V - 5.5V] at Protocol index : 162. Measurement after timestamp : 11.5390981S] Load set to 0.75A: [PASS] Vbus voltage before load increase: 4.95V , Limit:[4.75V - 5.5V] at Protocol index : 170. Measurement after timestamp : 12.1430959S] Load set to 1A: [PASS] Vbus voltage before load increase: 4.9V , Limit:[4.75V - 5.5V] at Protocol index : 178. Measurement after timestamp : 12.7471001S]	PASS
		Transition (PDO change) - TEST.PD.PS.SRC.1#3	PASS
		Vbus transition - Slew measurement - TEST.PD.PS.SRC.1#4	PASS

SI No	Test ID	Test Name	Test Result
		VSrcValid limit - TEST.PD.PS.SRC.1#5	PASS
		Vbus voltage measurement - TEST.PD.PS.SRC.1#6	PASS
		Validate PS_RDY before Vbus - TEST.PD.PS.SRC.1#7	PASS
		Vbus voltage measurement - TEST.PD.PS.SRC.1#8	PASS
		PPS Transition - Current Decrease - TEST.PD.PS.SRC.1#9	PASS
		Validate Request Sequence - TEST.PD.PS.SRC.1#10 >>DUT responded with Accept at the protocol index 148	PASS
		Validate PS_RDY message - TEST.PD.PS.SRC.1#11 >>[PASS] Max = 325ms. Obtained time difference is 37.101ms Packet 150	PASS
		Validate Source_Capability message - TEST.PD.PS.SRC.1#12	PASS
		Validate PS_RDY message - TEST.PD.PS.SRC.1#13	PASS
		Primary Check	PASS
		Load Check >>Configured Eload value is 0.25 A at packet index 160 and measured is 0.2673 A at time 10.98133856s	PASS
		Load Check >>Configured Eload value is 0.5 A at packet index 168 and measured is 0.5169 A at time 11.58548033s	PASS
		Load Check >>Configured Eload value is 0.75 A at packet index 176 and measured is 0.7661 A at time 12.19153836s	PASS
		Load Check >>Configured Eload value is 1 A at packet index 184 and measured is 1.0155 A at time 12.79506144s	PASS
		Load Check >>Configured Eload value is 0.75 A at packet index 190 and measured is 0.7663 A at time 13.36833598s	PASS
		Load Check >>Configured Eload value is 0.5 A at packet index 198 and measured is 0.5169 A at time 13.96614556s	PASS
		Load Check >>Configured Eload value is 0.25 A at packet index 206 and measured is 0.2675 A at time 14.57109196s	PASS

SI No	Test ID	Test Name	Test Result
91	TEST.PD.PS.SRC.2	TEST.PD.PS.SRC.2 PDO Transition	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.21s and Sourcecap time: 1.385s [PASS] Max = 250ms. Obtained time difference is 175.461ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet21	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 41.996ms Packet 23	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 4.335s and Sourcecap time: 4.513s [PASS] Max = 250ms. Obtained time difference is 178.035ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet64	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 41.591ms Packet 66	PASS
		Rev2Src	PASS
		PDO Transistion in PD2.0 Mode	PASS
		>>PDO Transition 1 to 1	PASS
		Check Accept - TEST.PD.PS.SRC.2#1	PASS
		Check PsRdy - TEST.PD.PS.SRC.2#2 >>[PASS] Max = 325ms. Obtained time difference is 41.996ms Packet 23	PASS
		Check Vbus is within the vSrcNew or vPpsNew - TEST.PD.PS.SRC.2#3	PASS
		Vbus transition - TEST.PD.PS.SRC.2#4	PASS
		Vbus transition - TEST.PD.PS.SRC.2#5	PASS
		Vbus transition - TEST.PD.PS.SRC.2#6	PASS
		UUT does not send PS_RDY before the VBUS is within vSrcNew or vPpsNew - TEST.PD.PS.SRC.2#7	PASS

SI No	Test ID	Test Name	Test Result
		Check Source Capability matches VIF - TEST.PD.PS.SRC.2#8	PASS
		Check Accept - TEST.PD.PS.SRC.2#9	PASS
		Rev3ChkdSrc	PASS
		PDO Transistion in PD3.0 Mode	PASS
		>>PDO Transition 1 to 1	PASS
		Check Accept - TEST.PD.PS.SRC.2#1	PASS
		Check PsRdy - TEST.PD.PS.SRC.2#2	PASS
		>>[PASS] Max = 325ms. Obtained time difference is 41.591ms Packet 66	
		Check Vbus is within the vSrcNew or vPpsNew - TEST.PD.PS.SRC.2#3	PASS
		Vbus transition - TEST.PD.PS.SRC.2#4	PASS
		Vbus transition - TEST.PD.PS.SRC.2#5	PASS
		Vbus transition - TEST.PD.PS.SRC.2#6	PASS
		UUT does not send PS_RDY before the VBUS is within vSrcNew or vPpsNew - TEST.PD.PS.SRC.2#7	PASS
		Check Source Capability matches VIF - TEST.PD.PS.SRC.2#8	PASS
		Check Accept - TEST.PD.PS.SRC.2#9	PASS
92	TEST.PD.PS.SRC.3	TEST.PD.PS.SRC.3 Initial Source PDO Transition Post PR Swap	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.332s and Sourcecap time: 1.51s [PASS] Max = 250ms. Obtained time difference is 178.316ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet22	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 41.157ms Packet 24	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 20.341s and Sourcecap time: 20.52s [PASS] Max = 250ms. Obtained time difference is 179.149ms	PASS

SI No	Test ID	Test Name	Test Result
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet102	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 41.969ms Packet 104	PASS
		Rev2Src	PASS
		PR_Swap Response Check - TEST.PD.PS.SRC.3#1 >>DRP UUT sent Accept for PR_Swap message.	PASS
		UUT PS_RDY Check - TEST.PD.PS.SRC.3#2 >UUT respond PS_RDY message to PR_SWAP, but VBUS voltage within vSafe0V(0V - 0.8V). The present voltage is 0.4067V	PASS
		Tester PS_RDY Check - TEST.PD.PS.SRC.3#3 >>UUT sent PS_RDY within tSrcTransition_Max(35ms) + tSrcSwapStdbby_Max(650ms) time. The time interval is 0.0505s, start time 2.4309s, stop time 2.4815s	PASS
		Source capability check after PR_SWAP - TEST.PD.PS.SRC.3#4	PASS
		Accept Check for PR_Swap - TEST.PD.PS.SRC.3#5	PASS
		Accept Check for PR_Swap - TEST.PD.PS.SRC.3#6	PASS
		Accept Check for PR_Swap - TEST.PD.PS.SRC.3#7	PASS
		Current drawn by the DUT - TEST.PD.PS.SRC.3#8 >>Supply Type is Fixed	PASS
		Request Check - TEST.PD.PS.SRC.3#9	PASS
		Accept Check - TEST.PD.PS.SRC.3#10	PASS
		Accept Check - TEST.PD.PS.SRC.3#11	PASS
		Accept Check - TEST.PD.PS.SRC.3#12 >>Current drawn by UUT did not exceed previously contracted current (3.01mA) measured from time 8.24068804s to 8.44068804s	PASS
		Current drawn by the DUT - TEST.PD.PS.SRC.3#13 >>Supply Type is Fixed	PASS
		Request Check - TEST.PD.PS.SRC.3#14 >>Tester sent SourceCap message Packet 74 UUT sent Request message Packet 76	PASS

SI No	Test ID	Test Name	Test Result
		Accept Check - TEST.PD.PS.SRC.3#17 >>Tester sent Accept message Packet 78 UUT is drawing power pSnkSusp max 25mW	PASS
		Current drawn by the DUT - TEST.PD.PS.SRC.3#18 >>Tester sent PS_RDY message Packet 80 Supply Type is Fixed UUT is drawing power current PDO at time 13.72812016s ,Obt Current = 1.864 A.	PASS
		Current drawn by the DUT - TEST.PD.PS.SRC.3#19	PASS
		Rev3ChkdSrc	PASS
		PR_Swap Response Check - TEST.PD.PS.SRC.3#1 >>Tester sent Hard Reset message. MsgID Exp:0 Obt: 0	PASS
		UUT PS_RDY Check - TEST.PD.PS.SRC.3#2	PASS
		Tester PS_RDY Check - TEST.PD.PS.SRC.3#3	PASS
		Source capability check after PR_SWAP - TEST.PD.PS.SRC.3#4	PASS
		Accept Check for PR_Swap - TEST.PD.PS.SRC.3#5	PASS
		Accept Check for PR_Swap - TEST.PD.PS.SRC.3#6	PASS
		Accept Check for PR_Swap - TEST.PD.PS.SRC.3#7	PASS
		Current drawn by the DUT - TEST.PD.PS.SRC.3#8	PASS
		Request Check - TEST.PD.PS.SRC.3#9	PASS
		Accept Check - TEST.PD.PS.SRC.3#10	PASS
		Accept Check - TEST.PD.PS.SRC.3#11	PASS
		Accept Check - TEST.PD.PS.SRC.3#12	PASS
		Current drawn by the DUT - TEST.PD.PS.SRC.3#13	PASS
93	TEST.PD.PS.SRC.4	TEST.PD.PS.SRC.4 Source Behavior with Capability Mismatch Bit	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.171s and Sourcecap time: 1.349s [PASS] Max = 250ms. Obtained time difference is 177.482ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet21	PASS



SI No	Test ID	Test Name	Test Result
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 39.587ms Packet 23	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 4.283s and Sourcecap time: 4.457s [PASS] Max = 250ms. Obtained time difference is 174.149ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet64	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 41.112ms Packet 66	PASS
		Rev2Src	PASS
		PDO Transistion in REVISION_2_0 Mode	PASS
		>>PDO Transition 1 to 1	PASS
		Check Accept - TEST.PD.PS.SRC.4#1 >>Accept recieved at protocol index 40	PASS
		Check PS_RDY - TEST.PD.PS.SRC.4#2 >>PS_RDY recieved at protocol index 42	PASS
		Check PS_RDY recive time - TEST.PD.PS.SRC.4#3 >>[PASS] Max = 325ms. Obtained time difference is 34.993ms Packet 42	PASS
		Check Accept - TEST.PD.PS.SRC.4#4	PASS
		Check PS_RDY - TEST.PD.PS.SRC.4#5	PASS
		Check PS_RDY receive time - TEST.PD.PS.SRC.4#6	PASS
		Check SourceCap matches VIF - TEST.PD.PS.SRC.4#7	PASS
		Rev3ChkdSrc	PASS
		PDO Transistion in REVISION_3_0 Mode	PASS
		>>PDO Transition 1 to 1	PASS
		Check Accept - TEST.PD.PS.SRC.4#1 >>Accept recieved at protocol index 83	PASS

SI No	Test ID	Test Name	Test Result
		Check PS_RDY - TEST.PD.PS.SRC.4#2 >>PS_RDY recieved at protocol index 85	PASS
		Check PS_RDY recive time - TEST.PD.PS.SRC.4#3 >>[PASS] Max = 325ms. Obtained time difference is 37.681ms Packet 85	PASS
		Check Accept - TEST.PD.PS.SRC.4#4	PASS
		Check PS_RDY - TEST.PD.PS.SRC.4#5	PASS
		Check PS_RDY receive time - TEST.PD.PS.SRC.4#6	PASS
		Check SourceCap matches VIF - TEST.PD.PS.SRC.4#7	PASS
94	TEST.PD.PS.SRC.5	TEST.PD.PS.SRC.5 Source Hard Reset Test	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.203s and Sourcecap time: 1.375s [PASS] Max = 250ms. Obtained time difference is 172.483ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet21	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 42.325ms Packet 23	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 5.721s and Sourcecap time: 5.895s [PASS] Max = 250ms. Obtained time difference is 174.149ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet79	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 41.896ms Packet 81	PASS
		Rev2Src	PASS
		Check VBUS stays within present valid voltage range - TEST.PD.PS.SRC.5#1 >>Vbus stay within present valid voltage range for tPSHardReset min. Measured volt at 2.31550615s	PASS

SI No	Test ID	Test Name	Test Result
		Check VBUS reaches vSafe0V max - TEST.PD.PS.SRC.5#2 >>VBUS reaches vSafe0V max at 2.3513369 S	PASS
		Check VBUS rises above vSafe0V max - TEST.PD.PS.SRC.5#3 >>VBUS staying below 0.8 V for duration tSrcRecover min VBUS rise above vSafe0V max after 0.716661 S. Measured at 3.0679979 S	PASS
		Check VBUS reaches vSafe5V - TEST.PD.PS.SRC.5#4 >>VBUS reaches vSafe5V within 3.08549615 S	PASS
		Source Capabilities message - TEST.PD.PS.SRC.5#5 >>DUT sent Src Cap at 3.24163s.Vbus reached vsafe5v 3.06665s. Tester transmits Source Cap within tFirstSourceCap max 0.17498s	PASS
		Highest Fixed PDO Contract check - TEST.PD.PS.SRC.5#6 >>DUT has no highest fixed PDO availability	PASS
		Check VBUS stays within present valid voltage range - TEST.PD.PS.SRC.5#7	PASS
		Check VBUS reaches vSafe5V max - TEST.PD.PS.SRC.5#8	PASS
		Check VBUS reaches vSafe0V max - TEST.PD.PS.SRC.5#9	PASS
		Check VBUS rises above vSafe0V max - TEST.PD.PS.SRC.5#10	PASS
		Check VBUS reaches vSafe5V - TEST.PD.PS.SRC.5#11	PASS
		Source Capabilities message - TEST.PD.PS.SRC.5#12	PASS
		Rev3ChkdSrc	PASS
		Check VBUS stays within present valid voltage range - TEST.PD.PS.SRC.5#1 >>Vbus stay within present valid voltage range for tPSHardReset min. Measured volt at 6.82951219s	PASS
		Check VBUS reaches vSafe0V max - TEST.PD.PS.SRC.5#2 >>VBUS reaches vSafe0V max at 6.86784269 S	PASS
		Check VBUS rises above vSafe0V max - TEST.PD.PS.SRC.5#3 >>VBUS staying below 0.8 V for duration tSrcRecover min VBUS rise above vSafe0V max after 0.72249375 S. Measured at 7.59033644 S	PASS
		Check VBUS reaches vSafe5V - TEST.PD.PS.SRC.5#4 >>VBUS reaches vSafe5V within 7.60700144 S	PASS
		Source Capabilities message - TEST.PD.PS.SRC.5#5 >>DUT sent Src Cap at 7.76188s.Vbus reached vsafe5v 7.58857s. Tester transmits Source Cap within tFirstSourceCap max 0.17332s	PASS

SI No	Test ID	Test Name	Test Result
		Highest Fixed PDO Contract check - TEST.PD.PS.SRC.5#6 >>DUT has no highest fixed PDO availability	PASS
		Check VBUS stays within present valid voltage range - TEST.PD.PS.SRC.5#7	PASS
		Check VBUS reaches vSafe5V max - TEST.PD.PS.SRC.5#8	PASS
		Check VBUS reaches vSafe0V max - TEST.PD.PS.SRC.5#9	PASS
		Check VBUS rises above vSafe0V max - TEST.PD.PS.SRC.5#10	PASS
		Check VBUS reaches vSafe5V - TEST.PD.PS.SRC.5#11	PASS
		Source Capabilities message - TEST.PD.PS.SRC.5#12	PASS
95	TEST.PD.PS.SNK.1	TEST.PD.PS.SNK.1 PDO Transition	NA
96	TEST.PD.PS.SNK.2	TEST.PD.PS.SNK.2 Initial Sink PDO Transition	NA
97	TEST.PD.PS.SNK.3	TEST.PD.PS.SNK.3 Multiple Request Load Test Post PR Swap	NA
98	TEST.PD.EPR.SRC3.1	TEST.PD.EPR.SRC3.1 EPR Entry Process - UUT as VCONN Source	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.197s and Sourcecap time: 1.371s [PASS] Max = 250ms. Obtained time difference is 174.149ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet21	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 40.259ms Packet 23	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 9.702s and Sourcecap time: 9.881s [PASS] Max = 250ms. Obtained time difference is 179.149ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet80	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 40.117ms Packet 82	PASS
		Rev3ChkdSrc >> Rev3ChkdSrc sequence starts from protocol index 5	PASS

SI No	Test ID	Test Name	Test Result
		EPR Mode check - TEST.PD.EPR.SRC3.1#2 >>UUT did respond with Not_Supported at the protocol index 44 and VIF field EPR_Supported_As_Source is NO Packet 44	PASS
		Vconn_Swap message - TEST.PD.EPR.SRC3.1#3	PASS
		Discover ID SOP1 message check - TEST.PD.EPR.SRC3.1#4	PASS
		EPR Mode Enter Succeeded message check - TEST.PD.EPR.SRC3.1#5	PASS
		EPR_Source_Capability message check - TEST.PD.EPR.SRC3.1#6	PASS
		Accept message check - TEST.PD.EPR.SRC3.1#7	PASS
		PS_Rdy message check - TEST.PD.EPR.SRC3.1#8	PASS
		Source Cap message check - TEST.PD.EPR.SRC3.1#9	PASS
		Source Cap message Detail check - TEST.PD.EPR.SRC3.1#10	PASS
		Source Cap message Detail check - TEST.PD.EPR.SRC3.1#11	PASS
		Wait response check - TEST.PD.EPR.SRC3.1#12	PASS
		EPR Get Sourcecap Check - TEST.PD.EPR.SRC3.1#13 >>Tester sent Extended_Control EPR_Get_Source_Cap message Packet 37 UUT responded with Not_Supported.UUT is DRP , VIF field EPR_Supported_As_Src is NO and VIF field EPR_Supported_As_Snk is NO	PASS
		Rev3UnchkdSrc >> Rev3UnchkdSrc sequence starts from protocol index 63	PASS
		EPR Mode check - TEST.PD.EPR.SRC3.1#2 >>UUT did respond with Not_Supported at the protocol index 103 and VIF field EPR_Supported_As_Source is NO Packet 103	PASS
		Vconn_Swap message - TEST.PD.EPR.SRC3.1#3	PASS
		Discover ID SOP1 message check - TEST.PD.EPR.SRC3.1#4	PASS
		EPR Mode Enter Succeeded message check - TEST.PD.EPR.SRC3.1#5	PASS
		EPR_Source_Capability message check - TEST.PD.EPR.SRC3.1#6	PASS
		Accept message check - TEST.PD.EPR.SRC3.1#7	PASS
		PS_Rdy message check - TEST.PD.EPR.SRC3.1#8	PASS
		Source Cap message check - TEST.PD.EPR.SRC3.1#9	PASS
		Source Cap message Detail check - TEST.PD.EPR.SRC3.1#10	PASS

SI No	Test ID	Test Name	Test Result
		Source Cap message Detail check - TEST.PD.EPR.SRC3.1#11	PASS
		Wait response check - TEST.PD.EPR.SRC3.1#12	PASS
		EPR Get Sourcecap Check - TEST.PD.EPR.SRC3.1#13 >>Tester sent Extended_Control EPR_Get_Source_Cap message Packet 96 UUT responded with Not_Supported.UUT is DRP , VIF field EPR_Supported_As_Src is NO and VIF field EPR_Supported_As_Snk is NO	PASS
99	TEST.PD.EPR.SRC3.2	TEST.PD.EPR.SRC3.2 EPR Entry Process - Tester as VCONN Source	NA
		--- EPR_Supported_As_Src is set to NO in VIF	
100	TEST.PD.EPR.SRC3.3	TEST.PD.EPR.SRC3.3 EPR Entry failed - EPR Mode Capable bit not set in RDO	NA
		--- EPR_Supported_As_Src is set to NO in VIF	
101	TEST.PD.EPR.SRC3.4	TEST.PD.EPR.SRC3.4 EPR Entry failed – Tester as VCONN source	NA
		--- EPR_Supported_As_Src is set to NO in VIF	
102	TEST.PD.EPR.SRC3.5	TEST.PD.EPR.SRC3.5 EPR Entry Failed - EPR_Mode(Reserved) message	NA
		--- EPR_Supported_As_Src is set to NO in VIF	
103	TEST.PD.EPR.SRC3.6	TEST.PD.EPR.SRC3.6 EPR Entry Failed - Cable not EPR capable	NA
		--- EPR_Supported_As_Src is set to NO in VIF	
104	TEST.PD.EPR.SRC3.7	TEST.PD.EPR.SRC3.7 EPR Entry Failed - Interrupted by EPR_Get_Sink_Cap message	NA
		--- EPR_Supported_As_Src is set to NO in VIF	
105	TEST.PD.EPR.SRC3.8	TEST.PD.EPR.SRC3.8 EPR mode - Request message response	NA
		--- EPR_Supported_As_Src is set to NO in VIF	
106	TEST.PD.EPR.SRC3.9	TEST.PD.EPR.SRC3.9 EPR mode - EPR_Get_Source_Cap message	NA
		--- EPR_Supported_As_Src is set to NO in VIF	
107	TEST.PD.EPR.SRC3.10	TEST.PD.EPR.SRC3.10 SPR mode - EPR_Get_Source_Cap message	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.265s and Sourcecap time: 1.438s [PASS] Max = 250ms. Obtained time difference is 173.316ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >>Packet21	PASS



SI No	Test ID	Test Name	Test Result
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >>[PASS] Max = 325ms. Obtained time difference is 43.205ms Packet 23	PASS
		Rev3ChkSrc	PASS
		EPR Mode Message Response - TEST.PD.EPR.SRC3.10#1 >>Tester sent Extended_Control EPR_Get_Source_Cap message Packet 37 UUT responded with Not_Supported.UUT is DRP , VIF field EPR_Supported_As_Src is NO and VIF field EPR_Supported_As_Snk is NO at protocol index 39	PASS
		DUT initiates Hard reset - TEST.PD.EPR.SRC3.10#2	NA
108	TEST.PD.EPR.SRC3.11	TEST.PD.EPR.SRC3.11 EPR Mode Exit by EPR_Mode_Exit message	NA
		--- EPR_Supported_As_Src is set to NO in VIF	
109	TEST.PD.EPR.SRC3.12	TEST.PD.EPR.SRC3.12 EPR mode - Get_Source_Cap message and Request message response	NA
		--- EPR_Supported_As_Src is set to NO in VIF	
110	TEST.PD.EPR.SRC3.13	TEST.PD.EPR.SRC3.13 EPR mode - tSourceEPRKeepAlive Timeout	NA
		--- EPR_Supported_As_Src is set to NO in VIF	
111	TEST.PD.EPR.SRC3.14	TEST.PD.EPR.SRC3.14 EPR mode - EPR_Request with Incorrect copy of PDO	NA
		--- EPR_Supported_As_Src is set to NO in VIF	
112	TEST.PD.EPR.SRC3.15	TEST.PD.EPR.SRC3.15 DiscoverIdentityCounter and DiscoverIdentityTimer check for SOP1	NA
		--- EPR_Supported_As_Src is set to NO in VIF Captive_Cable is set to NO in VIF	
113	TEST.PD.EPR.SNK3.1	TEST.PD.EPR.SNK3.1 EPR Entry Process - Success	NA
114	TEST.PD.EPR.SNK3.2	TEST.PD.EPR.SNK3.2 EPR Entry Fail tEnterEPR Timer Timeout	NA
115	TEST.PD.EPR.SNK3.3	TEST.PD.EPR.SNK3.3 EPR Fail by EPR Enter Failed Message	NA
116	TEST.PD.EPR.SNK3.4	TEST.PD.EPR.SNK3.4 EPR Entry Fail tFirstSourceCap Timer Timeout	NA
117	TEST.PD.EPR.SNK3.5	TEST.PD.EPR.SNK3.5 EPR Exit by Incorrect EPR Source Cap	NA
118	TEST.PD.EPR.SNK3.6	TEST.PD.EPR.SNK3.6 EPR Exit by EPR Exit Message	NA
119	TEST.PD.EPR.SNK3.7	TEST.PD.EPR.SNK3.7 EPR Fail by Wait Message	NA
120	TEST.PD.EPR.SNK3.8	TEST.PD.EPR.SNK3.8 EPR Exit by Source Cap Message	NA
121	TEST.PD.EPR.SNK3.9	TEST.PD.EPR.SNK3.9 EPR Entry failed due to SourceCap	NA

SI No	Test ID	Test Name	Test Result
122	TEST.PD.EPR.SNK3.10	TEST.PD.EPR.SNK3.10 EPR Exit fail due to SinkWaitCapTimer timeout	NA
123	TEST.PD.PS.EPR.SRC3.1	TEST.PD.PS.EPR.SRC3.1 Multiple EPR Request Load Test	NA
		--- EPR_Supported_As_Src is set to NO in VIF	
124	TEST.PD.PS.EPR.SRC3.2	TEST.PD.PS.EPR.SRC3.2 PDO Transitions in EPR Mode	NA
		--- EPR_Supported_As_Src is set to NO in VIF	
125	TEST.PD.FRS.SRC3.1	TEST.PD.FRS.SRC3.1 Normal Conditions	NA
126	TEST.PD.FRS.SRC3.2	TEST.PD.FRS.SRC3.2 Provider Only Checks	NA
127	TEST.PD.FRS.SRC3.3	TEST.PD.FRS.SRC3.3 GoodCRC Not Sent In Response To Accept	NA
128	TEST.PD.FRS.SRC3.4	TEST.PD.FRS.SRC3.4 GoodCRC Not Sent In Response To PS_RDY	NA
129	TEST.PD.FRS.SRC3.5	TEST.PD.FRS.SRC3.5 PSSourceOnTimer Deadline	NA
130	TEST.PD.FRS.SRC3.6	TEST.PD.FRS.SRC3.6 PSSourceOnTimer Timeout	NA
131	TEST.PD.FRS.SNK3.1	TEST.PD.FRS.SNK3.1 Normal Conditions	NA
132	TEST.PD.FRS.SNK3.2	TEST.PD.FRS.SNK3.2 Normal Conditions, Consumer Only	NA
133	TEST.PD.FRS.SNK3.3	TEST.PD.FRS.SNK3.3 FR_Swap Not Sent	NA
134	TEST.PD.FRS.SNK3.4	TEST.PD.FRS.SNK3.4 SendResponseTimer Timeout	NA
135	TEST.PD.FRS.SNK3.5	TEST.PD.FRS.SNK3.5 PSSourceOffTimer Deadline	NA
136	TEST.PD.FRS.SNK3.6	TEST.PD.FRS.SNK3.6 PSSourceOffTimer Timeout	NA
137	TEST.PD.FRS.SNK3.7	TEST.PD.FRS.SNK3.7 GoodCRC Not Sent in Response to PS_RDY	NA
138	TEST.PD.USB4.DRST.1	TEST.PD.USB4.DRST.1 –Data_Reset command response of UFP UUT	NA
139	TEST.PD.USB4.DRST.2	TEST.PD.USB4.DRST.2 –Data_Reset command response of UFP UUT, Invalid Sequence	NA
140	TEST.PD.USB4.DRST.3	TEST.PD.USB4.DRST.3 –Data_Reset command response of UFP UUT Sourcing Vconn	NA
141	TEST.PD.USB4.DRST.4	TEST.PD.USB4.DRST.4 –DataReset command response of UFP UUT Sourcing Vconn – Invalid Sequence	NA
142	TEST.PD.USB4.DRST.5	TEST.PD.USB4.DRST.5 –Data_Reset command response of DFP UUT Sourcing Vconn	NA
		--- In VIF Data_Reset_Supported field is NO	
143	TEST.PD.USB4.DRST.6	TEST.PD.USB4.DRST.6 –Data_Reset command response of DFP UUT, UFP Sourcing Vconn	NA
		--- In VIF VCONN_Swap_To_Off_Supported field is NO In VIF Data_Reset_Supported field is NO	

SI No	Test ID	Test Name	Test Result
144	TEST.PD.USB4.DRST.7	TEST.PD.USB4.DRST.7 –Data_reset command response of DFP UUT, UFP Sourcing Vconn- VCONNDISchargeTimer expiry check	NA
		--- In VIF VCONN_Swap_To_Off_Supported field is NO In VIF Data_Reset_Supported field is NO	
145	TEST.PD.USB4.EUSB.1	TEST.PD.USB4.EUSB.1 – Enter_USB Message response of UFP UUT-Valid Mode	NA
		--- In VIF USB4_UFP_Supported field is NONE	
146	TEST.PD.USB4.EUSB.2	TEST.PD.USB4.EUSB.2 – Enter_USB Message response of UFP UUT-Invalid Mode	NA
		--- In VIF USB4_UFP_Supported field is NONE	
147	TEST.PD.USB4.EUSB.3	TEST.PD.USB4.EUSB.3 – Enter_USB Flow-USB4 DFP Connected to USB4 UFP using an Active Cable	NA
		--- In VIF USB4_DFP_Supported field is NONE	
148	TEST.PD.USB4.EUSB.4	TEST.PD.USB4.EUSB.4 – DR_Swap after Entering USB4 Mode entry	NA
		--- In VIF USB4_UFP_Supported field is NONE In VIF USB4_DFP_Supported field is NONE	
149	TEST.PD.USB4.EUSB.5	TEST.PD.USB4.EUSB.5 – tEnterUSBWait check for USB4 DFP	NA
		--- In VIF USB4_DFP_Supported field is NONE	
150	TEST.PD.USB4.CBL.1	TEST.PD.USB4.CBL.1 – Enter_USB Message response of cable UUT-Valid Mode	NA
151	TEST.PD.USB4.CBL.2	TEST.PD.USB4.CBL.2 – Enter_USB Message response of Cable UUT-Invalid Mode	NA
152	2.1	Common Checks	PASS
		Common_Check_PD_1_Check_Preamble - COMMON.CHECK.PD.1	PASS
		Check Preamble sequence and count - COMMON.CHECK.PD.1#1	PASS
		Common_Check_PD_2_Check_Message_Header - COMMON.CHECK.PD.2	PASS
		Check message header fields - COMMON.CHECK.PD.2#1 >>TEST.PD.PROT.SRC.9: Message_ID: Expected val: 0 , Obtained val:0, at Protocol Index 52 Message_ID: Expected val: 0 , Obtained val:0, at Protocol Index 168 Message_ID: Expected val: 0 , Obtained val:0, at Protocol Index 237. Packet52, 168, 237,	PASS

SI No	Test ID	Test Name	Test Result
		Common_Check_PD_3_Check_GoodCRC - COMMON.CHECK.PD.3 > TEST.PD.PHY.ALL.1: Packet40, TEST.PD.PROT.ALL.2: Packet61, 65, 89, TEST.PD.PROT.ALL.3: Packet112, TEST.PD.PROT.ALL3.2: Packet72, 75, TEST.PD.PROT.ALL3.3: Packet72, 75, TEST.PD.PROT.PORT3.3: Packet75, 78, 111, 308, 339, 342, 353, 388, TEST.PD.PROT.PORT3.4: Packet59, 62, 70, 73, TEST.PD.PROT.PORT3.5: Packet72, 75, TEST.PD.PROT.SRC.9: Packet91,	PASS
		Check goodCRC response time - COMMON.CHECK.PD.3#1	PASS

SI No	Test ID	Test Name	Test Result
		<p>Check goodCRC message header fields - COMMON.CHECK.PD.3#2            &gt;&gt;TEST.PD.PROT.ALL.1: Specification Revision. Packet15, 19, 21, 31, 35, 37, 42, 49, 61, 66, 70, 72, 75, 79, 81,            TEST.PD.PROT.ALL.2: Specification Revision. Packet15, 19, 21, 31, 35, 37, 47, 51, 53, 74, 78, 80, 92, 243, 252, 256, 262, 270, 274, 281, 300, 309,            TEST.PD.PROT.ALL.3: Specification Revision. Packet15, 19, 21, 31, 35, 37, 42, 46, 50, 54, 58, 62, 66, 81, 85, 87, 97, 101, 103, 287, 296, 300, 306, 310, 314, 318, 322, 326, 330, 336, 343,            TEST.PD.PROT.ALL.4: Specification Revision. Packet15, 19, 21, 31, 35, 37, 42, 46, 50, 54, 58, 62, 68, 72, 74, 77, 82, 85, 255, 264, 268, 274, 278, 282, 286, 290, 294, 307, 316, 320, 325, 328,            TEST.PD.PROT.ALL.5: Specification Revision. Packet15, 19, 21, 31, 35, 37, 47, 51, 53, 63, 67,            TEST.PD.PROT.SRC.1: Specification Revision. Packet20, 29, 33, 39, 43,            TEST.PD.PROT.SRC.2: Specification Revision. Packet20, 29, 33, 39, 52, 61,            TEST.PD.PROT.SRC.3: Specification Revision. Packet23, 32, 36,            TEST.PD.PROT.SRC.4: Specification Revision. Packet23,            TEST.PD.PROT.SRC.5: Specification Revision. Packet23,            TEST.PD.PROT.SRC.6: Specification Revision. Packet23, 27, 31, 40, 44,            TEST.PD.PROT.SRC.7: Specification Revision. Packet20, 29, 33, 39, 44,            TEST.PD.PROT.SRC.8: Specification Revision. Packet20, 29, 33, 39,            TEST.PD.PROT.SRC.9: Specification Revision. Packet20, 29, 33, 39, 48, 51, 55, 60, 64, 66, 76, 80, 82, 94, 98, 100, 110, 114, 116,            TEST.PD.PROT.SRC.10: Specification Revision. Packet20, 29, 33, 39, 59, 63, 65, 75, 79, 81,            TEST.PD.PROT.SRC.11: Specification Revision. Packet20, 29, 33, 43, 47,            TEST.PD.PROT.SRC.12: Specification Revision. Packet20, 29, 33, 39,            TEST.PD.PROT.SRC.13: Specification Revision. Packet20, 29, 33, 39, 64, 68, 70, 80, 84, 88, 90,            TEST.PD.VDM.SRC.1: Specification Revision. Packet20, 29, 33, 38, 45, 50,            TEST.PD.VDM.SRC.2: Specification Revision. Packet20, 29, 33, 38, 45,            TEST.PD.PS.SRC.1: Specification Revision. Packet20, 29, 33, 39, 47, 55, 63, 71, 79, 87, 95, 103,            TEST.PD.PS.SRC.2: Specification Revision. Packet20, 29, 33, 39,            TEST.PD.PS.SRC.3: Specification Revision. Packet21, 30, 34, 37, 44, 53, 56,            TEST.PD.PS.SRC.4: Specification Revision. Packet20, 29, 33, 39,            TEST.PD.PS.SRC.5: Specification Revision. Packet20, 29, 33, 48, 57,</p>	PASS
		<p>60, 62, 66, 70, 72, 75, 79, 81,            TEST.PD.PS.SRC.4: Specification Revision. Packet20, 29, 33, 39,            TEST.PD.PS.SRC.5: Specification Revision. Packet20, 29, 33, 48, 57,</p>	

SI No	Test ID	Test Name	Test Result
		Common_Check_PD_4_Check_Atomic_Message_Sequence - COMMON.CHECK.PD.4 > TEST.PD.PHY.ALL.3: Packet54, TEST.PD.PROT.ALL3.7: Packet113, TEST_PD_PROT_SRC_9_PR_Swap_Response: Check the PD message and confirm the failure.Packet index: 237 TEST.PD.PROT.SRC.9: Tester Response . Packet38, 154,	PASS



SI No	Test ID	Test Name	Test Result
		<p>Check Atomic message sequence - COMMON.CHECK.PD.4#1            &gt;TEST.PD.PHY.ALL.1: Packet63,            TEST.PD.PHY.ALL.1:            Exp Time: 15ms and obt: 29.58ms. Packet108,            TEST.PD.PHY.ALL.2: Packet36, TEST.PD.PHY.ALL.2:            Exp Time: 15ms and obt: 12.276ms            Exp Time: 15ms and obt: 14.835ms            Exp Time: 15ms and obt: 13.957ms            Exp Time: 15ms and obt: 11.987ms            Exp Time: 15ms and obt: 12.693ms. Packet19, 91, 110, 129, 148,            TEST.PD.PHY.ALL.4:Exp Time: 15ms and obt: 12.681ms            Exp Time: 15ms and obt: 13.978ms. Packet38, 61,            TEST.PD.PHY.ALL.6:Exp Time: 15ms and obt: 13.23ms.            Packet38,            TEST.PD.PHY.ALL.7:Exp Time: 15ms and obt: 14.324ms            Exp Time: 15ms and obt: 14.76ms. Packet37, 113,            TEST.PD.PHY.ALL.8: Packet54, TEST.PD.PHY.ALL.8:            Exp Time: 15ms and obt: 13.105ms. Packet37,            TEST.PD.PHY.ALL.9: Packet89, TEST.PD.PHY.ALL.9:            Exp Time: 15ms and obt: 13.895ms. Packet37,            TEST.PD.PHY.PORT.1: Packet35, T            EST.PD.PHY.PORT.1:            Exp Time: 15ms and obt: 14.304ms. Packet78,            TEST.PD.PROT.ALL.1: Packet117, 171,            TEST.PD.PROT.ALL.1:            Exp Time: 15ms and obt: 14.416ms            Exp Time: 15ms and obt: 12.651ms            Exp Time: 15ms and obt: 14.708ms. Packet32, 100, 135,            TEST.PD.PROT.ALL.3: Packet112, TEST.PD.PROT.ALL.3:            Exp Time: 15ms and obt: 13.133ms            Exp Time: 15ms and obt: 12.852ms            Exp Time: 15ms and obt: 13.862ms            Exp Time: 15ms and obt: 13.885ms            Exp Time: 15ms and obt: 12.863ms</p>	PASS
		<p>This report is generated using GRL-USB-PD Compliance Test Solution ( Version: 1.0.0)            Date: 2025-02-14 : 11:41:15</p>	Page: 93

SI No	Test ID	Test Name	Test Result
		Common_Check_PD_5_Check_Unexpected_Messages_And_Signals - COMMON.CHECK.PD.5	PASS
		Unexpected Soft reset - COMMON.CHECK.PD.5#1 >>TEST.PD.PROT.SRC.9: Unexpected Soft Reset message. Packet241,	PASS
		Unexpected Hard Reset or a cable reset - COMMON.CHECK.PD.5#2 >>TEST.PD.PHY.PORT.1: Unexpected Hard Reset/Cable reset message. Packet109,	PASS
		Unexpected messages - COMMON.CHECK.PD.5#4	PASS
		Common_Check_PD_6_Control_Message - COMMON.CHECK.PD.6	PASS
		Number of data objects in header should be zero - COMMON.CHECK.PD.6#1	PASS
		Common_Check_PD_7_Source_Capability_Message - COMMON.CHECK.PD.7	PASS
		Check Source Capability message - COMMON.CHECK.PD.7#1	PASS
		Check Source Capability message - COMMON.CHECK.PD.7#2	PASS
		Check Data Objects field - COMMON.CHECK.PD.7#3	PASS

SI No	Test ID	Test Name	Test Result
		Check First PDO - COMMON.CHECK.PD.7#4 >>TEST.PD.PHY.PORT.1: Match in Unconstrained Power Field. Packet185, TEST.PD.PROT.ALL.2: Match in Unconstrained Power Field. Packet240, 271, 297, 327, 357, 381, TEST.PD.PROT.ALL.3: Match in Unconstrained Power Field. Packet284, 333, 362, 411, TEST.PD.PROT.ALL.4: Match in Unconstrained Power Field. Packet252, 304, 347, 399, TEST.PD.PROT.ALL3.2: Match in Unconstrained Power Field. Packet179, 220, TEST.PD.PROT.ALL3.3: Match in Unconstrained Power Field. Packet155, 196, TEST.PD.PROT.ALL3.4: Match in Unconstrained Power Field. Packet170, 211, TEST.PD.PROT.ALL3.6: Match in Unconstrained Power Field. Packet151, TEST.PD.PROT.ALL3.7: Match in Unconstrained Power Field. Packet180, 221, TEST.PD.PROT.PORT3.1: Match in Unconstrained Power Field. Packet108, TEST.PD.PROT.PORT3.3: Match in Unconstrained Power Field. Packet461, 542, TEST.PD.PROT.PORT3.4: Match in Unconstrained Power Field. Packet166, 212, TEST.PD.PROT.PORT3.5: Match in Unconstrained Power Field. Packet156, 197, TEST.PD.PROT.PORT3.6: Match in Unconstrained Power Field. Packet137, 178, TEST.PD.PROT.SRC.1: Match in Unconstrained Power Field. Packet17, 40, 64, 87, TEST.PD.PROT.SRC.2: Match in Unconstrained Power Field. Packet17, 40, 49, 80, 103, 112, TEST.PD.PROT.SRC.3: Match in Unconstrained Power Field. Packet20, 57, TEST.PD.PROT.SRC.4: Match in Unconstrained Power Field. Packet20, 57,	PASS
		This report is generated by GRL-USB-PD Compliance Test Solution ( Version: 1.0.0)	Page: 95

SI No	Test ID	Test Name	Test Result
		Check Fixed PDO - COMMON.CHECK.PD.7#5	PASS
		Check PPS Validation - COMMON.CHECK.PD.7#6	PASS
		Check Power Rules - COMMON.CHECK.PD.7#7	PASS
		Check PDO Consistency - COMMON.CHECK.PD.7#8	PASS
		Check PDO Sequence - COMMON.CHECK.PD.7#9	PASS
		Check Fixed PDO Voltage - COMMON.CHECK.PD.7#10	PASS
		Check Variable PDO Voltage - COMMON.CHECK.PD.7#11	PASS
		Check Battery PDO Voltage - COMMON.CHECK.PD.7#12	PASS
		Check AVS Validation - COMMON.CHECK.PD.7#13	PASS
		Common_Check_PD_8_Request_Message - COMMON.CHECK.PD.8	PASS
		Request messages fields check - COMMON.CHECK.PD.8#1	PASS
		Common_Check_PD_9_Structured_VDM - COMMON.CHECK.PD.9	PASS

SI No	Test ID	Test Name	Test Result
		Structured VDM header field check - COMMON.CHECK.PD.9#1 >>TEST.PD.PHY.PORT.1: CommandVersion [b[12:11]] Obt:0 and Exp: 1. Packet198, TEST.PD.PROT.ALL.2: CommandVersion [b[12:11]] Obt:0 and Exp: 1. Packet340, TEST.PD.PROT.ALL.3: CommandVersion [b[12:11]] Obt:0 and Exp: 1. Packet375, TEST.PD.PROT.ALL.4: CommandVersion [b[12:11]] Obt:0 and Exp: 1. Packet360, TEST.PD.PROT.ALL3.2: CommandVersion [b[12:11]] Obt:0 and Exp: 1. Packet192, 233, TEST.PD.PROT.ALL3.3: CommandVersion [b[12:11]] Obt:0 and Exp: 1. Packet168, 209, TEST.PD.PROT.ALL3.4: CommandVersion [b[12:11]] Obt:0 and Exp: 1. Packet183, 224, TEST.PD.PROT.ALL3.6: CommandVersion [b[12:11]] Obt:0 and Exp: 1. Packet164, TEST.PD.PROT.ALL3.7: CommandVersion [b[12:11]] Obt:0 and Exp: 1. Packet193, 234, TEST.PD.PROT.PORT3.1: CommandVersion [b[12:11]] Obt:0 and Exp: 1. Packet121, TEST.PD.PROT.PORT3.3: CommandVersion [b[12:11]] Obt:0 and Exp: 1. Packet474, 555, TEST.PD.PROT.PORT3.4: CommandVersion [b[12:11]] Obt:0 and Exp: 1. Packet179, 225, TEST.PD.PROT.PORT3.5: CommandVersion [b[12:11]] Obt:0 and Exp: 1. Packet169, 210, TEST.PD.PROT.PORT3.6: CommandVersion [b[12:11]] Obt:0 and Exp: 1. Packet150, 191, TEST.PD.PROT.SRC.1: CommandVersion [b[12:11]] Obt:0 and Exp: 1. Packet77, TEST.PD.PROT.SRC.2: CommandVersion [b[12:11]] Obt:0 and Exp: 1. Packet93, TEST.PD.PROT.SRC.3: CommandVersion [b[12:11]] Obt:0 and Exp: 1. Packet70, TEST.PD.PROT.SRC.6: CommandVersion [b[12:11]] Obt:0 and Exp: 1. Packet86, TEST.PD.PROT.SRC.7: CommandVersion [b[12:11]] Obt:0 and Exp: 1. Packet76, TEST.PD.PROT.SRC.8:	PASS

SI No	Test ID	Test Name	Test Result
		Common_Check_PD_10_Extended_Message_Header - COMMON.CHECK.PD.10	PASS
		Check Extended Message Header - COMMON.CHECK.PD.10#1	PASS
		Common_Check_PD_11_Source_Capability_Extended_Message - COMMON.CHECK.PD.11	PASS
		Source capabilities extended message fields check - COMMON.CHECK.PD.11#1	PASS
		Common_Check_PD_12_Check_Sink_Capabilities - COMMON.CHECK.PD.12	PASS



SI No	Test ID	Test Name	Test Result
		<p>Sink capabilities fields check - COMMON.CHECK.PD.12#1            &gt;&gt;TEST.PD.PROT.ALL.1:            Match in number of Data object count: PD Message: 1 ,VIF: 3 and PPS PDO: 1.            Packet43, 45, 50, 52, 54, 56, 76,            TEST.PD.PROT.ALL.1:            Bit[27] Unconstrained_Power for PD2: Expected val: 0 , Obtained val:0            Bit[9:0] Operational_Current for PD2: Expected val: 1.3 , Obtained val:1.3            Bit[27] Unconstrained_Power : Expected val: 0 , Obtained val:0            Bit[9:0] Operational_Current : Expected val: 1.3 , Obtained val:1.3. Packet43, 45,            50, 52, 54, 56, 76,            TEST.PD.PROT.ALL.1:            Bit[9:0] Operational_Current for PD2: Expected val: 1.3 , Obtained val:1.3            Bit[9:0] Operational_Current : Expected val: 1.3 , Obtained val:1.3. Packet43, 45,            50, 52, 54, 56, 76,            TEST.PD.PROT.ALL.2:            Match in number of Data object count: PD Message: 1 and VIF: 1            Match in number of Data object count: PD Message: 1 ,VIF: 1 and PPS PDO: 1.            Packet155, 158, 159, 196, 199, 200, 263, 264, 265, 266, 282, 283, 284, 285,            350, 351, 352, 368, 369, 370,            TEST.PD.PROT.ALL.2:            Bit[27] Unconstrained_Power : Expected val: 0 , Obtained val:0            Bit[9:0] Operational_Current : Expected val: 1.3 , Obtained val:1.3            Bit[27] Unconstrained_Power for PD3: Expected val: 0 , Obtained val:0            Bit[9:0] Operational_Current for PD3: Expected val: 1.3 , Obtained val:1.3            Bit[27] Unconstrained_Power for PD2: Expected val: 0 , Obtained val:0            Bit[9:0] Operational_Current for PD2: Expected val: 1.3 , Obtained val:1.3.            Packet155, 158, 159, 196, 199, 200, 263, 264, 265, 266, 282, 283, 284, 285,            350, 351, 352, 368, 369, 370,            TEST.PD.PROT.ALL.2:            Bit[9:0] Operational_Current : Expected val: 1.3 , Obtained val:1.3            Bit[9:0] Operational_Current for PD3: Expected val: 1.3 , Obtained val:1.3            Bit[9:0] Operational_Current for PD2: Expected val: 1.3 , Obtained val:1.3.            Packet155, 158, 159, 196, 199, 200, 263, 264, 265, 266, 282, 283, 284, 285,            350, 351, 352, 368, 369, 370,            TEST.PD.PROT.ALL.3:</p>	PASS
		<p>This report is generated using GRL-USB-PD Compliance Test Solution ( Version: 1.0.0)            Date: 2025-02-14 : 11:41:15</p>	Page: 99

SI No	Test ID	Test Name	Test Result
		Common_Check_PD_13_Check_Correct_Use_of_Rp - COMMON.CHECK.PD.13 > AMS sequence TEST.PD.PROT.ALL.1: Message sequence AMS sequence AMS sequence AMS sequence AMS sequence AMS sequence AMS sequence TEST.PD.PROT.ALL3.8: Message sequence AMS sequence	PASS
		Rp Level Validation - COMMON.CHECK.PD.13#1	PASS
		Common_Check_PD_14_Check_Hard_Reset - COMMON.CHECK.PD.14	PASS
		Check Hard_Reset basic timing - COMMON.CHECK.PD.14#1	PASS
		Common_Check_PD_15_Check_Sink_Capabilities_Extended_Message - COMMON.CHECK.PD.15	PASS
		Sink capabilities extended message fields check - COMMON.CHECK.PD.15#1	PASS
		COMMON_CHECK_PD3_1_Check_EPR_Request_Message - COMMON.CHECK.PD3.1	PASS
		EPR_Request messages fields check - COMMON.CHECK.PD3.1#1	PASS
		COMMON_CHECK_PD3_2_Check_EPR_Mode_Message - COMMON.CHECK.PD3.2	PASS
		EPR_Mode messages fields check - COMMON.CHECK.PD3.2#1	PASS
		COMMON_CHECK_PD3_3_Check_EPR_Source_Capabilities_Message - COMMON.CHECK.PD3.3	PASS
		VIF field EPR_Supported_As_Src check - COMMON.CHECK.PD3.3#1	PASS
		First Fixed PDO consistency check - COMMON.CHECK.PD3.3#2	PASS
		Fixed PDO check - COMMON.CHECK.PD3.3#3	PASS
		Programmable Power Supply APDO check - COMMON.CHECK.PD3.3#4	PASS
		EPR PDOs power rules check - COMMON.CHECK.PD3.3#5	PASS
		EPR PDOs consistency check - COMMON.CHECK.PD3.3#6	PASS

SI No	Test ID	Test Name	Test Result
		SPR PDOs check - COMMON.CHECK.PD3.3#7	PASS
		Extended field check - COMMON.CHECK.PD3.3#8	PASS
		Data size extended header check - COMMON.CHECK.PD3.3#9	PASS
		SPR PDO check - COMMON.CHECK.PD3.3#10	PASS
		COMMON_CHECK_PD3_4_Check_EPR_Sink_Capabilities_Message - COMMON.CHECK.PD3.4	PASS
		EPR_Sink_Capabilities fields check - COMMON.CHECK.PD3.4#1	PASS
153	2.2	Common Procedures	PASS
		COMMON_PROC_PD_2_UUT_Sent_Get_Source_Cap - COMMON.PROC.PD.2	PASS
		Validate Get source capabilities message initiated by DUT - COMMON.PROC.PD.2#1	PASS
		DUT's Request message validation - COMMON.PROC.PD.2#2	PASS
		COMMON_PROC_PD_3_UUT_Sent_Get_Sink_Cap - COMMON.PROC.PD.3	PASS
		Validate Get sink cap message initiated by DUT - COMMON.PROC.PD.3#1	PASS
		COMMON_PROC_PD_4_UUT_Sent_Ping - COMMON.PROC.PD.4	PASS
		Ping message initiated by DUT - COMMON.PROC.PD.4#1	PASS
		COMMON_PROC_PD_5_UUT_Sent_PR_Swap - COMMON.PROC.PD.5	PASS
		PR_Swap valid condition check - COMMON.PROC.PD.5#1	PASS
		PR_Swap init and VIF field value comparison - COMMON.PROC.PD.5#2	PASS
		PR_Swap init and VIF field value comparison - COMMON.PROC.PD.5#3	PASS
		COMMON_PROC_PD_6_UUT_Sent_VCONN_Swap - COMMON.PROC.PD.6	PASS
		Vconn_Swap valid condition check - Tester Vconn Source - COMMON.PROC.PD.6#1	PASS
		Vconn_Swap init and VIF field value comparison - COMMON.PROC.PD.6#2	PASS
		tVCONNSourceOn Timer Validation - COMMON.PROC.PD.6#3	PASS
		Vconn_Swap valid condition check - DUT Vconn Source - COMMON.PROC.PD.6#4	PASS
		COMMON_PROC_PD_7_UUT_Sent_Discover_Identity_Request - COMMON.PROC.PD.7	PASS
		Validate Discover ID request message initiated by DUT - COMMON.PROC.PD.7#1	PASS

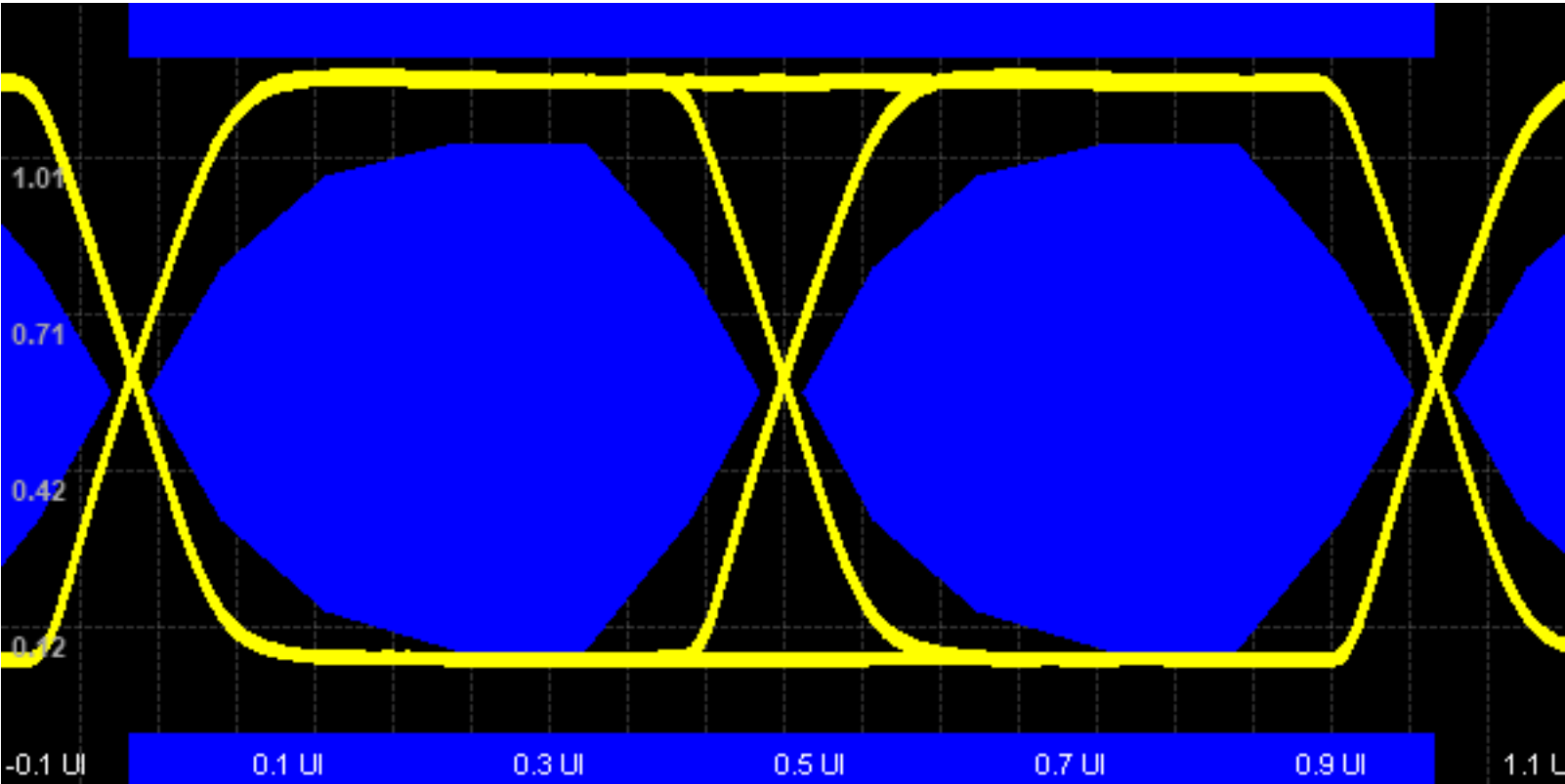
SI No	Test ID	Test Name	Test Result
		Structured VDM Message Header check - COMMON.PROC.PD.7#2	PASS
		Tester's VDM response check - COMMON.PROC.PD.7#3	PASS
		COMMON_PROC_PD_8_UUT_Sent_Discover_SVIDs_Request - COMMON.PROC.PD.8	PASS
		Validate Discover ID request message initiated by DUT - COMMON.PROC.PD.8#1	PASS
		Structured VDM Message Header check - COMMON.PROC.PD.8#2	PASS
		Tester's VDM response check - COMMON.PROC.PD.8#3	PASS
		COMMON_PROC_PD_9_UUT_Sent_Attention - COMMON.PROC.PD.9	PASS
		Validate attention request message initiated by DUT - COMMON.PROC.PD.9#1	PASS
		Structured VDM message header check - COMMON.PROC.PD.9#2	PASS
		COMMON_PROC_PD_10_UUT_Sent_Request - COMMON.PROC.PD.10	PASS
		Validate request message initiated by DUT - COMMON.PROC.PD.10#1 >TEST.PD.PHY.ALL.3: PS_Packet54, TEST.PD.PROT.ALL.2: PS_Packet91, TEST.PD.PROT.ALL3.7: PS_Packet113,	PASS
		COMMON_PROC_PD_11_UUT_Sent_Source_Capabilities - COMMON.PROC.PD.11	PASS
		Validate Source capabilities message initiated by DUT - COMMON.PROC.PD.11#1	PASS
		DUT should respond with Accept - COMMON.PROC.PD.11#2	PASS
		DUT should send PS_RDY - COMMON.PROC.PD.11#3	PASS
		Wait Message - COMMON.PROC.PD.11#4	PASS
		COMMON_PROC_PD_12_UUT_Sent_DR_Swap - COMMON.PROC.PD.12	PASS
		Validate DR_Swap message initiated by DUT - COMMON.PROC.PD.12#1	PASS
		COMMON_PROC_PD_17_Tester_Sent_Vconn_swap_message - COMMON.PROC.PD.17	PASS
		VCONN present check - COMMON.PROC.PD.17#1	PASS
		PS_RDY is missing - COMMON.PROC.PD.17#2	PASS
		VCONN present check - COMMON.PROC.PD.17#3	PASS
		tVONNSourceOff timer check - COMMON.PROC.PD.17#4	PASS

SI No	Test ID	Test Name	Test Result
		COMMON_PROC_PD3_1 Sink_Start_an_AMS - COMMON.PROC.PD3.1	PASS
		Sink Start AMS - COMMON.PROC.PD3.1#1	PASS
		COMMON_PROC_PD3_2_UUT_Sent_EPR_Source_Cap_message - COMMON.PROC.PD3.2	PASS
		Validate EPR_Source_Capabilities message initiated by UUT - COMMON.PROC.PD3.2#1	PASS
		UUT should respond with Accept - COMMON.PROC.PD3.2#2	PASS
		UUT should send PS_RDY - COMMON.PROC.PD3.2#3	PASS
		COMMON_PROC_PD3_3_UUT_Sent_EPR_Get_Source_Cap - COMMON.PROC.PD3.3	PASS
		Validate EPR Get Source Capabilities message initiated by DUT - COMMON.PROC.PD3.3#1	PASS
		DUT's EPR Request message validation - COMMON.PROC.PD3.3#2	PASS
		Requested Voltage and PDP - COMMON.PROC.PD3.3#3	PASS
		COMMON_PROC_PD3_4_UUT_Sent_EPR_Request - COMMON.PROC.PD3.4	PASS
		Validate EPR Request message initiated by DUT - COMMON.PROC.PD3.4#1	PASS
		COMMON_PROC_PD3_5_Tester_Sent_EPR_Mode_Enter - COMMON.PROC.PD3.5	PASS
		Validate EPR Enter Enter initiated by DUT - COMMON.PROC.PD3.5#1	PASS
		VIF Field Has_Invariant_PDOs check - COMMON.PROC.PD3.5#2	PASS
		UUT Request message check - COMMON.PROC.PD3.5#3	PASS
		UUT sends a wait message - COMMON.PROC.PD3.5#4	PASS
		UUT sends PSRdy Message - COMMON.PROC.PD3.5#5	PASS
		VIF specified Source Capabilities - COMMON.PROC.PD3.5#6	PASS
		Source Cap message - COMMON.PROC.PD3.5#7	PASS
		UUT EPR_Mode Enter_ - COMMON.PROC.PD3.5#8	PASS
		UUT Not_Supported Message - COMMON.PROC.PD3.5#9	PASS
		UUT EPR_Mode Enter_Acknowledged - COMMON.PROC.PD3.5#10	PASS
		UUT VCONN_Swap Message - COMMON.PROC.PD3.5#11	PASS
		UUT EPR_Source_Capabilities Message - COMMON.PROC.PD3.5#12	PASS
		UUT EPR Contract - COMMON.PROC.PD3.5#13	PASS

SI No	Test ID	Test Name	Test Result
		COMMON_PROC_PD3_6_UUT_Sent_EPR_Mode_Enter - COMMON.PROC.PD3.6	PASS
		Validate EPR_Mode_Enter initiated by DUT - COMMON.PROC.PD3.6#1	PASS
		Validate EPR_Mode_Enter response - COMMON.PROC.PD3.6#2	PASS
		Tester sends a Vconn_Swap message - COMMON.PROC.PD3.6#3	PASS
		Validate EPR_Mode_Enter failed message - COMMON.PROC.PD3.6#4	PASS
		Validate SOP' Discover_Id and EPR_Mode_Enter Succeeded message - COMMON.PROC.PD3.6#5	PASS
		EPR_Source_Cap message - COMMON.PROC.PD3.6#6	PASS
		UUT establishes EPR contract - COMMON.PROC.PD3.6#7	PASS
		COMMON_PROC_PD3_7_Tester_Sends_EPR_KeepAlive_Message - COMMON.PROC.PD3.7	PASS
		Validate EPR_KeepAlive response message initiated by DUT - COMMON.PROC.PD3.7#1	PASS



BMC Eye Diagram



Functional Tests Result Summary:

SI No	Test ID	Test Name	Result	Details
1	TD.4.11.2	TD.4.11.2 Sink Dead Battery Test	PASS	
2	TD.4.1.1	TD.4.1.1 Initial Voltage Test	PASS	

SI No	Test ID	Test Name	Result	Details
3	TD.4.2.1	TD.4.2.1 Source Connect Sink Test	NA	Type_C_State_Machine Expected state: SRC. Obtained state: DRP
4	TD.4.2.2	TD.4.2.2 Source Connect SNKAS Test	NA	Type_C_State_Machine is not Source
5	TD.4.2.3	TD.4.2.3 Source Connect DRP	NA	Type_C_State_Machine is not Source
6	TD.4.2.4	TD.4.2.4 Source Connect Try SRC DRP	NA	Type_C_State_Machine is not Source
7	TD.4.2.5	TD.4.2.5 Source Connect Try SNK DRP	NA	Type_C_State_Machine is not Source
8	TD.4.2.6	TD.4.2.6 Source Connect Audio Accessory	NA	Type_C_State_Machine is not Source
9	TD.4.2.7	TD.4.2.7 Source Connect Debug Accessory	NA	Type_C_State_Machine is not Source
10	TD.4.2.8	TD.4.2.8 Source Connect Vconn Accessory	NA	Type_C_State_Machine is not Source TYPE_C_SOURCES_VCONN is not set to YES
11	TD.4.3.1	TD.4.3.1 Sink Connect Source Test	NA	Type_C_State_Machine is not set to sink
12	TD.4.3.2	TD.4.3.2 Sink Connect DRP Test	NA	Type_C_State_Machine is not set to sink
13	TD.4.3.3	TD.4.3.3 Sink Connect Try SRC DRP Test	NA	Type_C_State_Machine is not set to sink
14	TD.4.3.4	TD.4.3.4 Sink Connect Try SNK DRP Test	NA	Type_C_State_Machine is not set to sink
15	TD.4.3.5	TD.4.3.5 Sink.Connect.SNKAS.Test	NA	Type_C_State_Machine is not set to sink
16	TD.4.3.6	TD.4.3.6 Sink.Connect.Accessories.Test	NA	Type_C_State_Machine is not set to SNK
17	TD.4.4.1	TD.4.4.1 SNKAS Connect Source Test	NA	Type_C_State machine is not set to SNK TYPE_C_SUPPORTS_AUDIO_ACCESSORY is not set to YES TYPE_C_SUPPORTS_VCONN_POWERED_ACCESSORY is not set to YES
18	TD.4.4.2	TD.4.4.2 SNKAS Connect DRP Test	NA	Type_C_State machine is not set to SNK TYPE_C_SUPPORTS_AUDIO_ACCESSORY is not set to YES TYPE_C_SUPPORTS_VCONN_POWERED_ACCESSORY is not set to YES
19	TD.4.4.3	TD.4.4.3 SNKAS Connect Try SRC DRP Test	NA	Type_C_State machine is not set to SNK TYPE_C_SUPPORTS_AUDIO_ACCESSORY is not set to YES TYPE_C_SUPPORTS_VCONN_POWERED_ACCESSORY is not set to YES

SI No	Test ID	Test Name	Result	Details
20	TD.4.4.4	TD.4.4.4 SNKAS Connect Try SNK DRP Test	NA	Type_C_State machine is not set to SNK TYPE_C_SUPPORTS_AUDIO_ACCESSORY is not set to YES TYPE_C_SUPPORTS_VCONN_POWERED_ACCESSORY is not set to YES
21	TD.4.4.5	TD.4.4.5 SNKAS Connect SNKAS Test	NA	Type_C_State machine is not set to SNK TYPE_C_SUPPORTS_AUDIO_ACCESSORY is not set to YES TYPE_C_SUPPORTS_VCONN_POWERED_ACCESSORY is not set to YES
22	TD.4.4.6	TD.4.4.6 SNKAS Connect Audio Acc	NA	Type_C_State machine is not set to SNK TYPE_C_SUPPORTS_AUDIO_ACCESSORY is not set to YES TYPE_C_SUPPORTS_VCONN_POWERED_ACCESSORY is not set to YES
23	TD.4.4.7	TD.4.4.7 SNKAS Connect Debug Accessory	NA	Type_C_State machine is not set to SNK TYPE_C_SUPPORTS_AUDIO_ACCESSORY is not set to YES TYPE_C_SUPPORTS_VCONN_POWERED_ACCESSORY is not set to YES
24	TD.4.4.8	TD.4.4.8 SNKAS Connect PoweredAcc	NA	Type_C_State machine is not set to SNK TYPE_C_SUPPORTS_AUDIO_ACCESSORY is not set to YES TYPE_C_SUPPORTS_VCONN_POWERED_ACCESSORY is not set to YES
25	TD.4.5.1	TD.4.5.1 DRP Connect Sink Test	NA	TYPE_C_IMPLEMENTS_TRY_SNK is not set to NO
26	TD.4.5.2	TD.4.5.2 DRP Connect SNKAS Test	NA	TYPE_C_IMPLEMENTS_TRY_SNK is not set to NO
27	TD.4.5.3	TD.4.5.3 DRP Connect Source Test	NA	TYPE_C_IMPLEMENTS_TRY_SNK is not set to NO
28	TD.4.5.4	TD.4.5.4 DRP Connect DRP Test	NA	TYPE_C_IMPLEMENTS_TRY_SNK is not set to NO
29	TD.4.5.5	TD.4.5.5 DRP Connect Try SRC DRP Test	NA	TYPE_C_IMPLEMENTS_TRY_SNK is not set to NO
30	TD.4.5.6	TD.4.5.6 DRP Connect Try SNK DRP Test	NA	TYPE_C_IMPLEMENTS_TRY_SNK is not set to NO
31	TD.4.6.1	TD.4.6.1 Try SRC DRP Connect Source Test	NA	TYPE_C_IMPLEMENTS_TRY_SRC is not set to YES

SI No	Test ID	Test Name	Result	Details
32	TD.4.6.2	TD.4.6.2 Try SRC DRP Connect DRP Test	NA	TYPE_C_IMPLEMENTS_TRY_SNK is not set to YES
33	TD.4.6.3	TD.4.6.3 Try SRC DRP Connect Try SRC DRP Test	NA	TYPE_C_IMPLEMENTS_TRY_SRC is not set to YES
34	TD.4.6.4	TD.4.6.4 Try SRC DRP Connect Try SNK DRP Test	NA	TYPE_C_IMPLEMENTS_TRY_SRC is not set to YES
35	TD.4.6.5	TD.4.6.5 Try SRC DRP Connect Sink Test	NA	TYPE_C_IMPLEMENTS_TRY_SRC is not set to YES
36	TD.4.6.6	TD.4.6.6 Try SRC DRP Connect SNKAS Test	NA	TYPE_C_IMPLEMENTS_TRY_SRC is not set to YES
37	TD.4.7.1	TD.4.7.1 Try SNK DRP Connect Source Test	NA	
38	TD.4.7.2	TD.4.7.2 Try SNK DRP Connect DRP Test	NA	
39	TD.4.7.3	TD.4.7.3 Try SNK DRP Connect Try SRC DRP Test	NA	
40	TD.4.7.4	TD.4.7.4 Try SNK DRP Connect Try SNK DRP Test	PASS	
41	TD.4.7.5	TD.4.7.5 Try SNK DRP Connect Sink Test	PASS	
42	TD.4.7.6	TD.4.7.6 Try SNK DRP Connect SNKAS Test	PASS	
43	TD.4.8.1	TD.4.8.1 DRP Connect Audio Acc Test	PASS	
44	TD.4.8.2	TD.4.8.2 DRP Connect Debug Acc Test	PASS	
45	TD.4.8.3	TD.4.8.3 DRP Connect Vconn Accessory Test	PASS	
46	TD.4.9.1	TD.4.9.1 Source Suspend Test	NA	DUT is not PUT_V
47	TD.4.9.2	TD.4.9.2 USB Type C Current Advertisement Test	PASS	
48	TD.4.9.3	TD.4.9.3 Source PR Swap Test	PASS	
49	TD.4.9.4	TD.4.9.4 Source Vconn Swap Test	NA	PUT is not PUT_V VIF field VCONN_SWAP_TO_OFF_SUPPORTED is not set to YES
50	TD.4.9.5	TD.4.9.5 Source Alternate Mode Test	NA	VIF field TYPE_C_IS_ALT_MODE_CONTROLLER is not set to YES
51	TD.4.10.1	TD.4.10.1 Sink Power Sub States Test	PASS	
52	TD.4.10.2	TD.4.10.2 Sink Power Precedence Test	PASS	

SI No	Test ID	Test Name	Result	Details
53	TD.4.10.3	TD.4.10.3 Sink Suspend Test	NA	
54	TD.4.10.4	TD.4.10.4 Sink PR Swap Test	NA	
55	TD.4.10.5	TD.4.10.5 Sink.VCONN Swap Test	NA	VCONN_SWAP_TO_ON_SUPPORTED is not set to YES
56	TD.4.10.6	TD.4.10.6 Sink Alternate Mode Test	NA	TYPE_C_IS_ALT_MODE_ADAPTER is not set to YES
57	TD.4.11.1	TD.4.11.1 DR Swap Test	NA	
58	TD.4.12.2	TD.4.12.2 Hub Port Types Test	NA	VIF field TYPE_C_PORT_ON_HUB is not set to YES
59	TD.4.1.2	TD.4.1.2 Unpowered CC Voltage Test	NA	PORT_BATTERY_POWERED is set to YES
60	TD.4.13.5	TD.4.13.5 Cable EnterUSB and Data Reset Test	NA	USB4_Supported is not set to YES Product_Type is not set to Cable

## Attachment 2

## Photo Documentation

Report No.: TCT250208S001

Product:

Smartphone

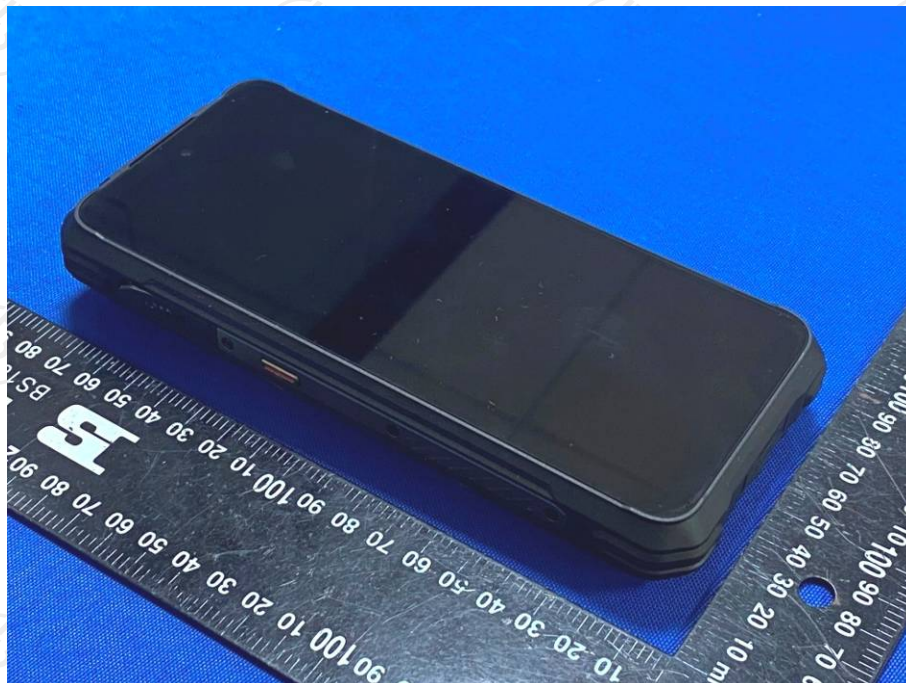
Type Designation:

KINGKONG POWER 5

Photo 1- Front view



Photo 2- Front view





## Attachment 2

## Photo Documentation

Report No.: TCT250208S001

Product:

Smartphone

Type Designation:

KINGKONG POWER 5

Photo 3- Back view



Photo 4- Input terminal view



## Attachment 2

## Photo Documentation

Report No.: TCT250208S001

Product:

Smartphone

Type Designation:

KINGKONG POWER 5

Photo 5- Test view



---End of Attachment ---