


<p align="center">TEST REPORT EN IEC 62680-1-2 Universal serial bus interfaces for data and power Part 1-2: Common components USB Power Delivery specification EN IEC 62680-1-3 Universal serial bus interfaces for data and power Part 1-3: Common components — USB Type-C(r) cable and connector specification(CI.4)</p>	
Report Number.....	TCT250324S002
Date of issue.....	2025-06-24
Total number of pages	90 pages (not included attachments)
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And Address.....	TCT testing Industrial Park, Fuqiao 5th Industrial Zone, Fuhai Street, Bao'an District, Shenzhen
Applicant's name	Shenzhen Huafurui Technology Co., Ltd.
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Test specification:	
Standard	EN IEC 62680-1-2:2022 EN IEC 62680-1-3:2022
Test procedure	Type-test
Non-standard test method	N/A
Test Report Form No.	62680_1_2B.1 62680_1_3B.1
Test Report Form(s) Originator	TCT
Master TRF	Dated 2025-03-27
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Test item description :	Smartphone	
Trade Mark :	CUBOT	
Manufacturer	Same as applicant	
Model/Type reference	X100	
Model difference :	N/A	
Rating	DC5.0V, 3A; DC9.0V,3A; DC12.0V,2.75A	
Testing Laboratory:	Shenzhen TCT Testing Technology Co., Ltd.	
Testing location/ address	TCT testing Industrial Park, Fuqiao 5th Industrial Zone, Fuhai Street, Bao'an District, Shenzhen	
Tested by (name, function + signature) :	Kevin Li	
Approved by (name, function + signature) :	Ringko.Shi	
<input type="checkbox"/> Testing procedure: CTF Stage 1		
Testing location/ address		
Tested by (name, function + signature) :		
Approved by (name, function + signature) :		
<input type="checkbox"/> Testing procedure: CTF Stage 2		
Testing location/ address		
Tested by (name, function + signature) :		
Witnessed by (name, function + signature):		
Approved by (name, function + signature) :		
<input type="checkbox"/> Testing procedure: CTF Stage 3:		
<input type="checkbox"/> Testing procedure: CTF Stage 4:		
Testing location/ address		
Tested by (name, function + signature) :		
Witnessed by (name, function + signature):		
Approved by (name, function + signature) :		
Supervised by (name, function + signature):		

List of Attachments (including a total number of pages in each attachment):

Attachment NO.1: GRL-USB-PD Compliance Test Solution, 149 pages.

Attachment NO.2: Photo documentation, 2 pages.

Summary of testing:

All applicable test completed and meet requirements.

Tests performed (name of test and test clause):

See report

Testing location:

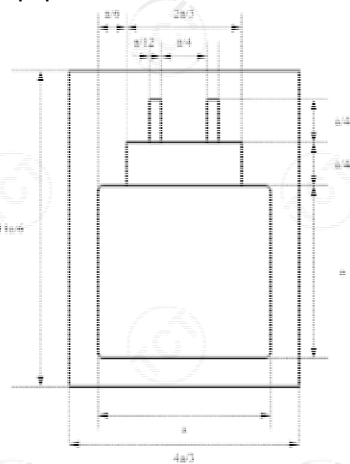
See above for details.

Copy of marking plate:

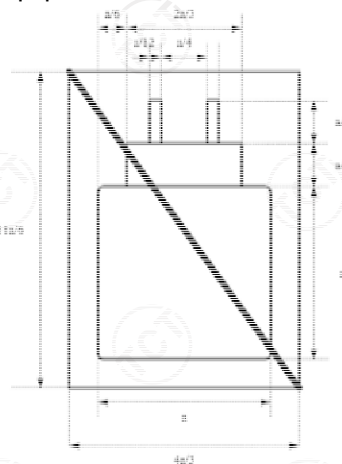
The artwork below may be only a draft. The use of certification marks on a product must be authorized by the respective NCBs that own these marks.

Marking and labelling information on package and user manual: 1a or 1b, and 2. (Requirements according to 2022/2380/EU if applicable, see corresponding legislation for details.)

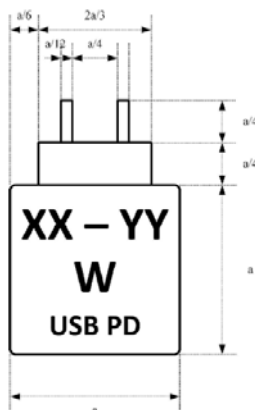
1a) A charging device is included with the radio equipment:



1b) No charging device is included with the radio equipment:



2) Content and format of the label:



Note:

1: The dimension "a" shall be greater than or equal to 7 mm;

2: "XX" the minimum power required by the radio equipment to charge;

"YY" the maximum power required by the radio equipment to achieve maximum charging speed;

"USB PD" (USB Power Delivery) : if the radio equipment supports that charging communication protocol;

Test item particulars.....:	
Classification of installation and use.....: --	
Supply Connection.....: Type C -port	
Possible test case verdicts:	
- test case does not apply to the test object.....: N/A	
- test object does meet the requirement.....: P (Pass)	
- test object does not meet the requirement.....: F (Fail)	
Testing.....:	
Date of receipt of test item	2025-03-24
Date (s) of performance of tests	2025-06-05 to 2025-06-05
General remarks:	
<p>"(See Enclosure #)" refers to additional information appended to the report.</p> <p>"(See appended table)" refers to a table appended to the report.</p> <p>Note: All reference Table and Figure are shown in the original standard</p> <p>Throughout this report a <input type="checkbox"/> comma / <input checked="" type="checkbox"/> point is used as the decimal separator.</p>	
When differences exist; they shall be identified in the General product information section.	
Name and address of factory (ies).....: same as manufacturer	

General product information:

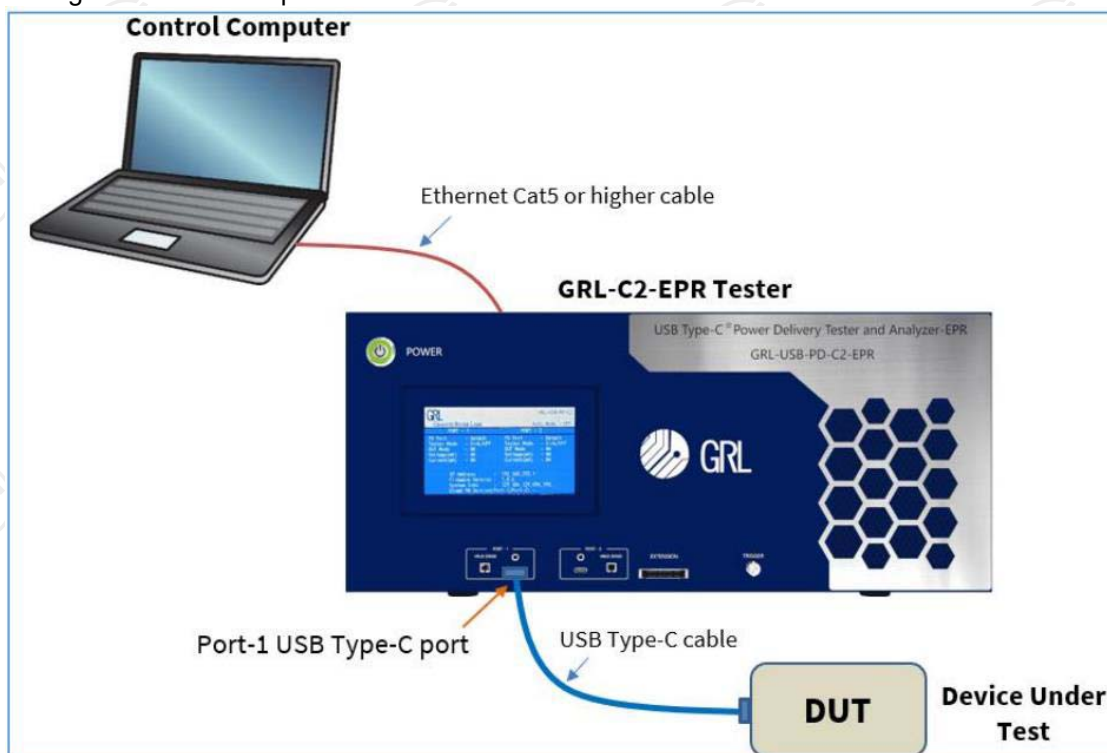
Standard and result:

Standard	Clause	Test description	Evaluation result
EN IEC 62680-1-3:2022	4	USB Type-C Functional Test	PASS
EN IEC 62680-1-2:2022	All applicable testes	--	PASS

2.Measuring Equipment and Software Used

Equipment	Manufacturer	Model No.	Serial No.	Last Cal.	Due Date
USB Type-C Power Delivery Tester-EPR	Granite River Labs Technology Pvt. Ltd., India	GRL-USB-PD-C2-EPR	--	2024-10-18	2025-10-17
Test Software for RE	Granite River Labs Technology Pvt. Ltd., India	GRL-C2-Browser App	1.6.30.0	--	--

3.Block Diagram of Test Setup



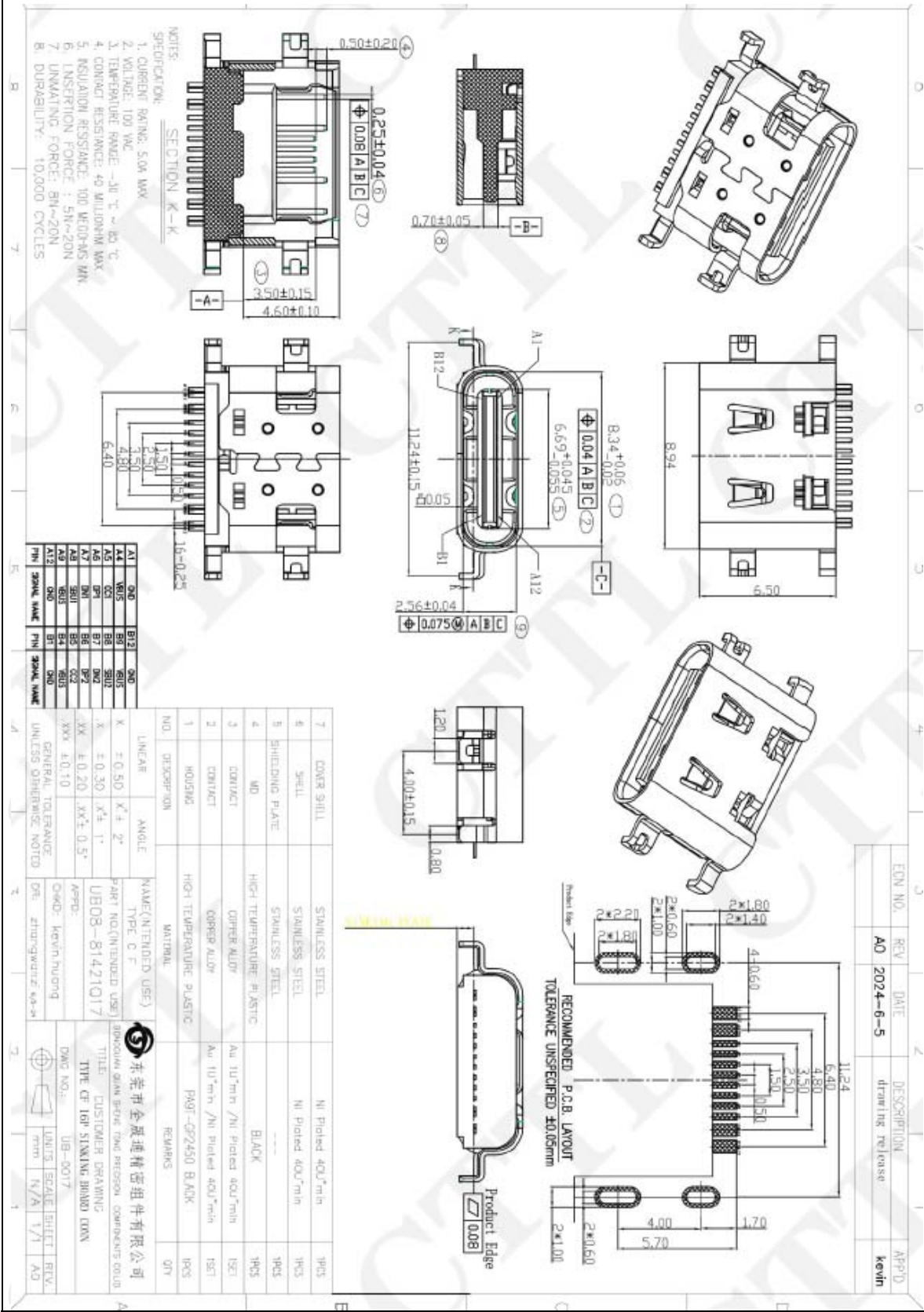
4.The Type-C Connector(receptacle) Information

Product Name:	TYPE CF 16P SINKING BOARD CONN
Model Name:	UB08-81421Q17
Report Number:	24B01N001273-001-COM
Manufacturer:	DONGGUAN QUANSHENG TONG PRECISION COMPONENTS CO.,LTD.
Standard:	EN IEC 62680-1-3:2022

5. Test Environment

Temperature:	22.4°C
Humidity:	51%

6.Type-C Connector Drawing (See below).



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Clause	Requirement + Test	Result - Remark	Verdict
4	Functional		P
	This chapter covers the functional requirements for the signaling across the USB Type-C® cables and connectors. This includes functional signal definition, discovery and configuration processes, and power delivery.		N/A
4.1	Signal Summary		N/A
4.2	Signal Pin Descriptions		N/A
4.2.1	SuperSpeed USB Pins		N/A
4.2.2	USB 2.0 Pins		N/A
4.2.3	Auxiliary Signal Pins		N/A
4.2.4	Power and Ground Pins		N/A
4.2.5	Configuration Pins		N/A
4.3	Sideband Use (SBU)		P
	The Sideband Use pins (SBU1 and SBU2) are limited to the uses as defined by this specification and additional functionality defined in the USB4 Specification. See Appendix E and Appendix A for use of the SBU pins in Alternate Modes and Audio Adapter Accessory Mode.		N/A
	The SBU pins on a port shall either be open circuit or have a weak pull-down to ground no stronger than zSBU Termination when in USB 3.2 or USB 2.0.		P
	These pins are pre-wired in the standard USB Full-Featured Type-C cable as individual single-ended wires (SBU_A and SBU_B). Note that SBU1 and SBU2 are cross-connected in the cable.		N/A
	When operating in USB4, these pins are used as the USB4 Sideband Channel with SBU1 mapping to SBTX and SBU2 mapping to SBRX. SBTX and SBRX functional requirements are as defined in the USB4 Specification. When a port determines that the locally-inserted plug is flipped (i.e. CC1 is open, CC2 is terminated), the USB4 Specification (reference Sideband Channel Lane Reversal) dictates that the port flip the SBTX and SBRX mappings to SBU1 and SBU2 in order to assure proper sideband transmit-to-receive end-to-end operation.		N/A
4.4	Power and Ground		P
4.4.1	IR Drop		N/A
	The maximum allowable cable IR drop for ground (including ground on a captive cable) shall be 250 mV and for VBUS shall be 500 mV through the cable to the cable's maximum rated VBUS current capacity. When VCONN is being		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	sourced, the IR drop for the ground shall still be met considering any additional VCONN return current.		
4.4.2	VBUS		P
	The allowable default range for VBUS as measured at the Source receptacle shall be as defined by the USB 2.0 Specification and USB 3.2 Specification. For USB4, the USB 3.2 Specification is used for this requirement. NOTE that due to higher currents allowed, legacy devices may experience a higher voltage (up to 5.5V maximum) at light loads.		N/A
	The Source's USB Type-C receptacle VBUS pin shall remain unpowered and shall limit the capacitance between VBUS and GND as specified in Table 4-2 until a Sink is attached. The VBUS pin shall return to the unpowered state when the Sink is detached. See Table 4-29 for VBUS timing values. Legacy hosts/chargers that by default source VBUS when connected using any legacy USB connector (Standard-A, Micro-B, etc.) to USB Type-C cable or adapter are exempted from these two requirements.		P
	A DRP or Source (or device with Accessory Support) implementing an Rp pull-up as its method of connection detection shall provide an impedance between VBUS and GND on its receptacle pins as specified in Table 4-2 when not sourcing power on VBUS (i.e., when in states Unattached. SRC or Unattached. Accessory).		P
4.4.3	VCONN		N/A
	VCONN is provided by the Source to power cables with electronics in the plug. VCONN is provided over the CC pin that is determined not to be connected to the CC wire of the cable.		N/A
	Initially, VCONN shall be sourced on all Source USB Type-C receptacles that utilize the TX and RX pins during specific connection states as described in Section 4.5.2.2. Subsequently, if VCONN is not explicitly required by the cable or device as indicated in its eMarker, VCONN may be removed as described in Table 4-4. VCONN may also be sourced by USB Type-C receptacles that do not utilize the TX and RX pins as described in Section 4.5.2.2. USB PD VCONN_Swap command also provides the Source a means to request that the attached Sink source VCONN.		N/A
	To aid in reducing the power associated with supplying VCONN, a Source is allowed to either not source VCONN or turn off VCONN under any of the following conditions:		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	Ra is not detected on the CC pin after tCCDebounce when the other CC pin is in the SRC.Rd state, or		N/A
	if there is no GoodCRC response to USB PD Discover Identity messages sent to SOP'.		N/A
	If the power source used to supply VCONN power is a shared power source for other USB VCONN and VBUS outputs, it must be bypassed with capacitance identical to the VBUS capacitance requirements of USB 3.2 Section 11.4.4 – Dynamic Attach and Detach. Any VCONN power source bypass capacitance must be isolated from the CC pins when VCONN is not being provided.		N/A
	The cable shall remove or weaken Ra according to the state diagram behavior in 4.5.2.5. The cable shall reapply Ra according to the state diagram behavior in 4.5.2.5. The cable shall discharge VCONN to below vVCONNDischarge on a cable disconnect. The cable shall control Ra at each of its ends independently based on the VCONN on that end.		N/A
	Implementation Note: Increasing Ra to 20KΩ will meet both the power dissipation for electronically marked passive cables and discharge 10μF to less than vVCONNDischarge in tvVCONNDischarge.		N/A
	The VPA shall remove or weaken Ra within tRaWeaken (as defined in Table 4-7) after VCONN enters the valid voltage range (vVCONNValid).		N/A
	The VPA shall reapply Ra when VCONN falls below vRaReconnect as defined in Table 4-7. The VPA shall discharge VCONN to below vVCONNDischarge within tvVCONNDischarge on a cable disconnect. The VPA shall consider the VCONN capacitance present in the accessory when discharging VCONN.		N/A
	The maximum power consumption while in an Alternate Mode is defined by the specification specific to the Alternate Mode being used.		N/A
	The VPD shall remove or weaken Ra within tRaWeaken (as defined in Table 4-8) after VCONN enters the valid voltage range (vVCONNValid).		N/A
	The VPD shall reapply Ra when VCONN falls below vRaReconnect as defined in Table 4-8. The VPD shall discharge VCONN to below vVCONNDischarge within tvVCONNDischarge on a cable disconnect. The VPD shall consider the VCONN capacitance present in the device when discharging VCONN.		N/A
4.5	Configuration Channel (CC)		P
4.5.1	Architectural Overview		P

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Clause	Requirement + Test	Result - Remark	Verdict
	For the USB Type-C solution, two pins on the connector, CC1 and CC2, are used to establish and manage the Source-to-Sink connection. When the device is connected through a hub, the connection between a Sink (UFP) on the hub and the Source (host port) and the connection between the Sink (device port) and a Source (DFP on the hub), are treated as separate connections. Functionally, the configuration channel is used to serve the following purposes.		N/A
	Detect attach of USB ports, e.g. a Source to a Sink		N/A
	Resolve cable orientation and twist connections to establish USB data bus routing		N/A
	Establish data roles between two attached ports		N/A
	Discover and configure VBUS: USB Type-C Current modes or USB Power Delivery		N/A
	Configure VCONN		N/A
	Discover and configure optional Alternate and Accessory modes		N/A
4.5.1.1	USB Data Bus Interface and USB Type-C Plug Flip-ability		N/A
	Since the USB Type-C plug can be inserted in either right-side-up or upside-down position, the hosts and devices that support USB data bus functionality must operate on the signal pins that are actually connected end-to-end. In the case of USB 2.0, this is done by shorting together the two D+ signal pins and the two D- signal pins in the host and device receptacles. In the case of USB 3.2 SuperSpeed USB or USB4 TX/RX signals in a single-lane implementation, it requires the functional equivalent of a switch in both the host and device to appropriately route the TX and RX signal pairs to the connected path through the cable. For a USB 3.2 SuperSpeed USB or USB4 dual-lane implementation, the host and/or device resolves the lane ordering.		N/A
	To establish the proper routing of the active USB data bus from host to device, the standard USB Type-C cable is wired such that a single CC wire is position aligned with the first TX/RX signal pairs (TXp1/TXn1 and RXp1/RXn1) – in this way, the CC wire and TX/RX data bus wires that are used for single-lane operational signaling within the cable track with regard to the orientation and twist of the cable. By being able to detect which of the CC pins (CC1 or CC2) at the receptacle is terminated by the device, the host is able to determine which		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	TX/RX signals are to be used for the single-lane connection and the host can use this to control the functional switch for routing the TX/RX signal pairs. Similarly in the device, detecting which of the CC pins at the receptacle is terminated by the host allows the device to control the functional switch that routes its TX/RX signal pairs.		
	For a dual-lane implementation, the TX/RX signal pairs in the cable/plug aligned with the CC wire/pin is Lane 0 and in reference to USB 3.2, shall be identified as the Configuration Lane. The second TX/RX signal pairs (TXp2/TXn2 and RXp2/RXn2) in the cable/plug is Lane 1 of a dual-lane configuration.		N/A
	The functional requirements for implementing TX/RX data bus routing for the USB Type-C receptacle are not included in the scope of this specification. There are multiple host, device and hub architectures that can be used to accomplish this which could include either discrete or integrated switching, and could include merging this functionality with other USB 3.2 or USB4 design elements, e.g. a bus repeater.		N/A
	The functional requirements for addressing SBU1 and SBU2 routing is not included in the scope of this specification. For USB4, where SBTX and SBRX are mapped to SBU1 and SBU2, the adjustment to the mapping of these signals based on the connection state (flipped and/or twisted) of the cable is defined by the USB4 Specification (reference Sideband Channel Lane Reversal).		N/A
4.5.1.2	Connecting Sources and Sinks		P
	Given that the USB Type-C receptacle and plug no longer differentiate host and device roles based on connector shape, e.g., as was the case with USB Type-A and Type-B connectors, any two ports that have USB Type-C receptacles can be connected together with a standard USB Type-C cable. Table 4-9 summarizes the expected results when interconnecting Source, Sink and DRP ports.		N/A
	In the cases where no function results, neither port shall be harmed by this connection. The user has to independently realize the invalid combination and take appropriate action to resolve. While these two invalid combinations mimic traditional USB where host-to-host and device-to-device connections are not intended to work, the non-keyed USB Type-C solution does not prevent the user from attempting such interconnects. VBUS and VCONN shall not be applied by a Source (host) in these cases.		P

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Clause	Requirement + Test	Result - Remark	Verdict
	The typical flow for the configuration of the interface in the general USB case of a Source (Host) to a Sink (Device) is as follows:		N/A
	1. Detect a valid connection between the ports (including determining cable orientation, Source/Sink and DFP/UFP relationship)		N/A
	2. Optionally discover the cable's capabilities		N/A
	3. Optionally establish alternatives to traditional USB power (See Section 4.6.2)		N/A
	a. USB PD communication over CC for advanced power delivery negotiation		N/A
	b. USB Type-C Current modes		N/A
	c. USB BC 1.2		N/A
	4. USB Device Enumeration		N/A
	For cases of Dual-Role-Power (DRP) ports connecting to either Source-only, Sink-only or another DRP, the process is essentially the same except that during the detecting a valid connection step, the DRP alternates between operating as a Source for detecting an attached Sink and presenting as a Sink to be detected by an attached Source. Ultimately this results in a Source-to-Sink connection.		N/A
4.5.1.2.1	Detecting a Valid Source-to-Sink Connection		N/A
	The general concept for setting up a valid connection between a Source and Sink is based on being able to detect terminations residing in the product being attached.		N/A
	To aid in defining the functional behavior of CC, a pull-up (Rp) and pull-down (Rd) termination model is used – actual implementation in hosts and devices may vary, for example, the pullup termination could be replaced by a current source. Figure 4-5 and Figure 4-6 illustrates two models, the first based on a pull-up resistor in the Source and the second replacing this with a current source.		N/A
	Initially, a Source exposes independent Rp terminations on its CC1 and CC2 pins, and a Sink exposes independent Rd terminations on its CC1 and CC2 pins, the Source-to-Sink combination of this circuit configuration represents a valid connection. To detect this, the Source monitors CC1 and CC2 for a voltage lower than its unterminated voltage – the choice of Rp is a function of the pull-up termination voltage and the Source's detection circuit. This indicates that either a Sink, a powered cable, or a Sink connected via a powered cable has been attached.		N/A
	Prior to application of VCONN, a powered cable exposes Ra on its VCONN pin. Ra		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	represents the load on VCONN plus any resistive elements to ground. In some cable plugs it might be a pure resistance and in others it may be simply the load.		
	The Source has to be able to differentiate between the presence of Rd and Ra to know whether there is a Sink attached and where to apply VCONN. The Source is not required to source VCONN unless Ra is detected.		N/A
	Two special termination combinations on the CC pins as seen by a Source are defined for directly attached Accessory Modes: Ra/Ra for Audio Adapter Accessory Mode (Appendix A) and Rd/Rd for Debug Accessory Mode (Appendix B).		N/A
	The Source uses de-bounce timers to reliably detect states on the CC pins to de-bounce the connection (tCCDebounce), and hide USB PD BMC communications (tPDDebounce).		N/A
	Once the Sink is powered, the Sink monitors CC1 and CC2 for a voltage greater than its local ground. The CC pin that is at a higher voltage (i.e. pulled up by Rp in the Source) indicates the orientation of the plug.		N/A
	Figure 4-3 shows how the inserted plug orientation is detected at the Source's receptacle by noting on which of the two CC pins in the receptacle an Rd termination is sensed. Now that the Source (Host) has recognized that a Sink (Device) is attached and the plug orientation is determined, it configures the TX/RX data bus routing to the receptacle.		N/A
	The Source (Host) then turns on VBUS. For the CC pin that does not connect Source-to-Sink through the cable, the Source supplies VCONN and may remove the termination. With the Sink (Device) now powered, it configures the USB data path. This completes the Host-to-Device connection.		N/A
	The Source monitors the CC wire for the loss of pull-down termination to detect detach. If the Sink is removed, the Source port removes any voltage applied to VBUS and VCONN, resets its interface configuration and resumes looking for a new Sink attach.		N/A
	Once a valid Source-to-Sink connection is established, alternatives to traditional USB power (VBUS as defined by either USB 2.0 or USB 3.2 specifications) may be available depending on the capabilities of the host and device. These include USB Type-C Current, USB Power Delivery, and USB Battery Charging 1.2.		N/A
	In the case where USB PD PR_Swap is used to swap the Source and Sink of VBUS, the supplier of VCONN remains unchanged during		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	and after the VBUS power swap. The new Source monitors the CC wire and the new Sink monitors VBUS to detect detach. When a detach event is detected, any voltages applied to VBUS and VCONN are removed, each port resets its interface configuration and resumes looking for an attach event.		
	In the case where USB PD DR_Swap is used to swap the data roles (DFP and UFP), the source of VBUS and VCONN do not change after the data role swap.		N/A
	In the case where USB PD VCONN Swap is used to swap the VCONN source, the VBUS Source/Sink and DFP/UFP roles are maintained during and after the VCONN swap.		N/A
	The last step in the normal USB Type-C connect process is for the USB device to be attached and enumerated per standard USB 2.0 and USB 3.2 processes.		N/A
4.5.1.3	Configuration Channel Functional Models		N/A
	The functional models for the configuration channel behavior based on the CC1 and CC2 pins are described in this section for each port type: Source, Sink and Dual-Role-Power (DRP).		N/A
	The figures in the following sections illustrate the CC1 and CC2 routing after the CC detection process is complete. In these figures, VBUS and VCONN may or may not actually be available.		N/A
4.5.1.3.1	Source Configuration Channel Functional Model		N/A
	Referring to Figure 4-7, a port that behaves as a Source has the following functional characteristics:		N/A
	1. The Source uses a FET to enable/disable power delivery across VBUS and initially the Source has VBUS disabled.		N/A
	2. The Source supplies pull-up resistors (Rp) on CC1 and CC2 and monitors both to detect a Sink. The presence of an Rd pull-down resistor on either pin indicates that a Sink is being attached. The value of Rp indicates the initial USB Type-C Current level supported by the host.		N/A
	3. The Source can optionally clamp the voltage on either of its CC pins. The minimum clamping voltage shall be vCC-Clamp. The clamp is intended to protect the Source circuitry associated with CC functionality.		N/A
	4. The Source uses the CC pin pull-down characteristic to detect and establish the correct routing for the SuperSpeed USB data path and determine which CC pin is intended for supplying VCONN.		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	5. Once a Sink is detected, the Source enables VBUS and VCONN.		N/A
	6. The Source can dynamically adjust the value of R_p to indicate a change in available USB Type-C Current to a Sink.		N/A
	7. The Source monitors the continued presence of R_d to detect Sink detach. When a detach event is detected, the Source removes, if supplied, VBUS and VCONN, and returns to step 2.		N/A
	8. If the Source supports advanced functions (USB Power Delivery and/or Alternate Modes), USB PD communication is required.		N/A
4.5.1.3.2	Sink Configuration Channel Functional Model		N/A
	Referring to Figure 4-9, a port that behaves as a Sink has the following functional characteristics:		N/A
	1. The Sink terminates both CC1 and CC2 to GND using pull-down resistors.		N/A
	2. The Sink determines that a Source is attached by the presence of power on VBUS.		N/A
	3. The Sink uses the CC pin pull-up characteristic to detect and establish the correct routing for the SuperSpeed USB data path.		N/A
	4. The Sink can optionally monitor CC to detect an available higher USB Type-C Current from the Source. The Sink shall manage its load to stay within the detected Source current limit.		N/A
	5. The Sink can optionally clamp the voltage on either of its CC pins. The minimum clamping voltage shall be $v_{CC-Clamp}$. The clamp is intended to protect the Sink circuitry associated with CC functionality.		N/A
	6. If the Sink supports advanced functions (USB Power Delivery and/or Alternate Modes), USB PD communication is required.		N/A
4.5.1.3.3	Dual-Role-Power (DRP) Configuration Channel Functional Model		N/A
	Referring to Figure 4-11, a port that can alternate between DFP and UFP behaviors has the following functional characteristics:		N/A
	1. The DRP uses a FET to enable/disable power delivery across VBUS and initially when in Source mode has VBUS disabled.		N/A
	2. The DRP uses switches for presenting as a Source or Sink.		N/A
	3. The DRP has logic used during initial attach to toggle between Source and Sink operation:		N/A
	a. Until a specific stable state is established, the DRP alternates between exposing itself as a Source and Sink. The timing of this process is		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	dictated by a period (tDRP), percentage of time that a DRP exposes Rp (dcSRC. DRP) and role transition time (tDRPTransition).		
	b. When the DRP is presenting as a Source, it follows Source operation to detect an attached Sink – if a Sink is detected, it applies VBUS, VCONN, and continues to operate as a Source (e.g., cease alternating).		N/A
	c. When the DRP is presenting as a Sink, it monitors VBUS to detect that it is attached to a Source – if a Source is detected, it continues to operate as a Sink (cease alternating).		N/A
	4. If the DRP supports advanced functions (USB Power Delivery and/or Alternate Modes), USB PD communication is required.		N/A
4.5.1.4	USB Type-C Port Power Roles and Role Swapping Mechanisms		N/A
	USB Type-C ports on products (USB hosts, USB devices, USB chargers, etc.) can be generally characterized as implementing one of seven power role behavioral models:		N/A
	Source-only		N/A
	Source (Default) – strong preference toward being a Source but subsequently capable of becoming a Sink using USB PD swap mechanisms.		N/A
	Sink-only		N/A
	Sink (Default) – strong preference toward being a Sink but subsequently capable of becoming a Source using USB PD swap mechanisms.		N/A
	DRP: Toggling (Source/Sink)		N/A
	DRP: Sourcing Device		N/A
	DRP: Sinking Host		N/A
	Two independent sets of swapping mechanisms are defined for USB Type-C port implementations, one based on role swapping within the initial state machine connection process and the other based on subsequent use of USB PD-based swapping mechanisms.		N/A
4.5.1.4.1	USB Type-C State-Machine-Based Role Swapping		N/A
	During the initial USB Type-C state machine connection process, the products being connected end up in one of the two following roles associated with the termination of its port:		N/A
	Rp - VBUS and VCONN source and behaving as a downstream facing port (USB Host)		N/A
	Rd - VBUS sink and behaving as an upstream facing port (USB Device)		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	A USB Type-C DRP-based product may incorporate either or both the Try.SRC and Try.SNK swap mechanisms to affect the resulting role. Try.SRC allows a DRP that has a policy-based preference to be a Source when connecting to another DRP to affect a transition from a destined Sink role to the Source role. Alternately, Try.SNK allows a DRP that has a policybased preference to be a Sink when connecting to another DRP to effect a transition from a destined Source role to the Sink role. Connection timing and other factors are involved in this process as defined in the USB Type-C state machine operation (see Section 4.5.2). It is important to note that these mechanisms, Try.SRC and Try.SNK, can only be used once as part of the initial connection process.		N/A
	Try.SRC and Try.SNK are intended to ensure more predictable power roles when initially connecting two DRPs, especially if the port partner does not support USB PD. For example, a small mobile device may want to implement Try.SNK, so that when attaching to a DRP laptop, the mobile device will always initially be the power sink. Similarly, a laptop or Power Bank may wish to implement Try.SRC to ensure it always sources power to attached DRPs. Selfpowered devices such as AMAs or those whose primary function is a data UFP may also consider implementing Try.SNK to ensure they can properly expose their functionality. If both sides support USB PD, the appropriate roles may then be further refined or swapped as per the USB PD specification.		N/A
4.5.1.4.2	USB PD-based Power Role, Data Role and VCONN Swapping		N/A
	Following the completion of the initial USB Type-C state machine connection process, products may use USB PD-based swapping mechanisms to command a change power roles, data roles and which end of the cable will supply VCONN. These mechanisms are:		N/A
	USB PD PR Swap : swaps Source (Rp) and Sink (Rd)		N/A
	USB PD DR Swap : swaps DFP (host data) and UFP (device data) roles		N/A
	USB PD VCONN Swap : swaps which port supplies VCONN		N/A
4.5.1.4.3	Power Role Behavioral Model Summary		N/A
4.5.2	CC Functional and Behavioral Requirements		P

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Clause	Requirement + Test	Result - Remark	Verdict
	This section provides the functional and behavioral requirements for implementing CC. The first sub-section provides connection state diagrams that are the basis for the remaining subsections.		N/A
	The terms Source (SRC) and Sink (SNK) used in this section refer to the port's power role while the terms DFP and UFP refer to the port's data role. A DRP (Dual-Role-Power) port is capable of acting as either a Source or Sink. Typically, Sources are found on hosts and supply VBUS while a Sink is found on a device and consumes power from VBUS. When a connection is initially made, the port's initial power state and data role are established. USB PD introduces three swap commands that may alter a port's power or data role:		N/A
	The PR_Swap command changes the port's power state as reflected in the following state machines. PR_Swap does not change the port sourcing VCONN.		N/A
	The DR_Swap command has no effect on the following state machines or VCONN as it only changes the port's data role.		N/A
	VCONN_Swap command changes the port sourcing VCONN. The PR_Swap command and DR_Swap command have no effect on the port sourcing VCONN.		N/A
	The connection state diagrams and CC behavior descriptions in this section describe the behavior of receptacle-based ports. The plug on a direct connect device or a device with a captive cable shall behave as a plug on a cable that is attached at its other end in normal orientation to a receptacle. These devices shall apply and sense CC voltage levels on pin A5 only and pin B5 shall have an impedance above zOPEN, unless it is a VCONN-Powered Accessory, in which case B5 shall have an impedance Ra.		N/A
4.5.2.1	Connection State Diagrams		N/A
	This section provides reference connection state diagrams for CC-based behaviors.		N/A
	Refer to Section 4.5.2.2 for the specific state transition requirements related to each state shown in the diagrams.		N/A
	Refer to Section 4.5.2.4 for a description of which states are mandatory for each port type, and a list of states where USB PD communication is permitted.		N/A
4.5.2.2	Connection State Machine Requirements		P
	Entry into any unattached state when "directed from any state" shall not be used to override tDRP toggle.		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	A DRP or a Sink may consume default power from VBUS in any state where it is not required to provide VBUS.		N/A
	The following two tables define the electrical states for a CC pin in both a Source and a Sink. Every port has CC1 and CC2 pins, each with its own individual CC pin state. The combination of a port's CC1 and CC2 pin states are be used to define the conditions under which a port transitions from one state to another.		N/A
4.5.2.2.1	Disabled State		P
	The Disabled state is where the port prevents connection from occurring by removing all terminations from the CC pins.		N/A
	The port should transition to the Disabled state from any other state when directed. When the port transitions to the Disabled state from Attached.SNK, it shall keep all terminations on the CC pins removed for a minimum of tErrorRecovery.		N/A
	A port may choose not to support the Disabled state. If the Disabled state is not supported, the port shall be directed to either the Unattached.SNK or Unattached.SRC states after power-on.		P
4.5.2.2.1.1	Disabled State Requirements		P
	The port shall not drive VBUS or VCONN, and shall present a high-impedance to ground (above zOPEN) on its CC1 and CC2 pins.		P
4.5.2.2.1.2	Exiting from Disabled State		N/A
	A Sink shall transition to Unattached.SNK when directed.		N/A
	A Source shall transition to Unattached.SRC when directed.		N/A
	A DRP shall transition to either Unattached.SNK or Unattached.SRC when directed.		N/A
4.5.2.2.2	ErrorRecovery Stat		N/A
	The ErrorRecovery state is where the port removes the terminations from the CC1 and CC2 pins for tErrorRecovery followed by transitioning to the appropriate Unattached.SNK or Unattached.SRC state based on port type. This is the equivalent of forcing a detach event and looking for a new attach.		N/A
	Ports that support USB Power Delivery shall support the ErrorRecovery state.		N/A
	Ports that support the ErrorRecovery state shall transition to the ErrorRecovery state from any other state when directed.		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	does not support USB Power Delivery may choose not to support the ErrorRecovery state. If the ErrorRecovery state is not supported, the port shall be directed to the Disabled state if supported. If the Disabled state is not supported, the port shall be directed to either the Unattached.SNK or Unattached.SRC states.		N/A
4.5.2.2.2.1	ErrorRecovery State Requirements		N/A
	The port shall not drive VBUS or VCONN, and shall present a high-impedance to ground (above zOPEN) on its CC1 and CC2 pins.		N/A
4.5.2.2.2.2	Exiting from ErrorRecovery State		N/A
	A Sink shall transition to Unattached.SNK after tErrorRecovery.		N/A
	A Source shall transition to Unattached.SRC after tErrorRecovery.		N/A
	A DRP (Figure 4-15) and a DRP with Accessory and Try.SNK Support (Figure 4-17) shall transition to Unattached.SNK after tErrorRecovery.		N/A
	A DRP with Accessory and Try.SRC Support (Figure 4-16) shall transition to Unattached.SRC after tErrorRecovery.		N/A
4.5.2.2.3	Unattached.SNK State		P
	When in the Unattached.SNK state, the port is waiting to detect the presence of a Source.		N/A
	A port with a dead battery shall enter this state while unpowered.		P
4.5.2.2.3.1	Unattached.SNK Requirements		P
	The port shall not drive VBUS or VCONN.		P
	Both CC1 and CC2 pins shall be independently terminated to ground through Rd.		P
	A Charge-Through VCONN-Powered USB Device shall isolate its Host-side port from its Charge-Through port, including CCs and VBUS, and independently terminate its Charge-Through port's CC1 and CC2 pins and Host-side port's CC pin to ground through Rd.		N/A
4.5.2.2.3.2	Exiting from Unattached.SNK State		P
	If the port supports USB PD or accessories, the port shall transition to AttachWait.SNK when the SNK.Rp state is present on at least one of its CC pins.		P
	The maximum times that a Port shall take to transition to AttachWait.SNK are the following:		N/A
	tNoToggleConnect when neither Port Partner is toggling		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	tOnePortToggleConnect when one Port Partner only is toggling		N/A
	When both Port Partners are toggling, a Port should transition to AttachWait.SNK within tTwoPortToggleConnect. Note that when both Port Partners are DRPs it is indeterminate whether the local port will transition to AttachWait.SRC or AttachWait.SNK.		N/A
	A USB 2.0 only Sink that doesn't support accessories and is self-powered or requires only default power and does not support USB PD may transition directly to Attached.SNK when VBUS is detected.		N/A
	A DRP shall transition to Unattached.SRC within tDRPTransition after the state of both CC pins is SNK.Open for tDRP – dcSRC.DRP · tDRP, or if directed.		P
	A Sink with Accessory support shall transition to Unattached.Accessory within tDRPTransition after the state of both the CC1 and CC2 pins is SNK.Open for tDRP – dcSRC.DRP · tDRP, or if directed.		N/A
	A Charge-Through VCONN-Powered USB Device shall transition to Unattached.SRC within tDRPTransition after the state of the Host-side port's CC pin is SNK.Open for tDRP – dcSRC.DRP · tDRP and both of the following is detected on the Charge-Through port.		N/A
	SNK.Rp state is detected on exactly one of the CC1 or CC2 pins for at least tCCDebounce		N/A
	VBUS is detected		N/A
	A Charge-Through VCONN-Powered USB Device shall transition to Attached.SNK when a Source connection is detected, as indicated by the SNK.Rp state on its Host-side port's CC pin.		N/A
4.5.2.2.4	AttachWait.SNK State		P
	When in the AttachWait.SNK state, the port has detected the SNK.Rp state on at least one of its CC pins and is waiting for VBUS.		N/A
	When in the AttachWait.SNK state, the Charge-Through VCONN-Powered USB Device has detected the SNK.Rp state on its Host-side port's CC pin and is waiting for host-side VBUS.		N/A
4.5.2.2.4.1	AttachWait.SNK Requirements		P
	The port shall not drive VBUS or VCONN.		P
	Both the CC1 and CC2 pins shall be independently terminated to ground through Rd.		P
	A Charge-Through VCONN-Powered USB Device shall isolate its Host-side port from its Charge-Through port, including CCs and		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	VBUS, and independently terminate its Charge-Through port's CC1 and CC2 pins and Host-side port's CC pin to ground through Rd.		
	It is strongly recommended that a USB 3.2 SuperSpeed device hold off VBUS detection to the device controller until the Attached.SNK state or the DebugAccessory.SNK state is reached, i.e. at least one CC pin is in the SNK.Rp state. Otherwise, it may connect as USB 2.0 when attached to a legacy host or hub's DFP.		N/A
4.5.2.2.4.2	Exiting from AttachWait. SNK State		P
	A Sink shall transition to Unattached.SNK when the state of both the CC1 and CC2 pins is SNK.Open for at least tPDDebounce.		N/A
	A DRP shall transition to Unattached.SRC when the state of both the CC1 and CC2 pins is SNK.Open for at least tPDDebounce.		N/A
	The port shall transition to Attached.SNK after the state of only one of the CC1 or CC2 pins is SNK.Rp for at least tCCDebounce and VBUS is detected. Note the Source may initiate USB PD communications which will cause brief periods of the SNK.Open state on one of the CC pins with the state of the other CC pin remaining SNK.Open, but this event will not exceed tPDDebounce.		P
	If the port is a VCONN-Powered Accessory or a VCONN-Powered USB Device, the port shall transition to Attached.SNK when either VCONN or VBUS is detected. The port may transition without waiting tCCDebounce on CC.		N/A
	If the port supports Debug Accessory Mode, the port shall transition to DebugAccessory.SNK if the state of both the CC1 and CC2 pins is SNK.Rp for at least tCCDebounce and VBUS is detected. Note the DAM Source may initiate USB PD communications which will cause brief periods of the SNK.Open state on one of the CC pins with the state of the other CC pin remaining SNK.Rp, but this event will not exceed tPDDebounce.		N/A
	A Charge-Through VCONN-Powered USB Device shall transition to Attached.SNK after the state of the Host-side port's CC pin is SNK.Rp for at least tCCDebounce and either host-side VCONN or VBUS is detected.		N/A
	A DRP that strongly prefers the Source role may optionally transition to Try.SRC instead of Attached.SNK when the state of only one CC pin has been SNK.Rp for at least tCCDebounce and VBUS is detected.		N/A
4.5.2.2.5	Attached.SNK State		P
	When in the Attached.SNK state, the port is attached and operating as a Sink. When the		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	port initially enters this state it is also operating as a UFP. The power and data roles can be changed using USB PD commands.		
	A port that entered this state directly from Unattached.SNK due to detecting VBUS shall not determine orientation or availability of higher than Default USB Power and shall not use USB PD.		N/A
4.5.2.2.5.1	Attached.SNK Requirements		P
	If the port needs to determine the orientation of the connector, it shall do so only upon entry to this state by detecting which of the CC1 or CC2 pins is connected through the cable (i.e., the CC pin that is in the SNK.Rp state).		N/A
	If the port supports signaling on SuperSpeed USB pairs, it shall functionally connect the SuperSpeed USB pairs and maintain the connection during and after a USB PD PR_Swap.		P
	If the port has entered the Attached.SNK state from the AttachWait.SNK or TryWait.SNK states, only one the CC1 or CC2 pins will be in the SNK.Rp state. The port shall continue to terminate this CC pin to ground through Rd.		P
	If the port has entered the Attached.SNK state from the Attached.SRC state following a USB PD PR_Swap, the port shall terminate the connected CC pin to ground through Rd.		P
	The port shall meet the Sink Power Sub-State requirements specified in Section 4.5.2.2.22.		P
	If the port is a VCONN-Powered USB Device, it shall respond to USB PD cable identity queries on SOP'. It shall not send or respond to messages on SOP. It shall ensure there is sufficient capacitance on CC to meet cReceiver as defined in USB PD.		N/A
	A Charge-Through VCONN-Powered USB Device shall isolate its Host-side port from its Charge-Through port, including CCs and VBUS, present a high-impedance to ground (above zOPEN) on its Charge-Through port's CC1 and CC2 pins and terminate its Host-side port's CC pin to ground through Rd.		N/A
	A Charge-Through VCONN-Powered USB Device shall start a Charge-Through Support Timer when it enters the Attached.SNK state. If a Charge-Through VCONN-Powered USB Device fails to exit the Attached.SNK state before the Charge-Through Support Timer exceeds tAMETimeout, it shall present a USB Billboard Device Class interface indicating that it does not support Charge-Through.		N/A
	A Charge-Through VCONN-Powered USB Device shall reset the Charge-Through Support Timer when it first receives any USB PD		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	Structured VDM Command it supports. If a Charge-Through VCONN-Powered USB Device receives a Structured VDM Command multiple times, it shall only reset the Charge-Through Support Timer once. This ensures a Charge-Through VCONN-Powered USB Device will present a USB Billboard Device Class interface if it fails to exit Attached.SNK while receiving repeated or continuous Structured VDM Commands (e.g., Discover Identity).		
	A Charge-Through VCONN-Powered USB Device shall reset the Charge-Through Support Timer when it receives any Data Message it supports. A Charge-Through VCONN-Powered USB Device shall hold the Charge-Through Support Timer in reset while it is in any USB PD BIST mode.		N/A
	Except for a VCONN-Powered USB Device or Charge-Through VCONN-Powered USB Device, the port may negotiate a USB PD PR_Swap, DR_Swap or VCONN_Swap.		N/A
	If the port supports Charge-Through VCONN-Powered USB Device, and an explicit USB PD contract has failed to be negotiated, the port shall query the identity of the cable via USB PD on SOP'.		N/A
	If the port supports Charge-Through VCONN-Powered USB Device, and an explicit USB PD contract has failed to be negotiated, the port shall query the identity of the cable via USB PD on SOP'.		N/A
	By default, upon entry from AttachWait.SNK or Unattached.SNK, VCONN shall not be supplied in the Attached.SNK state. If Attached.SNK is entered from Attached.SRC as a result of a USB PD PR_Swap, it shall maintain VCONN supply state, whether on or off, and its data role/connections. A USB PD DR_Swap has no effect on which port sources VCONN.		P
	The port may negotiate a USB PD VCONN_Swap. When the port successfully executes USB PD VCONN_Swap operation and was not sourcing VCONN, it shall start sourcing VCONN within tVCONNON. The port shall execute the VCONN_Swap in a make-before-break sequence in order to keep active USB Type-C to USB Type-C cables powered. When the port successfully executes USB PD VCONN_Swap operation and was sourcing VCONN, it shall stop sourcing VCONN within tVCONNOFF.		N/A
4.5.2.2.5.2	Exiting from Attached.SNK State		P
	A port that is not a VCONN-Powered USB Device and is not in the process of a USB PD		P

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Clause	Requirement + Test	Result - Remark	Verdict
	PR_Swap or a USB PD Hard Reset or a USB PD FR_Swap shall transition to Unattached.SNK within tSinkDisconnect when VBUS falls below vSinkDisconnect for VBUS operating at or below 5 V or below vSinkDisconnectPD when negotiated by USB PD to operate above 5 V.		
	A VCONN-Powered USB Device shall return to Unattached.SNK when VBUS has fallen below vSinkDisconnect and VCONN has fallen below vVCONNDisconnect.		N/A
	A port that has entered into USB PD communications with the Source and has seen the CC voltage exceed vRd-USB may monitor the CC pin to detect cable disconnect in addition to monitoring VBUS.		N/A
	A port that is monitoring the CC voltage for disconnect (but is not in the process of a USB PD PR_Swap or USB PD FR_Swap) shall transition to Unattached.SNK within tSinkDisconnect after the CC voltage remains below vRd-USB for tPDDebounce.		N/A
	If supplying VCONN, the port shall cease to supply it within tVCONNOff of exiting Attached.SNK.		P
	A Charge-Through VCONN-Powered USB Device shall transition to CTUnattached.VPD if VCONN is present and the state of its Host-side port's CC pin is SNK.Open for tVPDCTDD.		N/A
	A port that via SOP' has detected an attached Charge-Through VCONN-Powered USB Device shall transition to TryWait.SRC if implemented, or transition to Unattached.SRC or Unattached.Accessory if TryWait.SRC is not supported. This transition may be delayed until the device has sufficient battery charge needed to remain powered until it reaches the CTAttached.SNK state.		N/A
	After receiving a USB PD PS_RDY from the original Source during a USB PD PR_Swap, the port shall transition directly to the Attached.SRC state (i.e., remove Rd from CC, assert Rp on CC and supply VBUS), but shall maintain its VCONN supply state, whether off or on, and its data role/connections.		P
4.5.2.2.6	UnattachedWait.SRC State		N/A
	When in the UnattachedWait.SRC state, the port is discharging the CC pin that was providing VCONN in the previous Attached.SRC state.		N/A
4.5.2.2.6.1	UnattachedWait.SRC Requirements		N/A
	The port shall not enable VBUS or VCONN.		N/A
	The port shall complete the VCONN turn off initiated when leaving the previous		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	Attached.SRC state.		
	The port shall continue to provide an Rp termination, as specified in Table 4-24, on the CC pin not being discharged.		N/A
	The port shall not provide an Rp termination on the CC pin being discharged.		N/A
	The port shall not provide an Rp termination on the CC pin being discharged.		N/A
	The port shall discharge the CC pin being discharged below vVCONNDIScharge.		N/A
4.5.2.2.6.2	Exiting from UnattachedWait.SRC State		N/A
	The port shall transition to Unattached.SRC when VCONN is below vVCONNDIScharge. The port may delay this transition to allow the cable plug more time to reapply Ra.		N/A
4.5.2.2.7	Unattached.SRC State		P
	When in the Unattached.SRC state, the port is waiting to detect the presence of a Sink or an Accessory.		N/A
	When in the Unattached.SRC state, the Charge-Through VCONN-Powered USB Device has detected a Source on its Charge-Through port and is independently monitoring its Host-side port to detect the presence of a Sink.		N/A
4.5.2.2.7.1	Unattached.SRC Requirements		P
	The port shall not drive VBUS or VCONN.		P
	The port shall source current on both the CC1 and CC2 pins independently.		P
	The port shall provide a separate Rp termination on the CC1 and CC2 pins as specified in Table 4-24. Note: A Source with a captive cable or just a plug presents a single Rp termination on its CC pin (A5).		P
	The Charge-Through VCONN-Powered USB Device shall isolate its Host-side port from its Charge-Through port, including CCs and VBUS. The Charge-Through VCONN-Powered USB Device shall ensure that it is powered by VBUS from the Charge-Through port.		N/A
	Upon entry into this state, the Charge-Through VCONN-Powered USB Device shall remove its Rd termination to ground on the Host-side port CC and provide an Rp termination instead advertising Default USB Power, as specified in Table 4-24, and continue to independently terminate its Charge-Through port's CC1 and CC2 pins to ground through Rd.		N/A
4.5.2.2.7.2	Exiting from Unattached.SRC State		P
	The port shall transition to AttachWait.SRC		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	when:		
	The SRC.Rd state is present on either the CC1 or CC2 pin or		P
	The SRC.Ra state is present on both the CC1 and CC2 pins.		P
	The maximum times that a Port shall take to transition to AttachWait.SRC are the following:		N/A
	tNoToggleConnect when neither Port Partner is toggling		N/A
	tOnePortToggleConnect when one Port Partner only is toggling		N/A
	When both Port Partners are toggling, a Port should transition to AttachWait.SRC within tTwoPortToggleConnect. Note that when both Port Partners are DRPs it is indeterminate whether the local port will transition to AttachWait.SRC or AttachWait.SNK.		N/A
	The Charge-Through VCONN-Powered USB Device shall transition to AttachWait.SRC when host-side VBUS is vSafe0V and SRC.Rd state is detected on the Host-side port's CC pin.		N/A
	A DRP shall transition to Unattached.SNK within tDRPTransition after dcSRC.DRP · tDRP, or if directed.		P
	A Charge-Through VCONN-Powered USB Device shall transition to Unattached.SNK within tDRPTransition after dcSRC.DRP · tDRP, or if Charge-Through VBUS is removed.		N/A
4.5.2.2.8	AttachWait.SRC State		P
	The AttachWait.SRC state is used to ensure that the state of both of the CC1 and CC2 pins is stable after a Sink is connected.		N/A
	When in the AttachWait.SRC state, the Charge-Through VCONN-Powered USB Device ensures that the state of Host-side port's CC pin is stable after a Sink is connected.		N/A
4.5.2.2.8.1	AttachWait.SRC Requirements		N/A
	The requirements for this state are identical to Unattached.SRC.		N/A
4.5.2.2.8.2	Exiting from AttachWait.SRC State		P
	The port shall transition to Attached.SRC when VBUS is at vSafe0V and the SRC.Rd state is detected on exactly one of the CC1 or CC2 pins for at least tCCDebounce.		N/A
	The Charge-Through VCONN-Powered USB Device shall transition to Try.SNK when the hostside VBUS is at vSafe0V and the SRC.Rd state is on the Host-side port's CC pin for at least tCCDebounce.		N/A
	If the port supports Audio Adapter Accessory Mode, it shall transition to AudioAccessory		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	when the SRC.Ra state is detected on both the CC1 and CC2 pins for at least tCCDebounce.		
	If the port supports Debug Accessory Mode, it shall transition to UnorientedDebugAccessory.SRC when VBUS is at vSafe0V and the SRC.Rd state is detected on both the CC1 and CC2 pins for at least tCCDebounce.		N/A
	A Source shall transition to Unattached.SRC and a DRP to Unattached.SNK when the SRC.Open state is detected on both the CC1 and CC2 pins. The Source shall detect the SRC.Open state within tSRCDisconnect, but should detect it as quickly as possible.		N/A
	A Source shall transition to Unattached.SRC and a DRP to Unattached.SNK when the SRC.Open state is detected on either the CC1 or CC2 pin and the other CC pin is SRC.Ra. The Source shall detect the SRC.Open state within tSRCDisconnect, but should detect it as quickly as possible.		N/A
	A Charge-Through VCONN-Powered USB Device shall transition to Unattached.SNK when the SRC.Open state is detected on the Host-side port's CC or if Charge-Through VBUS falls below vSinkDisconnect. The Charge-Through VCONN-Powered USB Device shall detect the SRC.Open state within tSRCDisconnect, but should detect it as quickly as possible.		N/A
	A DRP that strongly prefers the Sink role may optionally transition to Try.SNK instead of Attached.SRC when VBUS is at vSafe0V and the SRC.Rd state is detected on exactly one of the CC1 or CC2 pins for at least tCCDebounce.		P
4.5.2.2.9	Attached.SRC State		P
	When in the Attached.SRC state, the port is attached and operating as a Source. When the port initially enters this state it is also operating as a DFP. Subsequently, the initial power and data roles can be changed using USB PD commands.		N/A
	When in the Attached.SRC state, the Charge-Through VCONN-Powered USB Device has detected a Sink on its Host-side port and has connected the Charge-Through port VBUS to the Host-side port VBUS.		N/A
4.5.2.2.9.1	Attached.SRC Requirements		P
	If the port needs to determine the orientation of the connector, it shall do so only upon entry to the Attached.SRC state by detecting which of the CC1 or CC2 pins is connected through the cable, i.e., which CC pin is in the SRC.Rd state.		N/A
	If the port has entered this state from the AttachWait.SRC state or the Try.SRC state, the SRC.Rd state will be on only one of the CC1 or		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	CC2 pins. The port shall source current on this CC pin and monitor its state.		
	If the port has entered this state from the Attached.SNK state as the result of a USB PD PR_Swap, the port shall source current on the connected CC pin and monitor its state.		P
	The port shall provide an Rp as specified in Table 4-24.		N/A
	The port shall supply VBUS current at the level it advertises on Rp.		N/A
	The port shall supply VBUS within tVBUSON of entering this state, and for as long as it is operating as a power source.		N/A
	The port shall not initiate any USB PD communications until VBUS reaches vSafe5V.		N/A
	If the port supports signaling on SuperSpeed USB pairs, it shall:		N/A
	Functionally connect the SuperSpeed USB pairs		N/A
	For VCONN, do one of two things:		N/A
	Supply VCONN unconditionally to the CC pin not in the SRC.Rd state, or		N/A
	Supply VCONN to the CC pin in the SRC.Ra state.		N/A
	A port that does not support signaling on SuperSpeed USB pairs may supply VCONN in the same manner described above.		N/A
	The port may negotiate a USB PD PR_Swap, DR_Swap or VCONN_Swap.		N/A
	If the port supplies VCONN, it shall do so within tVCONNON.		N/A
	The port may query the identity of the cable via USB PD on SOP'. If it detects that it is connected to a VCONN-Powered USB Device, the port may remove VBUS and discharge it to vSafe0V, while continuing to remain in this state with VCONN applied. The port may also initiate other SOP' communication.		N/A
	The port shall not supply VCONN if it has entered this state as a result of a USB PD PR_Swap and was not previously supplying VCONN. A USB PD DR_Swap has no effect on which port sources VCONN.		P
	The port may negotiate a USB PD VCONN_Swap. When the port successfully executes USB PD VCONN_Swap operation and was sourcing VCONN, it shall stop sourcing VCONN within tVCONNOFF. The port shall execute the VCONN_Swap in a make-before-break sequence in order to keep active		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	USB Type-C to USB Type-C cables powered. When the port successfully executes USB PD VCONN_Swap operation and was not sourcing VCONN, it shall start sourcing VCONN within tVCONNON.		
	The Charge-Through VCONN-Powered USB Device shall continue to isolate its Host-side port's CC pin from its Charge-Through CC pins.		N/A
	The Charge-Through VCONN-Powered USB Device shall maintain its Rp termination advertising Default USB Power on the Host-side port's CC pin, and continue to independently terminate its Charge-Through port's CC1 and CC2 pins to ground through Rd.		N/A
	The Charge-Through VCONN-Powered USB Device shall immediately connect the Charge-Through port's VBUS through to the Host-side port's VBUS.		N/A
	The Charge-Through VCONN-Powered USB Device shall ensure that it is powered entirely by VBUS.		N/A
	The Charge-Through VCONN-Powered USB Device shall only respond to USB PD Discover Identity queries on SOP' on its Host-side port and complete any active queries prior to exiting this state. It shall ensure there is sufficient capacitance on the Host-side port CC to meet cReceiver as defined in USB PD.		N/A
4.5.2.2.9.2	Exiting from Attached.SRC State		P
	A Source that is supplying VCONN or has yielded VCONN source responsibility to the Sink through USB PD VCONN_Swap messaging shall transition to UnattachedWait.SRC when the SRC.Open state is detected on the monitored CC pin. The Source shall detect the SRC.Open state within tSRCDisconnect, but should detect it as quickly as possible.		N/A
	A Source that is not supplying VCONN and has not yielded VCONN responsibility to the Sink through USB PD VCONN_Swap messaging shall transition to Unattached.SRC when the SRC.Open state is detected on the monitored CC pin. The Source shall detect the SRC.Open state within tSRCDisconnect, but should detect it as quickly as possible.		N/A
	When the SRC.Open state is detected on the monitored CC pin, a DRP shall transition to Unattached.SNK unless it strongly prefers the Source role. In that case, it shall transition to TryWait.SNK. This transition to TryWait.SNK is needed so that two devices that both prefer the Source role do not loop endlessly between Source and Sink. In other words, a DRP that would enter Try.SRC from AttachWait.SNK shall		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	enter TryWait.SNK for a Sink detach from Attached.SRC.		
	A DRP that supports Charge-Through VCONN-Powered USB Device shall transition to CTUnattached.SNK if the connected device identifies itself as a Charge-Through VCONNPowered USB Device in its Discover Identity Command response. The DRP may delay this transition in order to perform further SOP' communication.		N/A
	A port shall cease to supply VBUS within tVBUSOFF of exiting Attached.SRC.		N/A
	A port that is supplying VCONN shall cease to supply it within tVCONNOff of exiting Attached.SRC, unless it is exiting as a result of a USB PD PR_Swap or is transitioning into the CTUnattached.SNK state.		N/A
	After a USB PD PR_Swap is accepted (i.e., either an Accept message is received or acknowledged), a DRP shall transition directly to the Attached.SNK state (i.e., remove Rp from CC, assert Rd on CC and stop supplying VBUS) and maintain its current data role, connection and VCONN supply state.		P
	A Charge-Through VCONN-Powered USB Device shall transition to Unattached.SNK when VBUS falls below vSinkDisconnect or the Host-side port's CC pin is SRC.Open. The Charge- Through VCONN-Powered USB Device shall detect the SRC.Open state within tSRCDDisconnect, but should detect it as quickly as possible.		N/A
4.5.2.2.10	Try.SRC State		N/A
	When in the Try.SRC state, the port is querying to determine if the port partner supports the Sink role.		N/A
4.5.2.2.10.1	Try.SRC Requirements		N/A
	The port shall not drive VBUS or VCONN.		N/A
	The port shall source current on both the CC1 and CC2 pins independently.		N/A
	The port shall provide an Rp as specified in Table 4-24.		N/A
4.5.2.2.10.2	Exiting from Try.SRC State		N/A
	The port shall transition to Attached.SRC when the SRC.Rd state is detected on exactly one of the CC1 or CC2 pins for at least tTryCCDebounce.		N/A
	The port shall transition to TryWait.SNK after tDRPTry and the SRC.Rd state has not been detected and VBUS is within vSafe0V, or after tTryTimeout and the SRC.Rd state has not been detected.		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
4.5.2.2.11	TryWait.SNK State		N/A
	When in the TryWait.SNK state, the port has failed to become a Source and is waiting to attach as a Sink. Alternatively the port is responding to the Sink being removed while in the Attached.SRC state.		N/A
4.5.2.2.11.1	TryWait.SNK Requirements		N/A
	The port shall not drive VBUS or VCONN.		N/A
	Both the CC1 and CC2 pins shall be independently terminated to ground through Rd.		N/A
4.5.2.2.11.2	Exiting from TryWait.SNK State		N/A
	The port shall transition to Attached.SNK after tCCDebounce if or when VBUS is detected. Note the Source may initiate USB PD communications which will cause brief periods of the SNK.Open state on both the CC1 and CC2 pins, but this event will not exceed tPDDebounce.		N/A
	The port shall transition to Unattached.SNK when the state of both of the CC1 and CC2 pins is SNK.Open for at least tPDDebounce.		N/A
4.5.2.2.12	Try.SNK State		P
	When in the Try.SNK state, the port is querying to determine if the port partner supports the Source role.		N/A
	When in the Try.SNK state, the Charge-Through VCONN-Powered USB Device is querying to determine if the port partner on the Host-side port supports the Source role.		N/A
4.5.2.2.12.1	Try.SNK Requirements		P
	The port shall not drive VBUS or VCONN.		P
	Both the CC1 and CC2 pins shall be independently terminated to ground through Rd.		P
	The Charge-Through VCONN-Powered USB Device shall isolate its Host-side port from its Charge-Through port, including CCs and VBUS. The Charge-Through VCONN-Powered USB Device shall ensure that it is powered by VBUS from the Charge-Through port.		N/A
	The Charge-Through VCONN-Powered USB Device shall remove its Rp termination (Default USB Power advertisement) on the Host-side port CC and provide an Rd termination to ground instead, as specified in Table 4-24 and remain to independently terminate its Charge-Through port's CC1 and CC2 pins to ground through Rd.		N/A
4.5.2.2.12.2	Exiting from Try.SNK State		P

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Clause	Requirement + Test	Result - Remark	Verdict
	The port shall wait for tDRPTry and only then begin monitoring the CC1 and CC2 pins for the SNK.Rp state.		N/A
	The port shall then transition to Attached.SNK when the SNK.Rp state is detected on exactly one of the CC1 or CC2 pins for at least tTryCCDebounce and VBUS is detected.		P
	Alternatively, the port shall transition to TryWait.SRC if SNK.Rp state is not detected for tTryCCDebounce.		N/A
	The Charge-Through VCONN-Powered USB Device shall wait for tDRPTry and only then begin monitoring the Host-side port's CC pin for the SNK.Rp state.		N/A
	The Charge-Through VCONN-Powered USB Device shall wait for tDRPTry and only then begin monitoring the Host-side port's CC pin for the SNK.Rp state.		N/A
	Alternatively, the Charge-Through VCONN-Powered USB Device shall transition to TryWait.SRC if Host-side SNK.Rp state is not detected for tTryCCDebounce.		N/A
	A Sink with Accessory Support shall transition to Unsupported.Accessory if SNK.Rp state is not detected for tDRPTryWait.		N/A
4.5.2.2.13	TryWait.SRC State		N/A
	When in the TryWait.SRC state, the port has failed to become a Sink and is waiting to attach as a Source.		N/A
	When in the TryWait.SRC state, the Charge-Through VCONN-Powered USB Device has failed to become a Sink on its Host-side port and is waiting to attach as a Source on its Host-side port.		N/A
4.5.2.2.13.1	TryWait.SRC Requirements		N/A
	The requirements for this state are identical to Unattached.SRC.		N/A
4.5.2.2.13.2	Exiting from TryWait.SRC State		N/A
	The port shall transition to Attached.SRC when VBUS is at vSafe0V and the SRC.Rd state is detected on exactly one of the CC pins for at least tTryCCDebounce.		N/A
	The Charge-Through VCONN-Powered USB Device shall transition to Attached.SRC when host-side VBUS is at vSafe0V and the SRC.Rd state is detected on the Host-side port's CC pin for at least tTryCCDebounce.		N/A
	The port shall transition to Unattached.SNK after tDRPTry if neither of the CC1 or CC2 pins are in the SRC.Rd state.		N/A
	The Charge-Through VCONN-Powered USB Device shall transition to Unattached.SNK after tDRPTry if the Host-side port's CC pin is not in the SRC.Rd state.		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
4.5.2.2.14	Unattached.Accessory State		P
	The Unattached.Accessory state allows accessory-supporting Sinks to connect to audio or VCONN-Powered Accessories.		N/A
	This state is functionally equivalent to the Unattached.SRC state in a DRP, except that Attached.SRC is not supported.		N/A
4.5.2.2.14.1	Unattached.Accessory Requirements		P
	The port shall not drive VBUS or VCONN.		P
	The port shall source current on both the CC1 and CC2 pins independently.		P
	The port shall provide an Rp as specified in Table 4-24.		P
4.5.2.2.14.2	Exiting from Unattached.Accessory State		P
	A port that supports Audio Adapter Accessory Mode shall transition to AttachWait.Accessory when the state of both CC pins is SRC.Ra.		N/A
	A port that supports VCONN-Powered Accessories also shall transition to AttachWait.Accessory when the state of either CC1 or CC2 pin is SRC.Ra and the other CC pin is SRC.Rd.		P
	The maximum time the local port shall take to transition from Unattached.Accessory to the AttachWait.Accessory state when an Audio Adapter Accessory or VCONN-Powered Accessory is present is tOnePortToggleConnect.		N/A
	Otherwise, the port shall transition to Unattached.SNK within tDRPTransition after dcSRC.DRP · tDRP, or if directed.		N/A
4.5.2.2.15	AttachWait.Accessory State		P
	The AttachWait.Accessory state is used to ensure that the state of both of the CC1 and CC2 pins is stable after a cable is plugged in.		N/A
4.5.2.2.15.1	AttachWait.Accessory Requirements		N/A
	The requirements for this state are identical to Unattached.Accessory.		N/A
4.5.2.2.15.2	Exiting from AttachWait.Accessory State		P
	If the port supports Audio Adapter Accessory Mode, it shall transition to AudioAccessory when the state of both the CC1 and CC2 pins is SRC.Ra for at least tCCDebounce.		P
	The port shall transition to Unattached.SNK when the state of either the CC1 or CC2 pin is SRC.Open for at least tCCDebounce.		P
	If the port supports VCONN-Powered Accessories, it shall transition to PoweredAccessory state if the state of either the CC1 or CC2 pin is SRC.Rd and the other		P

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Clause	Requirement + Test	Result - Remark	Verdict
	CC pin is SRC.Ra concurrently for at least tCCDebounce.		
4.5.2.2.16	AudioAccessory State		P
	The AudioAccessory state is used for the Audio Adapter Accessory Mode specified in Appendix A.		N/A
4.5.2.2.16.1	AudioAccessory Requirements		P
	The port shall reconfigure its pins as detailed in Appendix A.		P
	The port shall not drive VBUS or VCONN. A port that sinks current from the audio accessory over VBUS shall not draw more than 500 mA.		P
	The port shall provide an Rp as specified in Table 4-24.		P
	The port shall source current on at least one of the CC1 or CC2 pins and monitor to detect when the state is no longer SRC.Ra. If the port sources and monitors only one of CC1 or CC2, then it shall ensure that the termination on the unmonitored CC pin does not affect the monitored signal when the port is connected to an Audio Accessory that may short both CC1 and CC2 pins together.		P
4.5.2.2.16.2	Exiting from AudioAccessory State		P
	If the port is a Sink, the port shall transition to Unattached.SNK when the state of the monitored CC1 or CC2 pin(s) is SRC.Open for at least tCCDebounce.		P
	If the port is a Source or DRP, the port shall transition to Unattached.SRC when the state of the monitored CC1 or CC2 pin(s) is SRC.Open for at least tCCDebounce.		N/A
4.5.2.2.17	UnorientedDebugAccessory.SRC		N/A
	The UnorientedDebugAccessory.SRC state is used for the Debug Accessory Mode specified in Appendix B.		N/A
4.5.2.2.17.1	UnorientedDebugAccessory.SRC Requirements		N/A
	This mode is for debug only and shall not be used for communicating with commercial products.		N/A
	The port shall provide an Rp as specified in Table 4-24 on both the CC1 and CC2 pins and monitor to detect when the state of either is SRC.Open.		N/A
	The port shall supply VBUS current at the level it advertises on Rp. The port shall not drive VCONN.		N/A
	The port may connect any non-orientation specific debug signals for Debug Accessory Mode operation only after entry to this state.		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
4.5.2.2.17.2	Exiting from UnorientedDebugAccessory.SRC State		N/A
	If the port is a Source, the port shall transition to Unattached.SRC when the SRC.Open state is detected on either the CC1 or CC2 pin.		N/A
	If the port is a DRP, the port shall transition to Unattached.SNK when the SRC.Open state is detected on either the CC1 or CC2 pin.		N/A
	The port shall transition to OrientedDebugAccessory.SRC state if orientation is required and detected as described in Section B.2.6.1.2.		N/A
4.5.2.2.18	OrientedDebugAccessory.SRC State		N/A
	The OrientedDebugAccessory.SRC state is used for the Debug Accessory Mode specified in Appendix B.		N/A
4.5.2.2.18.1	OrientedDebugAccessory.SRC State Requirements		N/A
	This mode is for debug only and shall not be used for communicating with commercial products.		N/A
	The port shall provide an Rp as specified in Table 4-24 on both the CC1 and CC2 pins and monitor to detect when the state of either is SRC.Open.		N/A
	The port shall supply VBUS current at the level it advertises on Rp. The port shall not drive VCONN.		N/A
	The port shall connect any orientation specific debug signals for Debug Accessory Mode operation only after entry to this state. Any non-orientation specific debug signals for Debug Accessory Mode operation shall be connected or remain connected in this state.		N/A
	If the port needs to establish USB PD communications, it shall do so only after entry to this state. The port shall not initiate any USB PD communications until VBUS reaches vSafe5V. In this state, the port takes on the initial USB PD role of DFP/Source.		N/A
4.5.2.2.18.2	Exiting from OrientedDebugAccessory.SRC State		N/A
	If the port is a Source, the port shall transition to Unattached.SRC when the SRC.Open state is detected on either the CC1 or CC2 pin.		N/A
	If the port is a DRP, the port shall transition to Unattached.SNK when the SRC.Open state is detected on either the CC1 or CC2 pin.		N/A
4.5.2.2.19	DebugAccessory.SNK		P
	The DebugAccessory.SNK state is used for the Debug Accessory Mode specified in Appendix B.		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
4.5.2.2.19.1	DebugAccessory.SNK Requirements		P
	This mode is for debug only and shall not be used for communicating with commercial products.		P
	The port shall not drive VBUS or VCONN.		P
	The port shall provide an Rd as specified in Table 4-25 on both the CC1 and CC2 pins and monitor to detect when the state of either is SRC. Open.		N/A
	If supported, orientation is determined as outlined in Section B.2.6.1.1. The port shall connect any debug signals for Debug Accessory Mode operation only after entry to this state.		N/A
4.5.2.2.19.2	Exiting from DebugAccessory.SNK State		N/A
	The port shall transition to Unattached.SNK when VBUS is no longer present.		N/A
4.5.2.2.20	PoweredAccessory State		P
	When in the PoweredAccessory state, the port is powering a VCONN-Powered Accessory or VCONN-Powered USB Device.		N/A
4.5.2.2.20.1	PoweredAccessory Requirements		P
	If the port needs to determine the orientation of the connector, it shall do so only upon entry to the PoweredAccessory state by detecting which of the CC1 or CC2 pins is connected through the cable (i.e., which CC pin is in the SRC.Rd state).		N/A
	The SRC.Rd state is detected on only one of the CC1 or CC2 pins. The port shall advertise either 1.5 A or 3.0 A (see Table 4-24) on this CC pin and monitor its state.		P
	The port shall supply VCONN on the unused CC pin within tVconnON-PA of entering the PoweredAccessory state.		P
	The port shall not drive VBUS.		P
	When the port initially enters the PoweredAccessory state it shall operate as a USB Power Delivery Source with a DFP data role. In addition, the port shall support at least one of the following:		P
	Use USB PD to establish an explicit contract and then use Structured Vendor Defined Messages (Structured VDMs) to identify a VCONN-Powered Accessory and enter an Alternate Mode.		P
	Use USB PD to query the identity of a VCONN-Powered USB Device (that operates as a cable plug responding to SOP').		N/A
4.5.2.2.20.2	Exiting from PoweredAccessory State		P
	The port shall transition to Unattached.SNK		P

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Clause	Requirement + Test	Result - Remark	Verdict
	when the SRC. Open state is detected on the monitored CC pin.		
	The port shall transition to Try.SNK if the attached device is not a VCONN-Powered Accessory or VCONN-Powered USB Device. For example, the attached device does not support USB PD or does not respond to USB PD commands required for a VCONN-Powered Accessory (e.g., Discover SVIDs, Discover Modes, etc.) or is a Sink or DRP attached through a Powered Cable.		P
	The port shall transition to Unsupported.Accessory if the attached device is a VCONN-Powered Accessory but the port has not successfully entered an Alternate Mode within tAMETimeout (see Appendix E).		P
	A port that supports Charge-Through VCONN-Powered USB Device shall transition to CTUnattached.SNK if the connected device identifies itself as a Charge-Through VCONNPowered USB Device in its Discover Identity Command response. The port may delay this transition in order to perform further SOP' communication.		N/A
	The port shall cease to supply VCONN within tVCONNOff of exiting the PoweredAccessory state unless it is transitioning into the CTUnattached.SNK state.		P
4.5.2.2.21	Unsupported.Accessory State		P
	If a VCONN-Powered Accessory does not enter an Alternate Mode, the Unsupported.Accessory state is used to wait until the accessory is unplugged before continuing.		N/A
4.5.2.2.21.1	Unsupported.Accessory Requirements		P
	Only one of the CC1 or CC2 pins shall be in the SRC.Rd state. The port shall advertise Default USB Power (see Table 4-24) on this CC pin and monitor its voltage.		P
	The port shall not drive VBUS or VCONN.		P
	A Sink with either VCONN-Powered Accessory or VCONN-Powered USB Device support shall provide user notification that it does not recognize or support the attached accessory or device.		N/A
4.5.2.2.21.2	Exiting from Unsupported.Accessory		P
	The port shall transition to Unattached.SNK when the SRC. Open state is detected on the monitored CC pin.		P
4.5.2.2.22	CTUnattached.VPD State		N/A
	When in the CTUnattached.VPD state, the Charge-Through VCONN-Powered USB Device has detected SNK.Open on its host port		N/A

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	for tVPDCTDD, indicating that it is connected to a Charge-Through capable Source, and is independently monitoring its Charge-Through port for the presence of a pass-through Power Source.		
	This state may also have been entered through detach of a Power Source on the Charge-Through port or detach of a sink from the CTVPD's Charge-through port.		N/A
4.5.2.2.22.1	CTUnattached.VPD Requirements		N/A
	The Charge-Through VCONN-Powered USB Device shall isolate its Host-side port from its Charge-Through port, including CCs and VBUS. The Charge-Through VCONN-Powered USB Device shall ensure that it is powered by VCONN, does not consume more than ICCS (USB 3.2) / ICCSH (USB 2.0) from VBUS for monitoring, and is sufficiently isolated from VBUS to tolerate high voltages during Charge-Through operation.		N/A
	Upon entry into this state, the device shall remove its Rd termination to ground (if present) on the Host-side port CC and provide an Rp termination advertising 3.0 A instead, as specified in Table 4-24. Note that because VBUS is not provided, the Rp termination signals continued connection to the port partner but does not carry with it any current advertisement.		N/A
	The Charge-Through VCONN-Powered USB Device shall only respond to USB PD Discover Identity queries on SOP' on its Host-side port. It shall ensure there is sufficient capacitance on the Host-side port CC to meet cReceiver as defined in USB PD.		N/A
	The Charge-Through VCONN-Powered USB Device shall independently terminate both the Charge-Through port's CC1 and CC2 pins to ground through Rd.		N/A
	The Charge-Through VCONN-Powered USB Device shall provide a bypass capacitance of CCTB on the Charge-Through Port's VBUS pins.		N/A
4.5.2.2.22.2	Exiting from CTUnattached.VPD		N/A
	The Charge-Through VCONN-Powered USB Device shall transition to CTAttachWait.VPD when a Source connection is detected on the Charge-Through port, as indicated by the SNK.Rp state on exactly one of the Charge-Through port's CC pins.		N/A
	Debug accessories are not supported on the Charge-Through port.		N/A
	The Charge-Through VCONN-Powered USB Device shall transition to Unattached.SNK if		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	VCONN falls below vVCONNDisconnect.		
	The Charge-Through VCONN-Powered USB Device shall transition to CTUnattached. Unsupported within tDRPTransition after the state of both the Charge-Through port's CC1 and CC2 pins is SNK.Open for tDRP – dcSRC.DRP · tDRP, or if directed.		N/A
4.5.2.2.23	CTAttachWait.VPD State		N/A
	When in the CTAttachWait.VPD state, the device has detected the SNK.Rp state on exactly one of its Charge-Through port's CC pins and is waiting for VBUS on the Charge-Through port.		N/A
4.5.2.2.23.1	CTAttachWait.VPD Requirements		N/A
	The Charge-Through VCONN-Powered USB Device shall isolate its Host-side port from its Charge-Through port, including CCs and VBUS. The Charge-Through VCONN-Powered USB Device shall ensure that it is powered by VCONN, does not consume more than ICCS (USB 3.2) / ICCSH (USB 2.0) from VBUS for monitoring, and is sufficiently isolated from VBUS to tolerate high voltages during Charge-Through operation.		N/A
	The Charge-Through VCONN-Powered USB Device shall maintain its Rp termination advertising 3.0 A on the Host-side port's CC pin, as well as the independent terminations to ground through Rd on the Charge-Through port's CC1 and CC2 pins.		N/A
	The Charge-Through VCONN-Powered USB Device shall only respond to USB PD Discover Identity queries on SOP' on its Host-side port, and complete any active queries prior to exiting this state. It shall ensure there is sufficient capacitance on the Host-side port CC to meet cReceiver as defined in USB PD.		N/A
4.5.2.2.23.2	Exiting from CTAttachWait.VPD		N/A
	The Charge-Through VCONN-Powered USB Device shall transition to CTUnattached.VPD when the state of both the Charge-Through port's CC1 and CC2 pins are SNK.Open for at least tPDDebounce.		N/A
	The Charge-Through VCONN-Powered USB Device shall transition to CTAttached.VPD after the state of only one of the Charge-Through port's CC1 or CC2 pins is SNK.Rp for at least tCCDebounce and VBUS on the Charge-Through port is detected.		N/A
	Note the Charge-Through Source may initiate USB PD communications which will cause brief periods of the SNK.Open state on one of the Charge-Through port's CC pins with the state of the Charge-Through port's other CC pin		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	remaining SNK.Open, but this event will not exceed tPDDebounce.		
	The Charge-Through VCONN-Powered USB Device shall transition to CTDisabled.VPD if VCONN falls below vVCONNDisconnect.		N/A
4.5.2.2.24	CTAttached.VPD State		N/A
	When in the CTAttached.VPD state, the Charge-Through VCONN-Powered USB Device has detected a Power Source on its Charge-Through port and has connected the Charge-Through port's CC and VBUS pins directly to the Host-side port's CC and VBUS pins. Hence all power delivery, negotiation and USB PD communication are performed directly between the unit on Host-side port and the Power Source connected to the Charge-Through port.		N/A
4.5.2.2.24.1	CTAttached.VPD Requirements		N/A
	Upon entry to this state, the Charge-Through VCONN-Powered USB Device shall detect which of the Charge-Through port's CC1 or CC2 pins is connected through the cable (i.e., the CC pin that is in the SNK.Rp state). The device shall then immediately, in the following order:		N/A
	1. Remove or reduce any additional capacitance on the Host-side CC port that was introduced in order to meet cReceiver as defined in USB PD to present on CC a value equal to or less than two times the maximum value for cCablePlug_CC.		N/A
	2. Disable the Rp termination advertising 3.0 A on the host port's CC pin.		N/A
	3. Passively multiplex the detected Charge-Through port's CC pin through to the host port's CC pin with an impedance of less than RccCON.		N/A
	4. Disable the Rd on the Charge-Through port's CC1 and CC2 pins.		N/A
	5. Connect the Charge-Through port's VBUS through to the host port's VBUS.		N/A
	These steps shall be completed within tVPDDetach minimum of entering this state.		N/A
	The Charge-Through VCONN-Powered USB Device shall ensure that it is powered by VCONN, does not consume more than ICCS (USB 3.2) / ICCSH (USB 2.0) from VBUS for monitoring, and is sufficiently isolated from VBUS to tolerate high voltages during Charge-Through operation.		N/A
	The Charge-Through VCONN-Powered USB Device shall not respond to any USB PD communication on any CC pin in this state. Any		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	active queries on SOP' shall have been completed prior to entering this state.		
4.5.2.2.24.2	Exiting from CTAttached.VP		N/A
	The Charge-Through VCONN-Powered USB Device shall transition to CTUnattached.VPD when VBUS falls below vSinkDisconnect and the state of the passed-through CC pin is SNK. Open for tVPDCTDD.		N/A
	The Charge-Through VCONN-Powered USB Device shall transition to CTDIsabled. VPD if VCONN falls below vVCONNDISconnect.		N/A
4.5.2.2.25	CTDisabled.VPD State		N/A
	When in the CTDIsabled.VPD state, the Charge-Through VCONN-Powered USB Device has detected the detach on its Host-side port but may still potentially be connected to a Power Source on the Charge-Through port, and is thus ensuring that the VBUS from the Power Source is removed.		N/A
4.5.2.2.25.1	CTDisabled.VPD Requirements		N/A
	The Charge-Through VCONN-Powered USB Device shall isolate its Host-side port from its Charge-Through port, including CCs and VBUS.		N/A
	The device shall present a high-impedance to ground (above zOPEN) on the Host-side port's CC pin and on the Charge-Through port CC1 and CC2 pins.		N/A
	The Charge-Through VCONN-Powered USB Device shall ensure that it is powered entirely by VBUS.		N/A
4.5.2.2.25.2	Exiting from CTDIsabled.VPD		N/A
	The Charge-Through VCONN-Powered USB Device shall transition to Unattached.SNK after tVPDDisable.		N/A
4.5.2.2.26	CTUnattached.SNK State		N/A
	When in the CTUnattached.SNK state, the port has detected that it is attached to a Charge-Through VCONN-Powered USB Device and is ready if a Power Source is attached to the Charge-Through VCONN-Powered USB Device.		N/A
	This state may also have been entered through detach of a Charge-Through Power Source.		N/A
4.5.2.2.26.1	CTUnattached.SNK Requirements		N/A
	Upon entry to this state, the port shall remove its Rp termination (if present) and terminate CC to ground through Rd.		N/A
	The port shall continue to supply VCONN.		N/A
	The port shall stop sourcing or sinking VBUS and discharge it.		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	In USB PD Version 2.0, the port shall initiate PD messages.		N/A
	The port may query the state of the attached VCONN-Powered USB Device by sending SOP' messages on USB PD to read the VPD's eMarker.		N/A
4.5.2.2.26.2	Exiting from CTUnattached.SNK		N/A
	The port shall transition to CTAttached.SNK when VBUS is detected. Note that by this point, the VCONN-Powered USB Device has already de-bounced the passed-through CC pin.		N/A
	The port shall transition to Unattached.SNK if the state of the CC pin is SNK. Open for tVPDDetach after VBUS is vSafe0V.		N/A
4.5.2.2.27	CTAttached.SNK State		N/A
	When in the CTAttached.SNK state, the port is connected to a Charge-Through VCONN-Powered USB Device, which in turn is passing through the connection to a Power Source.		N/A
4.5.2.2.27.1	CTAttached.SNK Requirements		N/A
	The port shall continue to terminate CC to ground through Rd. Since there is now a Power Source connected through to VBUS and CC, the port shall operate in one of the Sink Power Sub-States shown in Figure 4-19, and remain within the Sink Power Sub-States, until either VBUS is removed or a USB PD contract is established with the source.		N/A
	The port shall not negotiate a voltage on VBUS higher than the maximum voltage specified in the Charge-Through VCONN-Powered USB Device's Discover Identity Command response.		N/A
	The port shall continue to supply VCONN.		N/A
	The port shall reject a VCONN swap request.		N/A
	The port shall not perform USB BC 1.2 primary detection, as that will interfere with VPD functionality.		N/A
	In USB PD Version 2.0, the port shall not initiate USB PD messages, although it remains a DFP for USB data.		N/A
	The port shall neither initiate nor respond to any SOP' communication.		N/A
	The port shall meet the Sink Power Sub-State requirements specified in Section 4.5.2.2.29.		N/A
	The port shall meet the additional maximum current constraints described in Section 4.6.2.5.		N/A
	The port shall follow the restrictions on USB PD messages described in Section 4.10.2.		N/A
	The port shall alter its advertised capabilities to UFP role/sink only role as described in Section		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	4.10.2.		
4.5.2.2.27.2	Exiting from CTAttached.SNK		N/A
	A port that is not in the process of a USB PD Hard Reset shall transition to CTUnattached.SNK within tSinkDisconnect when VBUS falls below vSinkDisconnect for VBUS operating at or below 5 V or below vSinkDisconnectPD when negotiated by USB PD to operate above 5 V.		N/A
	A port that has entered into USB PD communications with the Source and has seen the CC voltage exceed vRd-USB may monitor the CC pin to detect cable disconnect in addition to monitoring VBUS.		N/A
	A port that is monitoring the CC voltage for disconnect shall transition to CTUnattached.SNK within tSinkDisconnect after the CC voltage remains below vRd-USB for tPDDebounce.		N/A
4.5.2.2.28	CTUnattached.Unsupported State		N/A
	When in the CTUnattached.Unsupported state, the Charge-Through VCONN-Powered USB Device has previously detected SNK. Open on its host port for tVPDCTDD, indicating that it is connected to a Charge-Through Capable Source, and is now monitoring its Charge-Through port for the presence of an unsupported sink.		N/A
	A Charge-Through VCONN-Powered USB Device does not support Sinks, Debug Accessory Mode, or Audio Adapter Accessory Mode.		N/A
4.5.2.2.28.1	CTUnattached.Unsupported Requirements		N/A
	The Charge-Through VCONN-Powered USB Device shall isolate its Host-side port from its Charge-Through port, including CCs and VBUS. The Charge-Through VCONN-Powered USB Device shall ensure that it is powered by VCONN, does not consume more than ICCS (USB 3.2) / ICCSH (USB 2.0) from VBUS for monitoring, and is sufficiently isolated from VBUS to tolerate high voltages during Charge-Through operation.		N/A
	Upon entry into this state, the Charge-Through VCONN-Powered USB Device shall maintain its Rp termination advertising 3.0 A on the Host-side port's CC pin, remove its Rd terminations to ground on the Charge-Through port's CC1 and CC2 pins, and provide a Rp termination advertising Default USB Power instead.		N/A
	The Charge-Through VCONN-Powered USB Device shall only respond to USB PD Discover Identity queries on SOP' on its Host-side port. It shall ensure there is sufficient capacitance on		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	the Host-side port CC to meet cReceiver as defined in USB PD.		
4.5.2.2.28.2	Exiting from CTUnattached.Unsupported		N/A
	The Charge-Through VCONN-Powered USB Device shall transition to CTAttachWait.Unsupported when a Sink connection is detected on the Charge-Through port, as indicated by the SRC.Rd state on at least one of the Charge-Through port's CC pins or SRC.Ra state on both the CC1 and CC2 pins.		N/A
	The Charge-Through VCONN-Powered USB Device shall transition to Unattached.SNK if VCONN falls below vVCONNDISCONNECT.		N/A
	Otherwise, a Charge-Through VCONN-Powered USB Device shall transition to CTUnattached.VPD within tDRPTransition after dcSRC.DRP · tDRP, or if directed.		N/A
4.5.2.2.29	CTAttachWait.Unsupported State		N/A
	The CTAttachWait.Unsupported state is used to ensure that the state of both the Charge-Through Port's CC1 and CC2 pins are stable for at least tCCDebounce.		N/A
4.5.2.2.29.1	CTAttachWait.Unsupported Requirements		N/A
	The requirements for this state are identical to CTUnattached.Unsupported state.		N/A
4.5.2.2.29.2	Exiting from CTAttachWait.Unsupported		N/A
	The Charge-Through VCONN-Powered USB Device shall transition to CTTry.SNK if the state of at least one of the Charge-Through port's CC pins is SRC.Rd, or if the state of both the CC1 and CC2 pins is SRC.Ra for at least tCCDebounce.		N/A
	The Charge-Through VCONN-Powered USB Device shall transition to CTUnattached.VPD when the state of either the Charge-Through Port's CC1 or CC2 pin is SRC.Open for at least tCCDebounce.		N/A
	The Charge-Through VCONN-Powered USB Device shall transition to Unattached.SNK if VCONN falls below vVCONNDISCONNECT.		N/A
4.5.2.2.30	CTTry.SNK State		N/A
	When in the CTTry.SNK state, the Charge-Through VCONN-Powered USB Device is querying to determine if the port partner on the Charge-Through port supports the source role.		N/A
4.5.2.2.30.1	CTTry.SNK Requirements		N/A
	The requirements for this state are identical to CTUnattached.VPD state.		N/A
4.5.2.2.30.2	Exiting from CTTry.SNK		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	The Charge-Through VCONN-Powered USB Device shall wait for tDRPTry and only then begin monitoring the Charge-Through port's CC pins for the SNK.Rp state.		N/A
	The Charge-Through VCONN-Powered USB Device shall then transition to CTAttached.VPD when the SNK.Rp state is detected on the Charge-Through port's CC pins for at least tTryCCDebounce and VBUS is detected on Charge-Through port.		N/A
	A Charge-Through VCONN-Powered USB Device shall transition to CTAttached. Unsupported if SNK.Rp state is not detected for tDRPTryWait.		N/A
	The Charge-Through VCONN-Powered USB Device shall transition to Unattached.SNK if VCONN falls below vVCONNDisconnect.		N/A
4.5.2.2.31	CTAttached.Unsupported State		N/A
	If the port partner to the Charge-Through VCONN-Powered USB Device's Charge-Through port either does not support the source power role, or failed to negotiate the source role, the CTAttached.Unsupported state is used to wait until that device is unplugged before continuing.		N/A
4.5.2.2.31.1	CTAttached.Unsupported Requirements		N/A
	The Charge-Through VCONN-Powered USB Device shall isolate its Host-side port from its Charge-Through port, including CCs and VBUS. The Charge-Through VCONN-Powered USB Device shall ensure that it is powered by VCONN, does not consume more than ICCS (USB 3.2) / ICCSH (USB 2.0) from VBUS for monitoring, and is sufficiently isolated from VBUS to tolerate high voltages during Charge-Through operation.		N/A
	Upon entry into this state, the Charge-Through VCONN-Powered USB Device shall maintain its Rp termination advertising 3.0 A on the Host-side port's CC pin, remove its Rd terminations to ground on the Charge-Through port's CC1 and CC2 pins, and provide a Rp termination advertising Default USB Power instead.		N/A
	At least one of the CC1 or CC2 pins will be in the SRC.Rd state or both will be in the SRC.Ra state. The Charge-Through port shall advertise Default USB Power (see Table 4-24) on its CC pins and monitor their voltage.		N/A
	The Charge-Through VCONN-Powered USB Device shall present a USB Billboard Device Class interface indicating that it does not recognize or support the attached accessory or device.		N/A
4.5.2.2.31.2	Exiting from CTAttached. Unsupported		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	The Charge-Through VCONN-Powered USB Device shall transition to CTUnattached.VPD when SRC. Open state is detected on both the Charge-Through port's CC pins or the SRC. Open state is detected on one CC pin and SRC.Ra is detected on the other CC pin.		N/A
4.5.2.3	Sink Power Sub-State Requirements		P
	When in the Attached.SNK or CTAttached.SNK states and the Source is supplying default VBUS, the port shall operate in one of the sub-states shown in Figure 4-19. The initial Sink Power Sub-State is PowerDefault.SNK. Subsequently, the Sink Power Sub-State is determined by Source's USB Type-C current advertisement. The port in Attached.SNK shall remain within the Sink Power Sub-States until either VBUS is removed or a USB PD contract is established with the Source.		P
	The Sink is only required to implement Sink Power Sub-State transitions if the Sink wants to consume more than default USB current.		N/A
	Note that for the CTAttached.SNK state, there are further limitations on maximum current (see Section 4.6.2.5).		N/A
4.5.2.3.1	PowerDefault.SNK Sub-State		P
	This sub-state supports Sinks consuming current within the lowest range (default) of Sourcesupplied current.		N/A
4.5.2.3.1.1	PowerDefault.SNK Requirements		P
	The port shall draw no more than the default USB power from VBUS. See Section 4.6.2.1.		P
	If the port wants to consume more than the default USB power, it shall monitor vRd to determine if more current is available from the Source.		P
4.5.2.3.1.2	Exiting from PowerDefault.SNK		P
	For any change in vRd indicating a change in allowable power, the port shall not transition until the new vRd has been stable for at least tRpValueChange.		P
	For a vRd in the vRd-1.5 range, the port shall transition to the Power1.5.SNK Sub-State.		P
	For a vRd in the vRd-3.0 range, the port shall transition to the Power3.0.SNK Sub-State.		P
4.5.2.3.2	Power1.5.SNK Sub-State		P
	This sub-state supports Sinks consuming current within the two lower ranges (default and 1.5 A) of Source-supplied current.		N/A
4.5.2.3.2.1	Power1.5.SNK Requirements		P
	The port shall draw no more than 1.5 A from		P

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Clause	Requirement + Test	Result - Remark	Verdict
	VBUS.		
	The port shall monitor vRd while it is in this sub-state.		P
4.5.2.3.2.2	Exiting from Power1.5.SNK		P
	For any change in vRd indicating a change in allowable power, the port shall not transition until the new vRd has been stable for at least tRpValueChange.		P
	For a vRd in the vRd-USB range, the port shall transition to the PowerDefault.SNK Sub-State and reduce its power consumption to the new range within tSinkAdj.		P
	For a vRd in the vRd-3.0 range, the port shall transition to the Power3.0.SNK Sub-State.		P
4.5.2.3.3	Power3.0.SNK Sub-State		P
	This sub-state supports Sinks consuming current within all three ranges (default, 1.5 A and 3.0 A) of Source-supplied current.		N/A
4.5.2.3.3.1	Power3.0.SNK Requirements		P
	The port shall draw no more than 3.0 A from VBUS.		P
	The port shall monitor vRd while it is in this sub-state.		P
4.5.2.3.3.2	Exiting from Power3.0.SNK		P
	For any change in vRd indicating a change in allowable power, the port shall not transition until the new vRd has been stable for at least tRpValueChange.		P
	For a vRd in the vRd-USB range, the port shall transition to the PowerDefault.SNK Sub-State and reduce its power consumption to the new range within tSinkAdj.		P
	For a vRd in the vRd-1.5 range, the port shall transition to the Power1.5.SNK Sub-State and reduce its power consumption to the new range within tSinkAdj.		P
4.5.2.4	Cable eMarker State Machine Requirements		N/A
4.5.2.4.1	Cable Power On State		N/A
4.5.2.4.1.1	Cable Power On State Requirements		N/A
	Each eMarker in the cable shall power on.		N/A
	The cable shall not respond to SOP' and SOP" commands in this state.		N/A
4.5.2.4.1.2	Exiting from Cable Power On State		N/A
	Each eMarker in a passive or active cable shall transition to Assign Cable SOP* when it has completed its boot process. Each eMarker shall transition to Assign Cable SOP* within tVCONNStable.		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
4.5.2.4.2	Respond to SOP'/' State		N/A
	A passive cable has only one eMarker powered at a time. This cable eMarker in a passive cable shall respond to SOP' in this state.		N/A
	Each cable eMarker in an active cable shall respond to a pre-set SOP' or SOP''. If only one eMarker exists in the cable, it shall only respond to SOP'.		N/A
	Cable designers shall ensure that the eMarker works correctly in the presence of ground and VCONN maximum IR drop.		N/A
4.5.2.4.2.1	Respond to SOP' /'' State Requirements		N/A
	Each eMarker in the passive or active cable shall be able to respond to any USB PD communication sent to its pre-set SOP' or SOP''. For a passive cable, only one eMarker should be powered at a time and shall respond to SOP' only. If two eMarkers exist in a passive or active cable and are powered at the same time, then only one shall respond to SOP' and the other shall respond to SOP''. The assignment of SOP' and SOP'' is fixed for each eMarker in a cable and shall not be dynamically set when power is applied to VCONN.		N/A
4.5.2.4.2.2	Exiting from Respond to SOP' /'' State		N/A
	Each eMarker in the cable shall transition to Cable Power On upon sensing VCONN less than vVconnDisconnect or upon a Power On Reset event.		N/A
	Each eMarker in the cable shall transition to Cable Power On upon sensing a Hard Reset or Cable Reset.		N/A
4.5.2.5	Cable Ra Management State Machine Requirements		N/A
4.5.2.5.1	Ra Applied State		N/A
	This state appears in Figure 4-22. This is the initial state at power on for each eMarker in the cable.		N/A
4.5.2.5.1.1	Ra Applied State Requirements		N/A
	Each eMarker in the cable shall apply Ra to VCONN within tRaReconnect.		N/A
4.5.2.5.1.2	Exiting from Ra Applied State		N/A
	Each eMarker in a passive or active cable shall transition to the Ra Weakened state when VCONN is greater than vVCONNDISCONNECT for tRaWeaken.		N/A
4.5.2.5.2	Ra Weakened State		N/A
4.5.2.5.2.1	Ra Weakened State Requirements		N/A
	The eMarker in the cable shall remove or weaken Ra.		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	Passive cables shall meet the Power for electronically marked passive cables defined in Table 4-6. Active cables shall meet the Power for Active Cables in Table 4-6.		N/A
4.5.2.5.2.2	Exiting from Ra Weakened State		N/A
	Each eMarker in a passive or active cable shall transition to the Ra Applied state when VCONN is below vVCONNDisconnect.		N/A
4.5.2.6	Connection States Summary		N/A
4.5.3	USB Port Interoperability Behavior		N/A
	This section describes interoperability behavior between USB Type-C to USB Type-C ports and between USB Type-C to legacy USB ports.		N/A
4.5.3.1	USB Type-C Port to USB Type-C Port Interoperability Behaviors		N/A
	The following sub-sections describe typical port-to-port interoperability behaviors for the various combinations of USB Type-C Source, Sink and DRPs as presented in Table 4-9. In all of the described behaviors, the impact of USB PD-based swaps (PR_Swap, DR_Swap or VCONN_Swap) are not considered.		N/A
	The figures in the following sections illustrate the CC1 and CC2 routing after the CC detection process is complete.		N/A
4.5.3.1.1	Source to Sink Behavior		N/A
	Figure 4-23 illustrates the functional model for a Source connected to a Sink. The single CC wire that is in a standard cable is only shown in one of the four possible connection routes, CC1 to CC1.		N/A
	The following describes the behavior when a Source is connected to a Sink.		N/A
	1. Source and Sink in the unattached state		N/A
	2. Source transitions from Unattached.SRC to Attached.SRC through AttachWait.SRC		N/A
	Source detects the Sink's pull-down on CC and enters Attached.SRC through AttachWait.SRC		N/A
	Source turns on VBUS and VCONN		N/A
	3. Sink transitions from Unattached.SNK to Attached.SNK through AttachWait.SNK. Sink may skip AttachWait.SNK if it is USB 2.0 only and does not support accessories.		N/A
	Sink detects VBUS and enters Attached.SNK through AttachWait.SNK		N/A
	4. While the Source and Sink are in the attached state:		N/A
	Source adjusts Rp as needed to limit the current the Sink may draw		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	Sink detects and monitors vRd for available current on VBUS		N/A
	Source monitors CC for detach and when detected, enters Unattached.SRC		N/A
	Sink monitors VBUS for detach and when detected, enters Unattached.SNK		N/A
4.5.3.1.2	Source to DRP Behavior		N/A
	Figure 4-24 illustrates the functional model for a Source connected to a DRP. The single CC wire that is in a standard cable is only shown in one of the four possible connection routes, CC1 to CC1.		N/A
	The following describes the behavior when a Source is connected to a DRP.		N/A
	1. Source and DRP in the unattached state		N/A
	DRP alternates between Unattached.SRC and Unattached.SNK		N/A
	2. Source transitions from Unattached.SRC to Attached.SRC through AttachWait.SRC		N/A
	Source detects the DRP's pull-down on CC and enters AttachWait.SRC. After tCCDebounce it then enters Attached.SRC.		N/A
	Source turns on VBUS and VCONN		N/A
	3. DRP transitions from Unattached.SNK to Attached.SNK through AttachWait.SNK		N/A
	DRP in Unattached.SNK detects pull up on CC and enters AttachWait.SNK. After that state persists for tCCDebounce and it detects VBUS, it enters Attached.SNK.		N/A
	4. While the Source and DRP are in their respective attached states:		N/A
	Source adjusts Rp as needed to limit the current the DRP (as Sink) may draw		N/A
	DRP (as Sink) detects and monitors vRd for available current on VBUS		N/A
	Source monitors CC for detach and when detected, enters Unattached.SRC		N/A
	DRP (as Sink) monitors VBUS for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)		N/A
4.5.3.1.3	DRP to Sink Behavior		N/A
	Figure 4-25 illustrates the functional model for a DRP connected to a Sink. The single CC wire that is in a standard cable is only shown in one of the four possible connection routes, CC1 to CC1.		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	The following describes the behavior when a DRP is connected to a Sink.		N/A
	1. DRP and Sink in the unattached state		N/A
	DRP alternates between Unattached.SRC and Unattached.SNK		N/A
	2. DRP transitions from Unattached.SRC to AttachWait.SRC to Attached.SRC		N/A
	DRP in Unattached.SRC detects one of the CC pull-downs of Sink which is in Unattached.SNK and DRP enters AttachWait.SRC		N/A
	DRP in AttachWait.SRC detects that pull down on CC persists for tCCDebounce. It then enters Attached.SRC and turns on VBUS and VCONN		N/A
	3. Sink transitions from Unattached.SNK to Attached.SNK through AttachWait.SNK if required.		N/A
	Sink detects VBUS and enters Attached.SNK		N/A
	4. While the DRP and Sink are in their respective attached states:		N/A
	DRP (as Source) adjusts Rp as needed to limit the current the Sink may draw		N/A
	Sink detects and monitors vRd for available current on VBUS		N/A
	DRP (as Source) monitors CC for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)		N/A
	Sink monitors VBUS for detach and when detected, enters Unattached.SNK		N/A
4.5.3.1.4	DRP to DRP Behavior		N/A
	Two behavior descriptions based on the connection state diagrams are provided below. In the first case, the two DRPs accept the resulting Source-to-Sink relationship achieved randomly whereas in the second case the DRP #2 chooses to drive the random result to the opposite result using the Try.SRC mechanism.		N/A
	Figure 4-26 illustrates the functional model for a DRP connected to a DRP in the first case described. The single CC wire that is in a standard cable is only shown in one of the four possible connection routes, CC1 to CC1. Port numbers have been arbitrarily assigned in the diagram to assist the reader to understand the process description.		N/A
	CASE 1: The following describes the behavior when a DRP is connected to another DRP. In this flow, the two DRPs accept the resulting Source-to-Sink relationship achieved randomly.		N/A
	1. Both DRPs in the unattached state		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	DRP #1 and DRP #2 alternate between Unattached.SRC and Unattached.SNK		N/A
	2. DRP #1 transitions from Unattached.SRC to AttachWait.SRC		N/A
	DRP #1 in Unattached.SRC detects a CC pull down of DRP #2 in Unattached.SNK and enters AttachWait.SRC		N/A
	3. DRP #2 transitions from Unattached.SNK to AttachWait.SNK		N/A
	DRP #2 in Unattached.SNK detects pull up on a CC and enters AttachWait.SNK		N/A
	4. DRP #1 transitions from AttachWait.SRC to Attached.SRC		N/A
	DRP #1 in AttachWait.SRC continues to see CC pull down of DRP #2 for tCCDebounce, enters Attached.SRC and turns on VBUS and VCONN		N/A
	5. DRP #2 transitions from AttachWait.SNK to Attached.SNK.		N/A
	DRP #2 after having been in AttachWait.SNK for tCCDebounce and having detected VBUS, enters Attached.SNK		N/A
	6. While the DRPs are in their respective attached states:		N/A
	DRP #1 (as Source) adjusts Rp as needed to limit the current DRP #2 (as Sink) may draw		N/A
	DRP #2 (as Sink) detects and monitors vRd for available current on VBUS		N/A
	DRP #1 (as Source) monitors CC for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)		N/A
	DRP #2 (as Sink) monitors VBUS for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)		N/A
	Figure 4-27 illustrates the functional model for a DRP connected to a DRP in the second case described.		N/A
	CASE 2: The following describes the behavior when a DRP is connected to another DRP. In this flow, the DRP #2 chooses to drive the random result to the opposite result using the Try.SRC mechanism.		N/A
	1. Both DRPs in the unattached state		N/A
	DRP #1 and DRP #2 alternate between Unattached.SRC and Unattached.SNK		N/A
	2. DRP #1 transitions from Unattached.SRC to AttachWait.SRC		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	DRP #1 in Unattached.SRC detects a CC pull down of DRP #2 in Unattached.SNK and enters AttachWait.SRC		N/A
	3. DRP #2 transitions from Unattached.SNK to AttachWait.SNK		N/A
	DRP #2 in Unattached.SNK detects pull up on a CC and enters AttachWait.SNK		N/A
	4. DRP #1 transitions from AttachWait.SRC to Attached.SRC		N/A
	DRP #1 in AttachWait.SRC continues to see CC pull down of DRP #2 for tCCDebounce, enters Attached.SRC and turns on VBUS and VCONN		N/A
	5. DRP #2 transitions from AttachWait.SNK to Try.SRC.		N/A
	DRP #2 in AttachWait.SNK has been in this state for tCCDebounce and detects VBUS but strongly prefers the Source role, so transitions to Try.SRC		N/A
	DRP #2 in Try.SRC asserts a pull-up on CC and waits		N/A
	6. DRP #1 transitions from Attached.SRC to Unattached.SNK to AttachWait.SNK		N/A
	DRP #1 in Attached.SRC no longer detects DRP #2's pull-down on CC and transitions to Unattached.SNK.		N/A
	DRP #1 in Unattached.SNK turns off VBUS and VCONN and applies a pull-down on CC		N/A
	DRP #1 in Unattached.SNK detects pull up on a CC and enters AttachWait.SNK		N/A
	7. DRP #2 transitions from Try.SRC to Attached.SRC		N/A
	DRP #2 in Try.SRC detects the DRP #1 in Unattached.SNK's pull-down on CC and enters Attached.SRC		N/A
	DRP #2 in Attached.SRC turns on VBUS and VCONN		N/A
	8. DRP #1 transitions from AttachWait.SNK to Attached.SNK		N/A
	DRP #1 in AttachWait.SNK after tCCDebounce and detecting VBUS, enters Attached.SNK		N/A
	9. While the DRPs are in their respective attached states:		N/A
	DRP #2 (as Source) adjusts Rp as needed to limit the current DRP #1 (as Sink) may draw		N/A
	DRP #1 (as Sink) detects and monitors vRd for available current on VBUS		N/A
	DRP #2 (as Source) monitors CC for detach and when detected, enters Unattached.SNK		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	(and resumes toggling between Unattached.SNK and Unattached.SRC)		
	DRP #1 (as Sink) monitors VBUS for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)		N/A
	CASE 3: The following describes the behavior when a DRP is connected to another DRP. In this flow, the DRP #1 chooses to drive the random result to the opposite result using the Try.SNK mechanism.		N/A
	1. Both DRPs in the unattached state		N/A
	DRP #1 and DRP #2 alternate between Unattached.SRC and Unattached.SNK		N/A
	2. DRP #1 transitions from Unattached.SRC to AttachWait.SRC		N/A
	DRP #1 in Unattached.SRC detects a CC pull down of DRP #2 in Unattached.SNK and enters AttachWait.SRC		N/A
	3. DRP #2 transitions from Unattached.SNK to AttachWait.SNK		N/A
	DRP #2 in Unattached.SNK detects pull up on a CC and enters AttachWait.SNK		N/A
	4. DRP #1 transitions from AttachWait.SRC to Try.SNK		N/A
	DRP #1 in AttachWait.SRC has been in this state for tCCDebounce and detects DRP #2's pull-down on CC but strongly prefers the Sink role, so transitions to Try.SNK		N/A
	DRP #1 in Try.SNK asserts a pull down on CC and waits		N/A
	5. DRP #2 transitions from AttachWait.SNK to Unattached.SRC to AttachWait.SRC.		N/A
	DRP #2 in AttachWait.SNK no longer detects DRP #1's pull up on CC and transitions to Unattached.SRC		N/A
	DRP #2 in Unattached.SRC applies a pull up on CC		N/A
	DRP #2 in Unattached.SRC detects a pull down on a CC pin and enters AttachWait.SRC		N/A
	DRP #1 detects DRP #2's pull up on CC and remains in Try.SNK		N/A
	6. DRP #2 transitions from AttachWait.SRC to Attached.SRC		N/A
	DRP #2 in AttachWait.SRC times out (tCCDebounce) and transitions to Attached.SRC		N/A
	DRP #2 in Attached.SRC turns on VBUS and VCONN		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	7. DRP #1 transitions from Try.SNK to Attached.SNK		N/A
	DRP #1 in Try.SNK after detecting VBUS, enters Attached.SNK		N/A
	8. While the DRPs are in their respective attached states:		N/A
	DRP #2 (as Source) adjusts Rp as needed to limit the current DRP #1 (as Sink) may draw		N/A
	DRP #1 (as Sink) detects and monitors vRd for available current on VBUS		N/A
	DRP #2 (as Source) monitors CC for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)		N/A
	DRP #1 (as Sink) monitors VBUS for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)		N/A
4.5.3.1.5	Source to Source Behavior		N/A
	Figure 4-28 illustrates the functional model for a Source connected to a Source. The single CC wire that is in a standard cable is only shown in one of the four possible connection routes, CC1 to CC1. Port numbers have been arbitrarily assigned in the diagram to assist the reader to understand the process description.		N/A
	The following describes the behavior when a Source is connected to another Source.		N/A
	1. Both Sources in the unattached state		N/A
	Source #1 fails to detect a Sink's pull-down on CC and remains in Unattached.SRC		N/A
	Source #2 fails to detect a Sink's pull-down on CC and remains in Unattached.SRC		N/A
4.5.3.1.6	Sink to Sink Behavior		N/A
	Figure 4-29 illustrates the functional model for a Sink connected to a Sink. The single CC wire that is in a standard cable is only shown in one of the four possible connection routes, CC1 to CC1. Port numbers have been arbitrarily assigned in the diagram to assist the reader to understand the process description.		N/A
	The following describes the behavior when a Sink is connected to another Sink.		N/A
	1. Both Sinks in the unattached state		N/A
	Sink #1 fails to detect pull up on CC or VBUS supplied by a Source and remains in Unattached.SNK		N/A
	Sink #2 fails to detect pull up on CC or VBUS supplied by a Source and remains in Unattached.SNK		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
4.5.3.1.7	DRP to VCONN-Powered USB Device (VPD) Behavior		N/A
	Figure 4-30 illustrates the functional model for a DRP connected to a VCONN-Powered USB Device that does not feature charge-through functionality.		N/A
	The following describes the behavior when a DRP that supports VPDs is connected to a VPD.		N/A
	1. DRP and VPD in the unattached state		N/A
	DRP alternates between Unattached.SRC and Unattached.SNK		N/A
	2. DRP transitions from Unattached.SRC to Attached.SRC through AttachWait.SRC		N/A
	DRP in Unattached.SRC detects the CC pull-down of VPD which is in Unattached.SNK and DRP enters AttachWait.SRC		N/A
	DRP in AttachWait.SRC detects that pull-down on CC persists for tCCDebounce. It then enters Attached.SRC and turns on VBUS and VCONN		N/A
	3. VPD transitions from Unattached.SNK to Attached.SNK through AttachWait.SNK		N/A
	VPD detects VCONN and enters Attached.SNK		N/A
	4. While DRP and VPD are in their respective attached states, DRP discovers the VPD and removes VBUS		N/A
	DRP (as Source) queries the cable identity via USB PD on SOP'.		N/A
	VPD responds on SOP', advertising that it is a VCONN-Powered USB Device that does not support charge-through		N/A
	DRP (as Source) removes VBUS		N/A
	DRP (as Source) maintains its Rp		N/A
	5. DRP and VPD for detach		N/A
	DRP (as Source) monitors CC for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)		N/A
	VPD monitors VCONN for detach and when detected, enters Unattached.SNK		N/A
4.5.3.1.8	DRP to Charge-Through VCONN-Powered USB Device (CTVPD) Behavior		N/A
	Figure 4-31 illustrates the functional model for a DRP connected to a Charge-Through VCONNPowered USB Device, with a Source attached to the Charge-Through port on the VCONNPowered USB Device.		N/A
	CASE 1: The following describes the behavior when a DRP is connected to a Charge-Through		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	VCONN-Powered USB Device (abbreviated CTVPD), with no Power Source attached to the Charge-Through port on the CTVPD.		
	1. DRP and CTVPD are both in the unattached state		N/A
	a. DRP alternates between Unattached.SRC and Unattached.SNK		N/A
	b. CTVPD has applied Rd on its Charge-Through port's CC1 and CC2 pins and Rd on the Host-side port's CC pin		N/A
	2. DRP transitions from Unattached.SRC to Attached.SRC through AttachWait.SRC		N/A
	a. DRP in Unattached.SRC detects a CC pull down of CTVPD which is in Unattached.SNK and DRP enters AttachWait.SRC		N/A
	b. DRP in AttachWait.SRC detects that pull down on CC persists for tCCDebounce, enters Attached.SRC and turns on VBUS and VCONN		N/A
	3. CTVPD transitions from Unattached.SNK to Attached.SNK through AttachWait.SNK		N/A
	a. CTVPD detects the host-side CC pull-up of the DRP and CTVPD enters AttachWait.SNK		N/A
	b. CTVPD in AttachWait.SNK detects that pull up on the Host-side port's CC persists for tCCDebounce, VCONN present and enters Attached.SNK		N/A
	c. CTVPD present a high-impedance to ground (above zOPEN) on its Charge-Through port's CC1 and CC2 pins		N/A
	4. While DRP and CTVPD are in their respective attached states, DRP discovers the CTVPD and transitions to CTUnattached.SNK		N/A
	a. DRP (as Source) queries the device identity via USB PD (Device Identity Command) on SOP'		N/A
	b. CTVPD responds on SOP', advertising that it is a Charge-Through VCONN Powered USB Device		N/A
	c. DRP (as Source) removes VBUS		N/A
	d. DRP (as Source) changes its Rp to a Rd		N/A
	e. DRP (as Sink) continues to provide VCONN and enters CTUnattached.SNK		N/A
	5. CTVPD transitions to CTUnattached.VPD		N/A
	a. CTVPD detects VBUS removal, VCONN presence, the low Host-side CC pin and enters CTUnattached.VPD		N/A
	b. CTVPD changes its host-side Rd to a Rp advertising 3.0 A		N/A
	c. CTVPD isolates itself from VBUS		N/A
	d. CTVPD apply Rd on its Charge-Through		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	port's CC1 and CC2 pins		
	6. While the CTVPD in CTUnattached.VPD state and the DRP in CTUnattached.SNK state:		N/A
	a. CTVPD monitors Charge-Through CC pins for a source or sink; when a Power Source attach is detected, enters CTAttachWait.VPD; when a sink is detected, enters CTAttachWait.Unsupported		N/A
	b. CTVPD monitors VCONN for Host detach and when detected, enters Unattached.SNK		N/A
	c. DRP monitors VBUS and CC for CTVPD detach for tVPDDetach and when detected, enters Unattached.SNK		N/A
	d. DRP monitors VBUS for Power Source attach and when detected, enters CTAttached.SNK		N/A
	CASE 2: The following describes the behavior when a Power Source is connected to a Charge-Through VCONN-Powered USB Device (abbreviated CTVPD), with a Host already attached to the Host-side port on the CTVPD.		N/A
	1. DRP is in CTUnattached.SNK state, CTVPD in CTUnattached.VPD, and Power Source in the unattached state		N/A
	a. CTVPD has applied Rd on the Charge-Through port's CC1 and CC2 pins and Rp termination advertising 3.0 A on the Host-side port's CC pin		N/A
	2. Power Source transitions from Unattached.SRC to Attached.SRC through AttachWait.SRC		N/A
	a. Power Source detects the CC pull-down of the CTVPD and enters AttachWait.SRC		N/A
	b. Power Source in AttachWait.SRC detects that pull down on CC persists for tCCDebounce, enters Attached.SRC and turns on VBUS		N/A
	3. CTVPD transitions from CTUnattached.VPD through CTAttachWait.VPD to CTAttached.VPD		N/A
	a. CTVPD detects the Source's Rp on one of its Charge-Through CC pins, and transitions to CTAttachWait.VPD		N/A
	b. CTVPD finishes any active USB PD communication on SOP' and ceases to respond to SOP' queries		N/A
	c. CTVPD in CTAttachWait.VPD detects that the pull up on Charge-Through CC pin persists for tCCDebounce, detects VBUS and enters CTAttached.VPD		N/A
	d. CTVPD connects the active Charge-Through CC pin to the Host-side port's CC pin		N/A
	e. CTVPD disables its Rp termination advertising 3.0 A on the Host-side port's CC pin		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	f. CTVPD disables its Rd on the Charge-Through CC pins		N/A
	g. CTVPD connects VBUS from the Charge-Through side to the Host side		N/A
	4. DRP (as Sink) transitions to CTAttached.SNK		N/A
	a. DRP (as Sink) detects VBUS, monitors vRd for available current and enter CTAttached.SNK		N/A
	5. While the devices are all in their respective attached states:		N/A
	a. CTVPD monitors VCONN for DRP detach and when detected, enters CTDisabled.VPD		N/A
	b. CTVPD monitors VBUS and CC for Power Source detach and when detected, enters CTUnattached.VPD within tVPDCTDD		N/A
	c. DRP (as Sink) monitors VBUS for Charge-Through Power Source detach and when detected, enters CTUnattached.SNK		N/A
	d. DRP (as Sink) monitors VBUS and CC for CTVPD detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)		N/A
	e. Power Source monitors CC for CTVPD detach and when detected, enters Unattached.SRC		N/A
	CASE 3: The following describes the behavior when a Power Source is connected to a Charge-Through VCONN-Powered USB Device (abbreviated CTVPD), with no Host attached to the Host-side port on the CTVPD.		N/A
	1. CTVPD and Power Source are both in the unattached state		N/A
	a. CTVPD has applied Rd on the Charge-Through port's CC1 and CC2 pins and Rd on the Host-side port's CC pin		N/A
	2. Power Source transitions from Unattached.SRC to Attached.SRC through AttachWait.SRC		N/A
	a. Power Source detects the CC pull-down of the CTVPD and enters AttachWait.SRC		N/A
	b. Power Source in AttachWait.SRC detects that pull down on CC persists for tCCDebounce, enters Attached.SRC and turns on VBUS		N/A
	3. CTVPD alternates between Unattached.SNK and Unattached.SRC		N/A
	a. CTVPD detects the Source's Rp on one of its Charge-Through CC pins, detects VBUS for tCCDebounce and starts alternating between Unattached.SRC and Unattached.SNK		N/A
	4. While the CTVPD alternates between		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	Unattached.SRC and Unattached.SNK state and the Power Source in Attached.SRC state:		
	a. CTVPD monitors the Host-side port's CC pin for device attach and when detected, enters AttachWait.SRC		N/A
	b. CTVPD monitors VBUS for Power Source detach and when detected, enters Unattached.SNK		N/A
	c. Power Source monitors CC for CTVPD detach and when detected, enters Unattached.SRC		N/A
	CASE 4: The following describes the behavior when a DRP is connected to a Charge-Through VCONN-Powered USB Device (abbreviated CTVPD), with a Power Source already attached to the Charge-Through side on the CTVPD.		N/A
	1. DRP and CTVPD are in unattached state and Power Source in Attached.SRC state		N/A
	a. DRP alternates between Unattached.SRC and Unattached.SNK		N/A
	b. CTVPD alternates between Unattached.SRC and Unattached.SNK		N/A
	c. CTVPD has applied Rd on its Charge-Through port's CC1 and CC2 pins		N/A
	d. Power Source has applied VBUS		N/A
	2. DRP transitions from Unattached.SNK to AttachWait.SNK		N/A
	a. DRP in Unattached.SNK detects the CC pull-up of CTVPD which is in Unattached.SRC and DRP enters AttachWait.SNK		N/A
	3. CTVPD transitions from Unattached.SRC to Try.SNK through AttachWait.SRC		N/A
	a. CTVPD in Unattached.SRC detects the CC pull-down of DRP which is in Unattached.SNK and CTVPD enters AttachWait.SRC		N/A
	b. CTVPD in AttachWait.SRC detects that pull down on CC persists for tCCDebounce and enters Try.SNK		N/A
	c. CTVPD disables Rp termination advertising Default USB Power on the Hostside port's CC pin		N/A
	d. CTVPD enables Rd on the Host-side port's CC pin		N/A
	4. DRP transitions from AttachWait.SNK to Attached.SRC through Unattached.SRC and AttachWait.SRC		N/A
	a. DRP in AttachWait.SNK detects the CC pull-up removal of CTVPD which is in Try.SNK and DRP enters Unattached.SRC		N/A
	b. DRP in Unattached.SRC detects the CC pull-down of CTVPD which is in Try.SNK and DRP		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	enters AttachWait.SRC		
	c. DRP in AttachWait.SRC detects that pull down on CC persists for tCCDebounce. It then enters Attached.SRC and enable VBUS and VCONN		N/A
	5. CTVPD transitions from Try.SNK to Attached.SNK		N/A
	a. CTVPD detects the CC pull-up of the DRP persists for tTryCCDebounce		N/A
	b. CTVPD detects VBUS on the Host-side port and enters Attached.SNK		N/A
	6. While DRP and CTVPD are in their respective attached states, DRP discovers the Charge-Through CTVPD and transitions to CTUnattached.SNK		N/A
	a. DRP (as Source) queries the device identity via USB PD (Discover Identity Command) on SOP'		N/A
	b. CTVPD responds on SOP', advertising that it is a Charge-Through VCONNPowered USB Device		N/A
	c. DRP (as Source) removes VBUS		N/A
	d. DRP (as Source) changes its Rp into an Rd		N/A
	e. DRP (as Sink) continues to provide VCONN and enters CTUnattached.SNK		N/A
	7. CTVPD transitions to CTUnattached.VPD		N/A
	a. CTVPD detects VBUS removal, VCONN presence, and the low CC pin on its host port and enters CTUnattached.VPD		N/A
	b. CTVPD changes its host-side Rd into an Rp termination advertising 3.0 A		N/A
	c. CTVPD isolates itself from VBUS		N/A
	8. CTVPD transitions from CTUnattached.VPD through CTAttachWait.VPD to CTAttached.VPD		N/A
	a. CTVPD detects the Source's Rp on one of its Charge-Through CC pins, and transitions to CTAttachWait.VPD		N/A
	b. CTVPD in CTAttachWait.VPD detects that the pull up on Charge-Through CC pin persists for tCCDebounce, detects VBUS and enters CTAttached.VPD		N/A
	c. CTVPD finishes any active USB PD communication on SOP' and ceases to respond to SOP' queries		N/A
	d. CTVPD connects the active Charge-Through CC pin to the Host-side port's CC pin		N/A
	e. CTVPD disables its Rp termination advertising 3.0 A on the Host-side port's CC pin		N/A
	f. CTVPD disables its Rd on the Charge-Through CC pins		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	g. CTVPD connects VBUS from the Charge-Through side to the Host side		N/A
	9. DRP (as Sink) transitions to CTAttached.SNK		N/A
	a. DRP (as Sink) detects VBUS and monitors vRd for available current and enter CTAttached.SNK		N/A
	10. While the devices are all in their respective attached states:		N/A
	a. CTVPD monitors VCONN for DRP detach and when detected, enters CTDisabled.VPD		N/A
	b. CTVPD monitors VBUS and CC for Power Source detach and when detected, enters CTUnattached.VPD within tVPDCTDD		N/A
	c. DRP (as Sink) monitors VBUS for Charge-Through Power Source detach and when detected, enters CTUnattached.SNK		N/A
	d. DRP (as Sink) monitors VBUS and CC for CTVPD detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)		N/A
	e. Power Source monitors CC for CTVPD detach and when detected, enters Unattached.SRC		N/A
	CASE 5: The following describes the behavior when a Power Source is connected to a Charge-Through VCONN-Powered USB Device (abbreviated CTVPD), with a DRP (with dead battery) attached to the Host-side port on the CTVPD.		N/A
	1. DRP, CTVPD and Power Source are all in the unattached state		N/A
	a. DRP apply dead battery Rd		N/A
	b. CTVPD apply Rd on the Charge-Through port's CC1 and CC2 pins and Rd on the Host-side port's CC pin		N/A
	2. Power Source transitions from Unattached.SRC to Attached.SRC through AttachWait.SRC		N/A
	a. Power Source detects the CC pull-down of the CTVPD and enters AttachWait.SRC		N/A
	b. Power Source in AttachWait.SRC detects that pull down on CC persists for tCCDebounce, enters Attached.SRC and turns on VBUS		N/A
	3. CTVPD alternates between Unattached.SNK and Unattached.SRC		N/A
	a. CTVPD detects the Source's Rp on one of its Charge-Through CC pins, detects VBUS for tCCDebounce and starts alternating between Unattached.SRC and Unattached.SNK		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	4. CTVPD transitions from Unattached.SRC to Try.SNK through AttachWait.SRC		N/A
	a. CTVPD in Unattached.SRC detects the CC pull-down of DRP which is in Unattached.SNK and CTVPD enters AttachWait.SRC		N/A
	b. CTVPD in AttachWait.SRC detects that pull down on CC persists for tCCDebounce and enters Try.SNK		N/A
	d. CTVPD enables Rd on the Host-side port's CC pin		N/A
	5. DRP in dead battery condition remains in Unattached.SNK		N/A
	6. CTVPD transitions from Try.SNK to Attached.SRC through TryWait.SRC		N/A
	a. CTVPD didn't detect the CC pull-up of the DRP for tTryCCDebounce after tDRPTry and enters TryWait.SRC		N/A
	b. CTVPD disables Rp on the Host-side port's CC pin		N/A
	c. CTVPD enables Rp termination advertising Default USB Power on the Hostside port's CC pin		N/A
	d. CTVPD detects the CC pull-down of the DRP for tTryCCDebounce and enters Attached.SRC		N/A
	e. CTVPD connects VBUS from the Charge-Through side to the Host side		N/A
	7. DRP transitions from Unattached.SNK to Attached.SNK through AttachWait.SNK		N/A
	a. DRP in Unattached.SNK detects the CC pull-up of CTVPD which is in Attached.SRC and DRP enters AttachWait.SNK		N/A
	b. DRP in AttachWait.SNK detects that pull up on CC persists for tCCDebounce, VBUS present and enters Attached.SNK		N/A
	8. While the devices are all in their respective attached states:		N/A
	a. CTVPD monitors the Host-side port's CC pin for device attach and when detected, enters Unattached.SNK		N/A
	b. CTVPD monitors VBUS for Power Source detach and when detected, enters Unattached.SNK		N/A
	c. Power Source monitors CC for CTVPD detach and when detected, enters Unattached.SRC		N/A
	d. DRP monitors VBUS for CTVPD detach and when detected, enters Unattached.SNK		N/A
	e. Additionally, the DRP may query the identity of the cable via USB PD on SOP' when it has sufficient battery power and when a Charge-Through VPD is identified enters TryWait.SRC		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	if implemented, or enters Unattached.SRC if TryWait.SRC is not supported		
	CASE 6: The following describes the behavior when a DRP is connected to a Charge-Through VCONN-Powered USB Device (abbreviated CTVPD) and a Sink is attached to the Charge-Through port on the CTVPD.		N/A
	1. DRP, CTVPD and Sink are all in the unattached state		N/A
	a. DRP alternates between Unattached.SRC and Unattached.SNK		N/A
	b. CTVPD has applied Rd on its Charge-Through port's CC1 and CC2 pins and Rd on the Host-side port's CC pin		N/A
	2. DRP transitions from Unattached.SRC to Attached.SRC through AttachWait.SRC		N/A
	a. DRP in Unattached.SRC detects the CC pull-down of CTVPD which is in Unattached.SNK and DRP enters AttachWait.SRC		N/A
	b. DRP in AttachWait.SRC detects that pull down on CC persists for tCCDebounce. It then enters Attached.SRC and enable VBUS and VCONN		N/A
	3. CTVPD transitions from Unattached.SNK to Attached.SNK through AttachWait.SNK		N/A
	a. CTVPD detects the host-side CC pull-up of the DRP and CTVPD enters AttachWait.SNK		N/A
	b. CTVPD in AttachWait.SNK detects that pull up on the Host-side port's CC persists for tCCDebounce, VCONN present and enters Attached.SNK		N/A
	c. CTVPD present a high-impedance to ground (above zOPEN) on its Charge-Through port's CC1 and CC2 pins		N/A
	4. While DRP and CTVPD are in their respective attached states, DRP discovers the Charge-Through CTVPD and transitions to CTUnattached.SNK		N/A
	a. DRP (as Source) queries the device identity via USB PD (Discover Identity Command) on SOP'		N/A
	b. CTVPD responds on SOP', advertising that it is a Charge-Through VCONNPowered USB Device		N/A
	c. DRP (as Source) removes VBUS		N/A
	d. DRP (as Source) changes its Rp into an Rd		N/A
	e. DRP (as Sink) continues to provide VCONN and enters CTUnattached.SNK		N/A
	5. CTVPD transitions to CTUnattached.VPD		N/A
	a. CTVPD detects VBUS removal, VCONN presence, and the low CC pin on its host port		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	and enters CTUnattached.VPD		
	b. CTVPD changes its host-side Rd into an Rp termination advertising 3.0 A		N/A
	c. CTVPD isolates itself from VBUS		N/A
	d. CTVPD apply Rd on its Charge-Through port's CC1 and CC2 pins		N/A
	6. CTVPD alternates between CTUnattached.VPD and CTUnattached.Unsupported		N/A
	a. CTVPD detects SRC.Open on its Charge-Through CC pins and starts alternating between CTUnattached.VPD and CTUnattached.Unsupported		N/A
	7. CTVPD transitions from CTUnattached.Unsupported to CTTry.SNK through CTAttachWait.Unsupported		N/A
	a. CTVPD in CTUnattached.Unsupported detects the CC pull-down of the Sink which is in Unattached.SNK and CTVPD enters CTAttachWait.Unsupported		N/A
	b. CTVPD in CTAttachWait.Unsupported detects that pull down on CC persists for tCCDebounce and enters CTTry.SNK		N/A
	c. CTVPD disables Rp termination advertising Default USB Power on the Charge-Through port's CC pins		N/A
	d. CTVPD enables Rd on the Charge-Through port's CC pins		N/A
	8. CTVPD transitions from CTTry.SNK to CTAttached.Unsupported		N/A
	a. CTVPD didn't detect the CC pull-up of the potential Source for tDRPTryWait after tDRPTry and enters CTAttached.Unsupported		N/A
	9. While the CTVPD in CTAttached.Unsupported state, the DRP in CTUnattached.SNK state and the Sink in Unattached.SNK state:		N/A
	a. CTVPD disables the Rd termination on the Charge-Through port's CC pins and applies Rp termination advertising Default USB Power		N/A
	b. CTVPD exposes a USB Billboard Device Class to the DRP indicating that it is connected to an unsupported device on its Charge Through port		N/A
	c. CTVPD monitors Charge-Through CC pins for Sink detach and when detected, enters CTUnattached.VPD		N/A
	d. CTVPD monitors VCONN for Host detach and when detected, enters Unattached.SNK		N/A
	e. DRP monitors CC for CTVPD detach for tVPDDetach and when detected, enters Unattached.SNK		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	f. DRP monitors VBUS for CTVPD Charge-Through source attach and, when detected, enters CTAttached.SNK		N/A
4.5.3.2	USB Type-C port to Legacy Port Interoperability Behaviors		N/A
	The following sub-sections describe port-to-port interoperability behaviors for the various combinations of USB Type-C Source, Sink and DRPs and legacy USB ports.		N/A
4.5.3.2.1	Source to Legacy Device Port Behavior		N/A
	Figure 4-32 illustrates the functional model for a Source connected to a legacy device port. This model is based on having an adapter present as a Sink to the Source. This adapter has a USB Type-C plug on one end plugged into the Source and either a USB Standard-B plug, USB Micro-B plug, USB Mini-B plug, or a USB Standard-A receptacle on the other end.		N/A
	The following describes the behavior when a Source is connected to a legacy device adapter that has an Rd to ground so as to mimic the behavior of a Sink.		N/A
	1. Source in the unattached state		N/A
	2. Source transitions from Unattached.SRC to Attached.SRC through AttachWait.SRC		N/A
	Source detects the Sink's pull-down on CC and enters AttachWait.SRC. After tCCDebounce, it enters Attached.SRC.		N/A
	Source turns on VBUS and VCONN		N/A
	3. While the Source is in the attached state:		N/A
	Source monitors CC for detach and when detected, enters Unattached.SRC		N/A
4.5.3.2.2	Legacy Host Port to Sink Behavior		N/A
	Figure 4-33 illustrates the functional model for a legacy host port connected to a Sink. This model is based on having an adapter that presents itself as a Source to the Sink, this adapter is either a USB Standard-A legacy plug or a USB Micro-B legacy receptacle on one end and the USB Type-C plug on the other end plugged into a Sink.		N/A
	The following describes the behavior when a legacy host adapter that has an Rp to VBUS so as to mimic the behavior of a Source that is connected to a Sink. The value of Rp shall indicate an advertisement of Default USB Power (See Table 4-24), even though the cable itself can carry 3 A. This is because the cable has no knowledge of the capabilities of the power source, and any higher current is negotiated via USB BC 1.2.		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	1. Sink in the unattached state		N/A
	2. Sink transitions from Unattached.SNK to Attached.SNK through AttachWait.SNK if needed.		N/A
	While in Unattached.SNK, if device is not USB 2.0 only, supports accessories or requires more than default power, it enters AttachWait.SNK when it detects a pull up on CC and ignores VBUS. Otherwise, it may enter Attached.SNK directly when VBUS is detected.		N/A
	Sink detects VBUS and enters Attached.SNK		N/A
	3. While the Sink is in the attached state:		N/A
	Sink monitors VBUS for detach and when detected, enters Unattached.SNK		N/A
4.5.3.2.3	DRP to Legacy Device Port Behavior		N/A
	Figure 4-34 illustrates the functional model for a DRP connected to a legacy device port. This model is based on having an adapter present as a Sink (Device) to the DRP. This adapter has a USB Type-C plug on one end plugged into a DRP and either a USB Standard-B plug, USB Micro-B plug, USB Mini-B plug, or a USB Standard-A receptacle on the other end.		N/A
	The following describes the behavior when a DRP is connected to a legacy device adapter that has an Rd to ground so as to mimic the behavior of a Sink.		N/A
	1. DRP in the unattached state		N/A
	DRP alternates between Unattached.SRC and Unattached.SNK		N/A
	2. DRP transitions from Unattached.SRC to Attached.SRC		N/A
	DRP in Unattached.SRC detects the adapter's pull-down on CC and enters AttachWait.SRC		N/A
	DRP in AttachWait.SRC times out (tCCDebounce) and transitions to Attached.SRC		N/A
	DRP in Attached.SRC turns on VBUS and VCONN		N/A
	DRP in AttachWait.SRC may support Try.SNK and if so, may transition through Try.SNK and TryWait.SRC prior to entering Attached.SRC		N/A
	3. While the DRP is in the attached state:		N/A
	DRP monitors CC for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)		N/A
4.5.3.2.4	Legacy Host Port to DRP Behavior		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	Figure 4-35 illustrates the functional model for a legacy host port connected to a DRP operating as a Sink. This model is based on having an adapter that presents itself as a Source (Host) to the DRP operating as a Sink, this adapter is either a USB Standard-A legacy plug or a USB Micro-B legacy receptacle on one end and the USB Type-C plug on the other end plugged into a DRP.		N/A
	The following describes the behavior when a legacy host adapter that has an Rp to VBUS so as to mimic the behavior of a Source is connected to a DRP. The value of Rp shall indicate an advertisement of Default USB Power (See Table 4-24), even though the cable itself can carry 3 A. This is because the cable has no knowledge of the capabilities of the power source, and any higher current is negotiated via USB BC 1.2.		N/A
	1. DRP in the unattached state		N/A
	DRP alternates between Unattached.SRC and Unattached.SNK		N/A
	2. DRP transitions from Unattached.SNK to AttachWait.SNK to Attached.SNK		N/A
	DRP in Unattached.SNK detects pull up on CC and enters AttachWait.SNK.		N/A
	DRP in AttachWait.SNK detects VBUS and enters Attached.SNK		N/A
	DRP in AttachWait.SNK may support Try.SRC and if so, may transition through Try.SRC and TryWait.SNK prior to entering Attached.SNK		N/A
	3. While the DRP is in the attached state:		N/A
	DRP monitors VBUS for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)		N/A
4.6	Power		P
	Power delivery over the USB Type-C connector takes advantage of the existing USB methods as defined by: the USB 2.0 and USB 3.2 specifications, the USB BC 1.2 specification and the USB Power Delivery specification. Power for USB4 operation requires a USB PD explicit contract as defined in Section 5.3 and the USB Power Delivery specification. Prior to entering a USB PD explicit contract, a USB4 port operates as a USB 3.2 port regarding power.		N/A
	The USB Type-C Current mechanism allows the Source to offer more current than defined by the USB BC 1.2 specification. A USB power source shall not provide more than 20 V		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	nominal on VBUS. USB PD power sources that deliver power over a USB Type-C connector shall follow the power rules as defined in Section 10 of the USB Power Delivery specification.		
	All USB Type-C-based devices shall support USB Type-C Current and may support other USB-defined methods for power. The following order of precedence of power negotiation shall be followed: USB BC 1.2 supersedes the USB 2.0 and USB 3.2 specifications, USB Type-C Current at 1.5 A and 3.0 A supersedes USB BC 1.2, and USB Power Delivery supersedes USB Type-C Current. Table 4-17 summarizes this order of precedence of power source usage.		P
	For example, once the PD mode (e.g. a power contract has been negotiated) has been entered, the device shall abide by that power contract ignoring any other previously made or offered by the USB Type-C Current, USB BC 1.2 or USB 2.0 and USB 3.2 specifications. When the PD mode is exited, the device shall fallback in order to the USB Type-C Current, USB BC 1.2 or USB 2.0 and USB 3.2 specification power levels.		P
	All USB Type-C ports shall tolerate being connected to USB power source supplying default USB power, e.g. a host being connected to a legacy USB charger that always supplies VBUS.		N/A
4.6.1	Power Requirements during USB Suspend		P
	USB Type-C implementations with USB Type-C Current, USB PD and VCONN, along with active cables, requires the need to expand the traditional USB suspend definition.		N/A
4.6.1.1	VBUS Requirements during USB Suspend		P
	The USB 2.0 and USB 3.2 specifications define the amount of current a Sink is allowed to consume during suspend.		N/A
	USB suspend power rules shall apply when the USB Type-C Current is at the Default USB Power level or when USB PD is being used and the Suspend bit is set appropriately.		P
	When USB Type-C Current is set at 1.5 A or 3.0 A, the Sink is allowed to continue to draw current from VBUS during USB suspend. During USB suspend, the Sink's requirement to track and meet the USB Type-C Current advertisement remains in force (See Section 4.5.2.3).		N/A
	USB PD provides a method for the Source to communicate to the Sink whether or not the Sink has to follow the USB power rules for suspend.		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
4.6.1.2	VCONN Requirements during USB Suspend		N/A
	If the Source supplies VBUS power during USB suspend, it shall also supply VCONN and meet the requirements defined in Table 4-5.		N/A
	Electronically Marked Cables shall meet the requirements in Table 4-6 during USB suspend.		N/A
	VCONN powered accessories shall meet the requirements defined in Table 4-7 during USB suspend.		N/A
4.6.2	VBUS Power Provided Over a USB Type-C Cable		P
	The minimum requirement for VBUS power supplied over the USB Type-C cable assembly matches the existing requirement for VBUS supplied over existing legacy USB cable assemblies.		N/A
	USB Power Delivery in Standard Power Range (SPR) operation is intended to work over unmodified USB Type-C to USB Type-C cables, therefore any USB Type-C cable assembly that incorporates electrical components or electronics shall ensure that it tolerate, or be protected from, a VBUS voltage of 21 V.		N/A
	USB Power Delivery in Extended Power Range (EPR) operation requires EPR-compatible USB Type-C to USB Type-C cables. Any USB Type-C cable assembly that incorporates electrical components or electronics that may be powered by VBUS shall ensure that it can functionally tolerate, or be protected from, a VBUS voltage of up to 53.65 V (51 V + 5% + 100mV).		N/A
4.6.2.1	USB Type-C Current		P
	Default USB voltage and current are defined by the USB 2.0 and USB 3.2 specifications. All USB Type-C Current advertisements are at the USB VBUS voltage defined by these specifications.		N/A
	The USB Type-C Current feature provides the following extensions:		N/A
	Higher current than defined by the USB 2.0, the USB 3.2 or the BC 1.2 specifications		N/A
	Allows the power source to manage the current it provides		N/A
	The USB Type-C connector uses CC pins for configuration including an ability for a Source to advertise to its port partner (Sink) the amount of current it shall supply:		N/A
	Default is the as-configured for high-power operation current value as defined by the USB Specification (500 mA for USB 2.0 ports; 900		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	mA or 1,500 mA for USB 3.2 ports in single-lane or dual-lane operation, respectively)		
	1.5 A		N/A
	3.0 A		N/A
	When a Source is advertising USB Type-C Default current, the Sink behavior is defined as follows:		N/A
	It connects as a USB 2.0 or USB 3.2 device, after which the Sink shall follow the appropriate USB specification.		N/A
	It enters a USB PD contract, after which the Sink shall follow the USB PD specification to determine the current (e.g., Rp will no longer be Default as it is superseded by the USB PD contract).		N/A
	It detects a USB BC 1.2 charging port, after which the Sink shall follow the USB BC 1.2 specification.		N/A
	It attaches as a USB Type-C Power Sinking Device (PSD), after which the Sink may draw up to 500 mA and shall meet the inrush requirement for USB 2.0.		N/A
	A PSD shall fully support USB Type-C Current operation, should support USB PD and may support USB BC 1.2. A PSD may be a Sink or a DRP operating in Sink mode. A PSD shall not have a USB or USB Type-C Alternate Mode communications function.		N/A
	The relationship of USB Type-C Current and the equivalent USB PD Power (PDP) value is shown in Table 4-18.		N/A
	A Sink that takes advantage of the additional current offered (e.g., 1.5 A or 3.0 A) shall monitor the CC pins and shall adjust its current consumption within tSinkAdj to remain within the value advertised by the Source. While a USB PD contract is in place, a Sink is not required to monitor USB Type-C current advertisements and shall not respond to USB Type-C current advertisements.		P
	The Source shall supply VBUS to the Sink within tVBUSON. VBUS shall be in the specified voltage range at the advertised current.		P
	A Source (port supplying VBUS) shall protect itself from a Sink that draws current in excess of the port's USB Type-C Current advertisement.		N/A
	The Source adjusts Rp (or current source) to advertise which of the three current levels it supports. See Table 4-24 for the termination requirements for the Source to advertise currents.		N/A
	The value of Rp establishes a voltage (vRd) on CC that is used by the Sink to determine the		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	maximum current it may draw.		
	Table 4-35 defines the CC voltage range observed by the Sink that only support default USB current.		N/A
	If the Sink wants to consume more than the default USB current, it shall track vRd to determine the maximum current it may draw. See Table 4-36.		P
	Figure 4-36 and Figure 4-37 illustrate where the Sink monitors CC for vRd to detect if the host advertises more than the default USB current.		N/A
4.6.2.2	USB Battery Charging 1.2		P
	USB Battery Charging Specification, Revision 1.2 defines a method that uses the USB 2.0 D+ and D- pins to advertise VBUS can supply up to 1.5 A. Support for USB BC 1.2 charging is optional.		N/A
	A USB Type-C port that implements USB BC 1.2 that is capable of supplying at least 1.5 A shall advertise USB Type-C Current at the 1.5 A level within tVBUSON of entering the Attached.SRC state, otherwise the port shall advertise USB Type-C Current at the Default USB Power level. A USB Type-C port that implements USB BC 1.2 that also supports USB Type-C Current at 3.0 A may advertise USB Type-C Current at 3.0 A.		P
	If a Sink that supports USB BC 1.2 detection, detects Rp at the Default USB Power level and does not discover a USB BC 1.2-compliant Source, then it shall limit its maximum current consumption to the standard USB levels based on Table 4-17. This will ensure maximum current limits are not exceeded when connected to a Source which does not support USB BC 1.2.		N/A
	A Sink that supports USB BC 1.2 detection and has a maximum current draw greater than Default USB Type-C Current shall monitor vRd on the CC pins to detect the Source's Rp and shall implement Sink Power Sub-State transitions (Figure 4-19). If a Sink that supports USB BC 1.2 detection and has a maximum current draw greater than Default USB Type-C Current detects Rp at USB Type-C Current of 1.5 A or 3.0 A levels but does not detect a USB BC 1.2 source, it shall limit its maximum current consumption to the appropriate USB Type-C Current level advertised, and shall adjust its current consumption to remain within the value advertised by the Source on Sub-State transitions. For Sub-State transitions starting from a higher power level and ending at a lower power level, the Sink shall reduce power consumption within tSinkAdj. See Sections		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	4.5.2.3.2.2 and 4.5.2.3.3.2.		
	While in a Power Delivery Mode, a device acting as a Sink shall not initiate a USB BC 1.2 detection until the port pair is detached or there is an Error Recovery or Hard Reset.		N/A
4.6.2.3	Proprietary Power Source		P
	This section has been deprecated. Devices with USB Type-C connectors shall only employ signaling methods defined in USB specifications to negotiate power.		P
4.6.2.4	USB Power Delivery		P
	USB Power Delivery is a feature on the USB Type-C connector. When USB PD is implemented, USB PD Bi-phase Mark Coded (BMC) carried on the CC wire shall be used for USB PD communications between USB Type-C ports.		N/A
	At attach, VBUS shall be operationally stable prior to initiating USB PD communications.		N/A
	When not in an Explicit Contract, USB PD Sources that are, based on their PDP, capable of supplying:		N/A
	5 V at 3 A or greater shall advertise USB Type-C Current at the 3 A level		N/A
	5 V at 1.5A or greater but less than 3 A shall advertise USB Type-C Current at the 1.5 A level		N/A
	5 V at less than 1.5A shall advertise USB Type-C Current at the Default USB Power level		N/A
	within tVBUSON of entering the Attached.SRC state. For Multi-Port Shared Capacity Chargers, a USB PD Source capable of supplying 5 V at 3A or greater may initially offer USB Type-C Current at the 1.5 A level and subsequently increase the offer after attach (see Section 4.8.6.2). During USB Suspend a USB PD Source may set its Rp value to default to indicate that the Sink shall only draw USB suspend current as defined in Section 4.6.1.1.		N/A
	While a USB PD Explicit Contract is in place, a Source compliant with USB PD Revision 2 shall advertise a USB Type-C Current of either 1.5 A or 3.0 A. The USB PD Revision 2 Source upon entry into an Explicit Contract shall advertise an Rp value of 1.5 A or 3.0 A after it receives the GoodCRC in response to the first PS_RDY Message.		P
	While a USB PD Explicit Contract is in place, a Source compliant with USB PD Revision 3 shall set the Rp value according to the collision avoidance scheme defined in Section 5.7 of the USB PD Revision 3 specification. The USB PD Revision 3 Source upon entry into an Explicit Contract shall advertise an Rp value consistent with the USB PD Revision 3 collision avoidance		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	scheme.		
	Refer to Section 1.6 of the USB Power Delivery specification for a definition of an Explicit Contract.		N/A
4.6.2.5	Charge-Through VCONN-Powered USB Device (CTVPD) Current Limitations		N/A
	Since Charge-Through VCONN-Powered USB Devices implement charging by passively connecting the Source's CC and VBUS to the Host, the VCONN-Powered USB Device is effectively increasing the impedance on VBUS, GND, and CC between the Power Source and the Host, resulting in impedances that can exceed the maximum allowed for cables. To avoid communication issues and false disconnects from the increased GND and VBUS drops, the following shall occur:		N/A
	1. The Charge-Through VCONN-Powered USB Device shall report its worst-case GND and VBUS impedance (including the extra mated connector pair and FETs) in its USB PD Discover Identity Command response on SOP'.		N/A
	2. The Host that supports Charge-Through VCONN-Powered USB Device shall use this information, along with inferred information about the cable, to limit its maximum current in the case where the Power Source advertises a current greater than what the Charge-Through VCONN-Powered USB Device would allow.		N/A
	The Host has no way to query the cable, as its VCONN source is consumed by the VCONNPowered USB Device. Instead, the Host may assume the cable is 5 A for the purposes of calculating the Charge-Through current limit only if it receives a USB PD SourceCapability PDO of greater than 3 A (even if the Host ultimately does not Request that PDO, or if the host requests a current of 3 A or less).		N/A
	The Host shall further limit its maximum current beyond that advertised by the Power Source, based on the reported GND impedance and the inferred cable capability. GND impedance is reported in the VPD Discover Identity Command Response in 1-milliohm steps and is used in the following formulas:		N/A
	GND-limited current with a 3A cable inferred = $0.25 \text{ V} / (0.25 \text{ V} / 3 \text{ A} + \text{VPD_GND_DCR})$		N/A
	GND-limited current with a 5A cable inferred = $0.25 \text{ V} / (0.25 \text{ V} / 5 \text{ A} + \text{VPD_GND_DCR})$		N/A
	In addition, the increased VBUS impedance could result in a greater than 1 V VBUS drop as measured at the input to the Host. Based on the VBUS impedance reported in the VPD Discover Identity Command Response in 2-		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	milliohm steps and the inferred cable capability, the Host shall either lower its VBUS detach threshold or further limit its maximum current based on the following formulas:		
	VBUS and GND-limited current with a 3A cable inferred = $0.75 \text{ V} / (0.75 \text{ V} / 3 \text{ A} + \text{VPD_VBUS_DCR} + \text{VPD_GND_DCR})$		N/A
	VBUS and GND-limited current with a 5A cable inferred = $0.75 \text{ V} / (0.75 \text{ V} / 5 \text{ A} + \text{VPD_VBUS_DCR} + \text{VPD_GND_DCR})$		N/A
4.6.2.6	USB Type-C Sink Requirements for High Voltage Operation		N/A
	This section sets electrical requirements for USB Type-C Sinks that support high-voltage operation. See Section 3.11 for EPR requirements for USB Type-C cables that support EPR.		N/A
	The Sink shall keep the voltage on its VBUS contact to within 12 volts of the voltage on the Source VBUS contact at the time of the cable plug withdrawal for a minimum of 250 μs from the time the VBUS contacts separate (see Figure 3-1). Refer to Appendix H for more information related to high-voltage contact arcing and mitigation guidelines.		N/A
4.7	USB Hubs		P
	USB 2.0, USB 3.2, and USB4 hubs are defined by the USB 2.0, USB 3.2, and USB4 specifications, respectively. USB hubs implemented with one or more USB Type-C connectors shall comply with these specifications as relevant to a USB Type-C implementation. All the downstream facing USB Type-C ports on a USB hub should support the same functionality or shall be clearly marked as to the functionality supported.		N/A
	USB hubs shall have an upstream facing port (to connect to a host or hub higher in the USB tree) that may be a Sourcing Device (See Section 4.8.4). The hub shall clearly identify to the user its upstream facing port. This may be accomplished by physical isolation, labeling or a combination of both.		N/A
	USB hub's downstream facing ports shall not have Dual-Role-Data (DRD) capabilities. However, these ports may have Dual-Role-Power (DRP) capabilities.		N/A
	CC pins are used for port-to-port connections and shall be supported on all USB Type-C connections on the hub.		N/A
	For USB 2.0 and USB 3.2 hubs, downstream-facing ports shall not implement or pass-through Alternate or Accessory Modes and SBU pins shall not be connected (zSBU Termination) on any USB hub port. For		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	USB4 hubs, see Section 5.2.3.2 regarding support for Alternate Modes.		
	The USB hub's DFPs shall support power source requirements for a Source. See Section 4.8.1.		P
	Additional requirements for USB4 hubs are in Chapter 5.		N/A
4.8	Power Sourcing and Charging		P
	This section defines requirements and recommendations related to using USB Type-C ports for delivering power. Any USB Type-C port that offers more than Default Current and/or supports USB Power Delivery shall meet the requirements as if it is a charger.		N/A
	The following lists the most applicable subsections by USB Type-C ports on:		N/A
	Host systems: 4.8.1 and 4.8.5. Note: 4.8.6 is not intended for host systems.		N/A
	Devices that can supply power: 4.8.4.		N/A
	Hubs:		N/A
	Traditional hubs – Refer to USB 2.0/USB 3.2 base specifications and 4.8.1 as applicable if USB BC 1.2 is supported.		N/A
	Hubs that can supply power beyond the base specs – 4.8.1, 4.8.4, 4.8.5 and 4.8.6.		N/A
	Dedicated chargers:		N/A
	Single-port chargers – 4.8.1.		N/A
	Multi-port chargers – 4.8.1 and 4.8.6.		N/A
4.8.1	DFP as a Power Source		P
	Sources (e.g. battery chargers, hub downstream ports and hosts) may all be used for battery charging. When a charger is implemented with a USB Type-C receptacle or a USB Type-C captive cable, it shall follow all the applicable requirements.		P
	A Source shall expose its power capabilities using the USB Type-C Current method and it may additionally support other USB-standard methods (USB BC 1.2 or USBPD).		P
	A Source advertising its current capability using USB BC 1.2 shall meet the requirements in Section 4.6.2.2 regarding USB Type-C Current advertisement.		P
	A Source that has negotiated a USB-PD contract shall meet the requirements in Section 4.6.2.4 regarding USB Type-C Current advertisement.		P
	If a Source is capable of supplying a voltage greater than default VBUS, it shall fully conform to the USB-PD specification and shall negotiate		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	its power contracts using only USB-PD.		
	If a Source is capable of reversing source and sink power roles, it shall fully conform to the USB-PD specification and shall negotiate its power contracts using only USBPD.		N/A
	If a Source is capable of supplying a current greater than 3.0 A, it shall use the USBPD Discover Identity to determine the current carrying capacity of the cable.		N/A
4.8.1.1	USB-based Chargers with USB Type-C Receptacles		P
	A USB-based charger with a USB Type-C receptacle (Source) shall only apply power to VBUS when it detects a Sink is attached and shall remove power from VBUS when it detects the Sink is detached (vOPEN).		P
	A USB-based charger with a USB Type-C receptacle shall not advertise current exceeding 3.0 A except when it uses the USB-PD Discover Identity mechanism to determine the cable's actual current carrying capability and then it shall limit the advertised current accordingly.		N/A
	A USB-based charger with a USB Type-C receptacle (Source) which is not capable of data communication shall advertise USB Type-C Current of at least 1.5 A within tVBUSON of entering the Attached.SRC state and shall short D+ and D- together with a resistance less than 200 ohms. This will ensure backwards compatibility with legacy sinks which may use USB BC 1.2 for charger detection.		N/A
4.8.1.2	USB-based Chargers with USB Type-C Captive Cables		P
	A USB-based charger with a USB Type-C captive cable that supports USB PD shall only apply power to VBUS when it detects a Sink is attached and shall remove power from VBUS when it detects the Sink is detached (vOPEN).		P
	A USB-based charger with a USB Type-C captive cable that does not support USB PD may supply VBUS at any time. It is recommended that such a charger only apply power to VBUS when it detects a Sink is present and remove power from VBUS when it detects the Sink is not present (vOPEN).		N/A
	A USB-based charger with a USB Type-C captive cable shall limit its current advertisement so as not to exceed the current capability of the cable (up to 5 A).		N/A
	A USB-based charger with a USB Type-C captive cable which is not capable of data communication shall advertise USB Type-C Current of at least 1.5 A. It shall short D+ and D- together with a resistance less than 200		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	ohms. This will ensure backwards compatibility with legacy sinks which may use USB BC 1.2 for charging detection.		
	The voltage as measured at the plug of a USB-based charger with a USB Type-C captive cable may be up to $0.75 \times I / 3 \text{ V}$ ($0 < I \leq 3 \text{ A}$), or $0.75 \times I / 5 \text{ V}$ ($0 < I \leq 5 \text{ A}$) lower than the standard tolerance range for the chosen voltage, where I is the actual current being drawn.		N/A
	A USB-based charger that advertises USB Type-C Current shall output a voltage in the range of $4.75 \text{ V} - 5.5 \text{ V}$ when no current is being drawn and between $4.0 \text{ V} - 5.5 \text{ V}$ at 3 A . The output voltage as a function of load up to the advertised USB Type-C Current (default, 1.5 A and 3 A) shall remain within the cross-hatched area shown in Figure 4-40.		N/A
	A USB PD-based charger that has negotiated a voltage V at $\leq 3 \text{ A}$ shall output a voltage in the range of $V_{\text{max}} (V + 5\%)$ and $V_{\text{min}} (V - 5\%)$ when no current is being drawn and V_{max} and $V_{\text{min}} - 0.75 \text{ V}$ at 3 A . Under all loads, the output voltage shall remain within the cross-hatched area shown in Figure 4-41.		N/A
	A USB PD-based charger that has negotiated a voltage V at between 3 A and 5 A shall output a voltage in the range of $V_{\text{max}} (V + 5\%)$ and $V_{\text{min}} (V - 5\%)$ when no current is being drawn and V_{max} and $V_{\text{min}} - 0.75 \text{ V}$ at 5 A . Under all loads, the output voltage shall remain within the cross hatched area shown in Figure 4-42.		N/A
4.8.2	Non-USB Charging Methods		P
	A product (Source and/or Sink) with a USB Type-C connector shall only employ signalling methods defined in USB specifications to negotiate power over its USB Type-C connector(s).		P
4.8.3	Sinking Host		P
	A Sinking Host is a special sub-class of a DRP that is capable of consuming power but is not capable of acting as a USB device. For example a hub's DFP or a notebook's DFP that operates as a host but not as a device.		N/A
	The Sinking Host shall follow the rules for a DRP (See Section 4.5.1.4 and Figure 4-15). The Sinking DFP shall support USB PD and shall support the DR_Swap command in order to get the Sink into the DFP data role.		P
4.8.4	Sourcing Device		P
	A Sourcing Device is a special sub-class of a DRP that is capable of supplying power but is not capable of acting as a USB host. For example a hub's UFP or a monitor's UFP that		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	operates as a device but not as a host.		
	The Sourcing Device shall follow the rules for a DRP (See Section 4.5.1.4 and Figure 4-15). It shall also follow the requirements for the Source as Power Source (See Section 4.8.1). The Sourcing Device shall support USB PD and shall support the DR_Swap command in order to enable the Source to assume the UFP data role.		P
4.8.5	Charging a System with a Dead Battery		P
	A system that supports being charged by USB whose battery is dead shall apply R_d to both CC1 and CC2 and follow all Sink rules. When it is connected to a Source, DRP or Sourcing Device, the system will receive the default VBUS. It may use any allowed method to increase the amount of power it can use to charge its battery.		P
	Circuitry to present R_d in a dead battery case only needs to guarantee the voltage on CC is pulled within the same range as the voltage clamp implementation of R_d in order for a Source to recognize the Sink and provide VBUS. For example, a 20% resistor of value R_d in series with a FET with $V_{GTH(max)} < V_{CLAMP(max)}$ with the gate weakly pulled to CC would guarantee detection and be removable upon power up.		N/A
	When the system with a dead battery has sufficient charge, it may use the USB PD DR_Swap message to become the DFP.		N/A
4.8.6	USB Type-C Multi-Port Chargers		N/A
	A USB Type-C Multi-Port Charger is a product that exposes multiple USB Type-C Source ports for the purpose of charging multiple connected devices. A compliant USB Type-C charger may offer on each of its ports a mix of power options as defined in Section 4.6.		N/A
	Multi-Port Chargers will generally fall into two categories as defined by the following.		N/A
	1. Assured Capacity Chargers: a multi-port charger where the sum of the maximum capabilities of all of the exposed ports, as indicated to the user, is equal to the total power delivery capacity of the charger.		N/A
	2. Shared Capacity Chargers: a multi-port charger where the sum of the maximum capabilities of all of the exposed ports, as indicated to the user, is less than the total power delivery capacity of the charger.		N/A
	A Multi-Port Charger may offer in a single product separate visually identifiable groupings of charging ports. In this case, each group can independently offer either one of the two		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	charging categories, either an Assured Capacity Charger or a Shared Capacity Charger.		
	This section defines the requirements and provides guidelines for the operation and behaviour of a USB Type-C Multi-Port Charger.		N/A
4.8.6.1	General Requirements		N/A
	Individual source ports shall always comply with power negotiation and rules set forth by the USB Type-C and USB Power Delivery specifications, adjusted as needed when available resources change as other ports take more or less power.		N/A
	The minimum capability of all individual USB Type-C ports of a USB Type-C Multi-Port Charger shall be 5V @ 1.5 A independent of how many of the other ports are in use.		N/A
	When a USB Type-C Charger includes charging ports that are based on USB Standard-A receptacles, the following requirements shall be met.		N/A
	The USB Standard-A ports shall be implemented as an independent group, i.e. USB Standard-A ports shall not be included in a group of USB Type-C ports behaving as a Shared Capacity Charger. Any load change on a USB Type-A port shall not result in a voltage change on any of the USB Type-C ports and vice-versa.		N/A
	The minimum capability of each USB Standard-A port shall be 5V @ 500 mA independent of how many of the other ports are in use.		N/A
4.8.6.2	Multi-Port Charger Behaviors		N/A
	Each Source port of Assured Capacity Chargers shall, by design, behave independently and be unaffected by the status and loading of the other ports. An exception to this behavior is allowed if the charger has to take any action necessary to meet an overall product operational safety requirement due to unexpected behavior on any port.		N/A
	For Shared Capacity Chargers, the following behavioral rules shall apply:		N/A
	Each of the exposed Source Ports shall have the same power capabilities. Each port of the charger shall be capable of the same maximum capability, minimum capability, and be able to draw from the shared power equally.		N/A
	All exposed USB PD unattached Source Ports shall have the same power capabilities.		N/A
	Ports shall have the ability to supply the available shared capacity power up to the port's maximum power.		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	A shared capacity charger's ports may offer less than this value but shall increase the offer up to the required value when the Sink sets the Capabilities Mismatch bit in its response. This may be done in multiple steps, but all ports in the Shared Capacity Group shall reach the maximum power within three seconds.		N/A
	Whenever a power contract is made or changed on any port, the available shared capacity shall be re-computed, and the source shall send updated Source Capability messages as needed.		N/A
	As ports of a Shared Capacity Group are connected, each remaining unattached Source Port shall be capable of advertising the lower of the Maximum Capability of the port OR the Total Shared Capacity – the contracted power for the attached ports – (the number of unattached ports – 1) * the minimum port power.		N/A
	Ports shall offer at least 7.5 W.		N/A
	When calculating the available shared capacity for ports in a Fixed Supply power contract, the shared capacity charger shall use the Voltage times the Maximum Current in the PDO as the power the port is supplying regardless of the actual Operating Current requested in the RDO request.		N/A
	When calculating the available shared capacity for ports in a Fixed Supply power contract, the shared capacity charger shall use the Voltage times the Maximum Current in the PDO as the power the port is supplying regardless of the actual Operating Current requested in the RDO request.		N/A
	Ports when not in a PD contract shall follow the rules for a shared USB Type-C Current source unless there is sufficient remaining power for each port to advertise 15 W.		N/A
	All exposed USB Type-C Current ports shall have the ability to offer the same power capabilities.		N/A
	All ports shall initially offer at least 1.5 A.		N/A
	The total of offers across all the ports shall never exceed the capacity of the shared supply.		N/A
	Ports that initially offer 1.5 A shall increase to 3 A after attach if they have sufficient available shared capacity within one second.		N/A
	Ports shall never offer less than 1.5 A – e.g. shall not offer Default.		N/A
	As Source ports are connected and begin providing power, the remaining Source ports will each have the same power capabilities. The maximum capability may be less than the		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	previously connected ports due to less unused capacity of the total power delivery capacity of the charger. For example, if the total power delivery capacity of a USB Type-C two-port charger is 60 W with a port PDP of 35 W and the first connected Source port has established a 35 W power contract with its connected Sink, then the second Source port will only be able to offer a PDP of 25 W.		
	Each port should start by offering the minimum capability for the port and increase the offering to the Sink upon a connection. For example, if the maximum capability of a USB Type-C only Source port is 3 A, then all of the exposed Source ports will be able to offer 3A. Each port should start by offering less than the max (such as 1.5 A) and then increase the offering to 3 A after an attach. This would happen for each port as it is connected until the unused shared capacity is exhausted, at which point no other ports would increase to 3 A offering. A sink, in this example, would see a starting advertisement of USB Type-C Current @ 1.5 A at attach and would then see the USB Type-C Current advertisement increase to 3 A. As another example, if the maximum capability of a USB Type-C Source port is to offer USB PD with a PDP of 35 W, then all of the exposed Source ports would also support USB PD 35 W. Each port would start by offering something less on initial connection, like 15 W, and then increase the offering with new Source Capabilities when it determines the Sink would like more power. If the Sink is not offered the power it requires, it will send a request with the Capability Mismatch bit set to indicate to the source it wants more power. This will happen for each port as it is connected until the unused shared capacity is exhausted, at which point no other ports would increase the power offering.		N/A
	When establishing the remaining available capacity, a charger that supports policy-based power rebalancing may include the power that can be reclaimed from ports already in use:		N/A
	1. by adjusting advertised source capabilities equivalent with a reduced PDP to one or more ports that are already in use; or		N/A
	2. by issuing a USB PD GotoMin command to one or more ports already in use.		N/A
	Policy-based power rebalancing should consider providing good user experience and preserving nominal USB functionality on impacted devices. Fixed rebalancing algorithms that do not factor in overall USB system policy may not be appropriate for power rebalancing		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	implementations.		
4.8.6.3	Multi-Port Charger Port Labeling		N/A
	Multi-port chargers shall have OEM-designed port labeling consistent with the following rules.		N/A
	For Assured Capacity Chargers, each exposed Source port shall be labeled to indicate the PDP of the port. In this case, the user will be able to expect that each of the labeled ports will be able to meet power contracts consistent with the labelling independent of how many of the Source ports are in use.		N/A
	For Shared Capacity Chargers, each Source port shall be labeled to indicate the same PDP. Additionally, the charger shall have a label that, with a minimum of equal visual prominence, indicates the total power delivery capacity being shared across all of the ports identified as a group.		N/A
	A Multi-Port Charger that offers in a single product separate groupings of charging ports, each grouping shall be clearly identified as a separate grouping and each grouping shall be individually labeled consistent with that group's behavior model, either as an Assured Capacity Charger or a Shared Capacity Charger.		N/A
	Refer to the USB Implementers Forum (USB-IF) for USB Type-C Chargers certification along with further labeling guidelines.		N/A
4.8.6.4	Multi-Port Charger that include USB Data Hub Functionality		N/A
	Multi-Port chargers that also incorporate USB data hub capabilities shall meet the same requirements as standalone chargers. These charging-capable hubs shall be self-powered and shall fully operate as a charger independent of the state of the USB data bus connections.		N/A
	For hub-based Multi-Port Chargers that offer power to the upstream-facing port (to the host), this port may either behave as an Assured Capacity Charging port (e.g. be a dedicated charging port) or as a Shared Capacity Charging port (e.g. sharing capacity with downstream-facing ports). In either case, it should be clearly labeled consistent with its designed behavior, including identifying it as part of a group if it is sharing capacity with other ports.		N/A
	When the upstream-facing port is sharing capacity with the downstream-facing ports, the PDP of the upstream-facing port can differ from the downstream-facing ports.		N/A
4.9	Electronically Marked Cables		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	All USB Full-Featured Type-C cables shall be electronically marked. USB 2.0 Type-C cables may be electronically marked. An eMarker is element in an Electronically Marked Cable that returns information about the cable in response to a USB PD Discover Identity command.		N/A
	Electronically marked cables shall support USB Power Delivery Structured VDM Discover Identity command directed to SOP' (the eMarker). This provides a method to determine the characteristics of the cable, e.g. its current carrying capability, its performance, vendor identification, etc. This may be referred to as the USB Type-C Cable ID function.		N/A
	Prior to an explicit USB PD contract, a Sourcing Device is allowed to use SOP' to discover the cable's identity. After an explicit USB PD contract has been negotiated, only the Source shall communicate with SOP' and SOP" (see Section 6.2.1).		N/A
	Passive cables that include an eMarker shall follow the Cable State Machine defined in Section 4.5.2.4 and Figure 4-20.		N/A
	Once VCONN is available, all electronically marked cables shall use it as the only power source. If VCONN is applied after VBUS then until VCONN is available, the cable may remain unpowered or may draw power from VBUS. Within tVCONNSwitch, the cable shall switch from VBUS to VCONN. Cables that include an eMarker shall meet the maximum power defined in Table 4-6. The only exception is an Optically Isolated Active Cable (OIAC Section 6), which can draw from both VCONN and VBUS.		N/A
	Refer to Table 4-5 for the requirements of a Source to supply VCONN. When VCONN is not present, a powered cable shall not interfere with normal CC operation including Sink detection, current advertisement and USB PD operation.		N/A
	Figure 4-43 illustrates a typical electronically marked cable. The isolation elements (Iso) shall prevent VCONN from traversing end-to-end through the cable. Ra is required in the cable to allow the Source to determine that VCONN is needed.		N/A
	Figure 4-44 illustrates an electronically marked cable where the VCONN wire does not extend through the cable, therefore an SOP' (eMarker) element is required at each end of the cable. In this case, no isolation elements are needed.		N/A
	For cables that only respond to SOP', the location of the responder is not relevant.		N/A
4.9.1	Parameter Values		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
4.9.2	Active Cables		N/A
	An active cable is an electronically marked cable that incorporates data bus signal conditioning circuits, for example to allow for implementing longer cables. Active cables with data bus signal conditioning in both plugs shall implement SOP' and may implement SOP". Active cables shall meet the power requirements defined in Table 4-6.		N/A
	Active cables may support either one TX/RX pair or two TX/RX pairs. The eMarker in the cable shall identify the number of TX/RX lanes supported. Active cables may or may not require configuration management. Active cable configuration management is defined in Section 5.5.4.		N/A
4.10	VCONN-Powered Accessories (VPAs) and VCONN-Powered USB Devices (VPDs)		N/A
	VCONN-Powered Accessories and VCONN-Powered USB Devices are both direct-attach Sinks that can operate with just VCONN.		N/A
	Both expose a maximum impedance to ground of Ra on the VCONN pin and Rd on the CC pin.		N/A
	The removal of VCONN when VBUS is not present shall be treated as a detach event.		N/A
4.10.1	VCONN-Powered Accessories (VPAs)		N/A
	A VCONN-Powered Accessory implements an Alternate Mode (See Appendix E).		N/A
	VCONN-Powered Accessories shall comply with Table 4-7.		N/A
	When operating in the Sink role and when VBUS is not present, VCONN-Powered Accessories shall treat the application of VCONN as an attach signal, and shall respond to USB Power Delivery messages.		N/A
	When powered by only VCONN, a VCONN-Powered Accessory shall negotiate an Alternate Mode. If it fails to negotiate an Alternate Mode within tAMETimeout, its port partner removes VCONN.		N/A
	When VBUS is supplied, a VCONN-Powered Accessory is subject to all of the requirements for Alternate Modes, including presenting a USB Billboard Device Class interface if negotiation for an Alternate Mode fails.		N/A
	Should a VCONN-Powered Accessory wish to provide charge-through functionality, it must do so by negotiating voltage and current independently on both the Host and charge-through ports, and possibly re-regulating the voltage from the Source before passing it through to the Sink. The Sink is able to take the		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	full current that is advertised to it by the VCONN-Powered Accessory.		
4.10.2	VCONN-Powered USB Devices (VPDs)		N/A
	A VCONN-Powered USB Device shall implement a USB UFP endpoint.		N/A
	VCONN-Powered USB Devices shall comply with Table 4-8.		N/A
	When VBUS is not present, VCONN-Powered USB Devices shall treat the application of VCONN as an attach signal.		N/A
	A VCONN-Powered USB Device shall respond to USB PD messaging on SOP' and shall not respond to other USB PD messaging. A VCONN-Powered USB Device shall respond to USB PD Hard Reset and Cable Reset signaling.		N/A
	A Charge-Through VCONN -Powered USB Device shall discard all USB PD messages while a connection is enabled between the host port CC and Charge-Through port CC.		N/A
	When VBUS is supplied by the Host, the VCONN-Powered USB Device shall behave like a normal UFP Sink, but still only respond to USB PD messaging on SOP'. If VBUS is subsequently removed while VCONN remains applied, the VCONN-Powered USB Device shall remain connected, and use VCONN as the sole detach signal.		N/A
	Since VCONN-Powered USB Devices do not respond to USB PD on SOP, they cannot enter Alternate Modes.		N/A
	A VCONN-Powered USB Device may provide Charge-Through functionality via VPD Charge-Through. VCONN-Powered USB Devices shall not provide any data pass-through to the Charge-Through port other than the CC wire.		N/A
	Since the power and CC negotiation is passed through directly, the Sink shall limit its maximum current based on the additional impedance introduced by the VCONN-Powered USB Device.		N/A
	Additionally, since power can only flow from the Charge-Through port to the Host, VCONN must be provided by the host, and there is no data connection beyond the CC wire passed through to the connected source, there are limitations on what the Host can advertise and support via USB PD:		N/A
	The Host shall not negotiate or accept a PR_Swap or VCONN_Swap		N/A
	The Host shall not enable FR_Swap		N/A
	The Host may only negotiate a DR_Swap when using USB PD Revision 2.0, and only for the		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	purpose of switching which side initiates PD communications. The Host will always remain a DFP for USB data.		
	The Host shall not advertise dual-role data or dual-role power in its SourceCapability or SinkCapability messages – Host changes its advertised capabilities to UFP role/sink only role.		N/A
	The Host shall not negotiate any Alternate Modes that change the function of pins on the connector.		N/A
	The Host shall represent itself to the Charge-Through Source using USB PD as if it were a Sink-only, data-less device.		N/A
4.11	Parameter Values		N/A
4.11.1	Termination Parameters		N/A
	Table 4-24 provides the values that shall be used for the Source's Rp or current source. Other pull-up voltages shall be allowed if they remain less than 5.5 V and fall within the correct voltage ranges on the Sink side – see Table 4-32, Table 4-33 and Table 4-34. Note: when two Sources are connected together, they may use different termination methods which could result in unexpected current flow.		N/A
	The Sink may find it convenient to implement Rd in multiple ways simultaneously (a wide range Rd when unpowered and a trimmed Rd when powered). Transitions between Rd implementations that do not exceed tCCDebounce shall not be interpreted as exceeding the wider Rd range. Transitions between Rd implementations shall not allow the voltage on CC to go outside the voltage band that defines a connection. Table 4-25 provides the methods and values that shall be used for the Sink's Rd implementation.		N/A
	Table 4-27 provides the minimum impedance value to ground on CC for a device (Sink or Source) to be undetected by a Source. This shall apply for ports in the Disabled state or ErrorRecovery state. This shall also apply for Sources when unpowered (for example a power brick unplugged from AC mains).		N/A
4.11.2	Timing Parameters		N/A
	Table 4-29 provides the timing values that shall be met for delivering power over VBUS and VCONN.		N/A
	Figure 4-46 illustrates the timing parameters associated with the DRP toggling process. The tDRP parameter represents the overall period for a single cycle during which the port is exposed as both a Source and a Sink. The portion of the period where the DRP is exposed		N/A

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Clause	Requirement + Test	Result - Remark	Verdict
	as a Source is established by dcSRC.DRP and the maximum transition time between the exposed states is dictated by tDRPTransition.		
	Table 4-30 provides the timing values that shall be met for DRPs. The clock used to control DRP swap should not be derived from a precision timing source such as a crystal, ceramic resonator, etc. to help minimize the probability of two DRP devices indefinitely failing to resolve into a Source-to-Sink relationship. Similarly, the percentage of time that a DRP spends advertising Source should not be derived from a precision timing source.		N/A
	Table 4-31 provides the timing requirement for CC connection behaviors.		N/A
4.11.3	Voltage Parameters		N/A
	Table 4-32, Table 4-33 and Table 4-34 provide the CC voltage values that a Source shall use to detect what is attached based on the USB Type-C Current advertisement (Default USB, 1.5A @ 5 V, or 3.0 A @ 5 V) that the Source is offering.		N/A
	Table 4-35 provides the CC voltage values that shall be detected across a Sink's Rd for a Sink that does not support higher than default USB Type-C Current Source advertisements.		N/A
	Table 4-36 provides the CC voltage values that shall be detected across a Sink's Rd for a Sink that implements detection of higher than default USB Type-C Current Source advertisements. This table includes consideration for the effect that the IR drop across the cable GND has on the voltage across the Sink's Rd.		N/A
	Table 4-37 provides the clamping voltage that any port (Source, Sink or DRP) may clamp its CC pin to protect from damage. The inclusion of clamping shall not impact the functionality when the CC pin is functioning as VCONN Source or Sink.		N/A

GRL-USB-PD Compliance Test Solution

DUT Information

Manufacturer : Shenzhen Huafurui Technology Co., Ltd.
Model : X100
Serial No. :

Test Information

Test Lab : Shenzhen TCT Testing Technology Co., Ltd.
Test_Engineer : Kevin Li
Remarks : Remarks
Date : 2025_06_05

Environment Information

Parameter	Value
GRL_USB_PD_Controller_Serial_No	GRL-C2-EPR-2022070
GRL_USB_PD_Software_Version	1.6.30.0
GRL_USB_PD_Firmware_Version	1.2.72
GRL USB-PD Ethernet Buffer Size	62K
GRL USB-PD Eload Firmware Version	1.5 / 1.5
GRL USB-PD PPS Firmware Version	4.0 / 4.0
Calibration	Calibration Success
RX mask Power selection	Neutral Power
Device_Type	DRP

Parameter	Value
Cable Type	GRL_SPL_EPR_CABLE_1
Impedance (milli ohm)	1
PD_Merged CTS Version	v.Q1-2025
FUNCTIONAL_TESTS CTS Version	v0.90
USB_PD_Spec Version	Rev3.2 Ver1.1RC2
USB_Type_C_Spec Version	v2.3 Oct-2023
VIF_File_Name	MTK_MT6375P_Revision-1.1_10146.xml
Noise Pattern Generation:	Two-Tone Noise
Application mode	Compliance

Power Delivery 3.2 Tests Information

Parameter	Value
Connect EPR Test Fixture	False
FR_Swap AUTO Box Connected	False

USB-C Functional Tests Information

Parameter	Value	Parameter
Connect EPR Test Fixture	False	
FR_Swap AUTO Box Connected	False	
Enable USB Data validation	Enabled	
Is Dead Battery connected to PUT	Enabled	
Number of USB Type-C Ports	0	
Number of USB Type-B or Micro-B Ports or Type-A plug	0	
Connected Hub is Embedded	Disabled	

Device Info Capabilities

Parameter	Vendor Info File	Get Capabilities
Port_Label	0	
Connector_Type	Type-C	
USB4_Supported	NO	
USB_PD_Support	YES	
PD_Port_Type	DRP	
Type_C_State_Machine	DRP	
Port_Battery_Powered	YES	
BC_1_2_Support	Portable Device	
Captive_Cable	NO	
PD_Spec_Revision_Major	3	
PD_Spec_Revision_Minor	1	
PD_Spec_Version_Major	2	
PD_Spec_Version_Minor	0	
PD_Specification_Revision	Revision 3	
SOP_Capable	YES	
SOP_P_Capable	NO	
SOP_PP_Capable	NO	
SOP_P_Debug_Capable	NO	
SOP_PP_Debug_Capable	NO	
Manufacturer_Info_Supported_Port	NO	
Chunking_Implemented_SOP	YES	
Unchunked_Extended_Messages_Supported	NO	
Security_Msgs_Supported_SOP	NO	
Unconstrained_Power	NO	
Num_Fixed_Batteries	1	
Num_Swappable_Battery_Slots	0	
ID_Header_Connector_Type_SOP	USB Type-C Receptacle	
USB_Comms_Capable	YES	
DR_Swap_To_DFP_Supported	YES	
DR_Swap_To_UFP_Supported	YES	
VCONN_Swap_To_On_Supported	NO	

Parameter	Vendor Info File	Get Capabilities
VCONN_Swap_To_Off_Supported	NO	
Responds_To_Discov_SOP_UFP	YES	
Responds_To_Discov_SOP_DFP	YES	
Attempts_Discov_SOP	YES	
Power_Interruption_Available	No Interruption Possible	
Data_Reset_Supported	NO	
Enter_USB_Supported	YES	
Type_C_Can_Act_As_Host	YES	
Type_C_Can_Act_As_Device	YES	
Type_C_Implements_Try_SRC	NO	
Type_C_Implements_Try_SNK	YES	
Type_C_Supports_Audio_Accessory	NO	
Type_C_Is_VCONN_Powered_Accessory	NO	
Type_C_Is_Debug_Target_SRC	YES	
Type_C_Is_Debug_Target_SNK	YES	
RP_Value	Default	
Type_C_Port_On_Hub	NO	
Type_C_Power_Source	Both	
Type_C_Sources_VCONN	NO	
Type_C_Is_Alt_Mode_Controller	NO	
Type_C_Is_Alt_Mode_Adapter	NO	
Product_Total_Source_Power_mW	15000	
Port_Source_Power_Type	Assured	
Host_Supports_USB_Data	YES	
Host_Speed	USB 2	
Host_Contains_Captive_Retimer	NO	
Host_Is_Embedded	YES	
Host_Suspend_Supported	NO	
Is_DFP_On_Hub	NO	
Device_Supports_USB_Data	1	
Device_Speed	USB 2	
Device_Max_USB2_Speed	High Speed	
Device_Contains_Captive_Retimer	NO	
EPR_Supported_As_Src	NO	

Parameter	Vendor Info File	Get Capabilities
FR_Swap_Type_C_Current_Capability_As_Initial_Sink	FR_Swap not supported	
Master_Port	YES	
Has_Invariant_PDOs	YES	
Port_Managed_Guaranteed_Type	Guaranteed Capability	
EPR_Supported_As_Snk	NO	
Accepts_PR_Swap_As_Src	YES	
Accepts_PR_Swap_As_Snk	YES	
Requests_PR_Swap_As_Src	NO	
Requests_PR_Swap_As_Snk	NO	
FR_Swap_Supported_As_Initial_Sink	NO	
XID_SOP	0	
Data_Capable_As_USB_Host_SOP	YES	
Data_Capable_As_USB_Device_SOP	YES	
Product_Type_UFP_SOP	PDUSB Peripheral	
Product_Type_DFP_SOP	PDUSB Host	
DFP_VDO_Port_Number	0	
Modal_Operation_Supported_SOP	NO	
USB_VID_SOP	0000	
PID_SOP	0000	
bcdDevice_SOP	0000	
PD_Power_As_Source	5000	
USB_Suspend_May_Be_Cleared	YES	
Sends_Pings	NO	
Num_Src_PDOs	1 Src PDO	
PD_OC_Protection	NO	
PD_Power_As_Sink	27000	
No_USB_Suspend_May_Be_Set	YES	
GiveBack_May_Be_Set	NO	
Higher_Capability_Set	NO	
FR_Swap_Reqd_Type_C_Current_As_Initial_Source	FR_Swap not supported	
Num_Snk_PDOs	3 Snk PDOs	
Src_PDO_Supply_Type_#1	Fixed	
Src_PDO_Peak_Current_#1	100% IOC	
Src_PDO_Voltage_#1	5000 mV	

Parameter	Vendor Info File	Get Capabilities
Src_PDO_Max_Current #1	2000 mA	
Snk_PDO_Supply_Type #1	Fixed	
Snk_PDO_Voltage #1	5000 mV	
Snk_PDO_Op_Current #1	2000 mA	
Snk_PDO_Supply_Type #2	Fixed	
Snk_PDO_Voltage #2	9000 mV	
Snk_PDO_Op_Current #2	3000 mA	
Snk_PDO_Supply_Type #3	Augmented	
Snk_PDO_APDO_Type #3	Programmable Power Supply (SPR)	
Snk_PDO_Min_Voltage #3	5000 mV	
Snk_PDO_Max_Voltage #3	9000 mV	
Snk_PDO_Op_Current #3	3000 mA	

PD_Merged Result

SI No	Test ID	Test Name	Test Result
1	TEST.PD.PHY.ALL.1	TEST.PD.PHY.ALL.1 Transmit Bit Rate and the Drift	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet16	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet18	PASS
		Rev3ChkdSnk	PASS
		fBitRateMeas - TEST.PD.PHY.ALL.1#1	PASS
		Bit Rate-1 >>Valid Protocol response for BIST Request	PASS
		Bit Rate-2 >>Valid BIST response pattern	PASS
		Bit Rate-3 >>Bit Rate is 296.572 Kbps. Test limit (270 ~ 330) Kbps	PASS
		pBitRateMeas - TEST.PD.PHY.ALL.1#2	PASS

SI No	Test ID	Test Name	Test Result
		Bit Rate-4 >>Bit Rate is 0.01 %. Test limit: X < 0.25%	PASS
		tBISTContMode Limits validation - TEST.PD.PHY.ALL.1#3	PASS
		Bit Rate-5 >>BIST pattern duration 55.2391203 mS [Limit : (30 ~ 60)ms]	PASS
		--- 1/1 captures completed	
2	TEST.PD.PHY.ALL.2	TEST.PD.PHY.ALL.2 Transmitter Eye Diagram	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet16	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet18	PASS
		Rev3ChkdSnk	PASS
		fBitRateMeas - TEST.PD.PHY.ALL.2#1	PASS
		Eye diagram-1 >>Valid Protocol response for BIST Request	PASS
		Eye diagram-2 >>Valid BIST response pattern	PASS
		Eye diagram-3 >>Eye diagram plot passed at Mid Crossing Level.	PASS
		pBitRateMeas - TEST.PD.PHY.ALL.2#2	PASS
		Eye diagram-4 >>BIST pattern duration 55.2523700 mS [Limit : (30 ~ 60)ms]	PASS

SI No	Test ID	Test Name	Test Result
		BMC_PHY_TX_EYE_5 >>Rise time: Average value = 440.925348 nS Minimum value = 429.797329 nS Maximum value = 457.062341 nS Minimum Limit = 300 ns Fall time: Average value = 499.796585 nS Minimum value = 484.304551 nS Maximum value = 521.919414 nS Minimum Limit = 300 ns	PASS
		--- 1/1 captures completed	
3	TEST.PD.PHY.ALL.3	TEST.PD.PHY.ALL.3 Collision Avoidance	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk	PASS
		>>SourceCap Packet16	
		UUT should respond with request - - COMMON.PROC.BU.2#1	PASS
		>>Request Packet18	
		Rev3ChkdSnk	PASS
		>> Packet42	
		Alternating 0's and 1's for 200us - TEST.PD.PHY.ALL.3#1	PASS
		>>Packet52	
		Continuous 0's for 195us - TEST.PD.PHY.ALL.3#2	PASS
		>>Packet62	
		--- 2/2 captures completed	
4	TEST.PD.PHY.ALL.4	TEST.PD.PHY.ALL.4 Bus Idle Detection	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk	PASS
		>>SourceCap Packet16	
		UUT should respond with request - - COMMON.PROC.BU.2#1	PASS
		>>Request Packet18	
		Rev3ChkdSnk	PASS
		>> First BIST message Packet 42	

SI No	Test ID	Test Name	Test Result
		Check BusIdle - TEST.PD.PHY.ALL.4#1 >>UUT respond GoodCRC to BIST_Test_Data	PASS
		--- 1/1 captures completed	
5	TEST.PD.PHY.ALL.5	TEST.PD.PHY.ALL.5 Receiver Interference Rejection	PASS
		Rev3ChkdSnk	PASS
		TX Group 1 Noise Src - TEST.PD.PHY.ALL.5#1 >>BIST count 13362 , GoodCRC count 13362	PASS
		TX Group 2 Noise - TEST.PD.PHY.ALL.5#2 >>BIST count 13362 , GoodCRC count 13362	PASS
		Rev3ChkdSrc	PASS
		TX Group 1 Noise Snk - TEST.PD.PHY.ALL.5#1 >>BIST count 13362 , GoodCRC count 13362	PASS
		TX Group 3 Noise - TEST.PD.PHY.ALL.5#3 >>BIST count 13362 , GoodCRC count 13362	PASS
		--- 4/4 captures completed	
6	TEST.PD.PHY.ALL.6	TEST.PD.PHY.ALL.6 Invalid SOP*	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet16	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet18	PASS
		Rev3ChkdSnk	PASS
		Check DUT Response - TEST.PD.PHY.ALL.6#1	PASS
7	TEST.PD.PHY.ALL.7	TEST.PD.PHY.ALL.7 Valid SOP*	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet17	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet19	PASS
		Rev3ChkdSnk	PASS
		Check BIST Response for SOP - TEST.PD.PHY.ALL.7#2 >DUT could respond with GoodCRC for all SOP BIST messages, No of GoodCRC's responded by DUT is 9	PASS

SI No	Test ID	Test Name	Test Result
		Check BIST Response for SOP1 - TEST.PD.PHY.ALL.7#3	PASS
		Check BIST Response for SOP2 - TEST.PD.PHY.ALL.7#5	PASS
		Check BIST Response for SOP1_Debug - TEST.PD.PHY.ALL.7#7	PASS
		Check BIST Response for SOP2_Debug - TEST.PD.PHY.ALL.7#8	PASS
8	TEST.PD.PHY.ALL.8	TEST.PD.PHY.ALL.8 Incorrect CRC	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet16	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet18	PASS
		Rev3ChkdSnk	PASS
		Check Flip 0 on CRC before 4b5b encoding - TEST.PD.PHY.ALL.8#2	PASS
		Check Flip 0 on CRC after 4b5b encoding - TEST.PD.PHY.ALL.8#2	PASS
		Check Flip 0 on payload before 4b5b encoding - TEST.PD.PHY.ALL.8#2	PASS
		Check Flip 0 on payload after 4b5b encoding - TEST.PD.PHY.ALL.8#2	PASS
		Check replace third 5b symbol - TEST.PD.PHY.ALL.8#2	PASS
9	TEST.PD.PHY.ALL.9	TEST.PD.PHY.ALL.9 Receiver Input Impedance	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet16	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet18	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet62	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet64	PASS
		Rev3ChkdSnk	PASS
		Sink UUT voltage on the CC line - TEST.PD.PHY.ALL.9#1 >>CC-line voltage is 1.055V at time 2.94236047s	PASS
		Source UUT voltage on the CC line - TEST.PD.PHY.ALL.9#2	PASS
		Cable Plug voltage on the CC line - TEST.PD.PHY.ALL.9#3	PASS
		Rev3ChkdSnk	PASS

SI No	Test ID	Test Name	Test Result
		Sink UUT voltage on the CC line - TEST.PD.PHY.ALL.9#4 >>CC-line voltage is 1.055V at time 6.18836911s	PASS
		Cable Plug voltage on the CC line [Without VCONN or VBUS] - TEST.PD.PHY.ALL.9#5	PASS
10	TEST.PD.PHY.PORT.1	TEST.PD.PHY.PORT.1 Invalid Reset Signals	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet16	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet18	PASS
		Rev3ChkdSnk	PASS
		Check Response message - TEST.PD.PHY.PORT.1#1	PASS
		Check Response message - TEST.PD.PHY.PORT.1#2	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 15.085s and SourceCap time: 15.149s at protocol index #129 [PASS] Max = 250ms. Obtained time difference is 63.327ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		Rev3ChkdSrc	PASS
		Check Response message - TEST.PD.PHY.PORT.1#1	PASS
		Check Response message - TEST.PD.PHY.PORT.1#2	PASS
11	TEST.PD.PROT.ALL.1	TEST.PD.PROT.ALL.1 Corrupted GoodCRC	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk >>SourceCap Packet14	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet16	PASS

SI No	Test ID	Test Name	Test Result
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet89	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet91	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 13.377s and SourceCap time: 13.439s at protocol index #199 [PASS] Max = 250ms. Obtained time difference is 61.661ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 18.927s and SourceCap time: 18.991s at protocol index #289 [PASS] Max = 250ms. Obtained time difference is 64.16ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 > Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		Rev2Snk	PASS
		GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.1#2	PASS
		SinkCap retransmit check - TEST.PD.PROT.ALL.1#5	PASS
		GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.1#7	PASS
		SinkCap retransmit check - TEST.PD.PROT.ALL.1#10	PASS

SI No	Test ID	Test Name	Test Result
		SinkCap retransmit messageId check - TEST.PD.PROT.ALL.1#11 >>Tester sent Get_Sink_Cap message Packet 56 Tester sent Get_Source_Cap message Packet 60	PASS
		UUT SoftReset Check - TEST.PD.PROT.ALL.1#12 >>UUT sent SoftReset message at protocol index 62	PASS
		Rev3ChkdSnk	PASS
		GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.1#2	PASS
		SinkCap retransmit check - TEST.PD.PROT.ALL.1#5	PASS
		GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.1#7	PASS
		SinkCap retransmit check - TEST.PD.PROT.ALL.1#10	PASS
		SinkCap retransmit messageId check - TEST.PD.PROT.ALL.1#11 >>Tester sent Get_Sink_Cap message Packet 155 Tester sent Get_Source_Cap message Packet 159	PASS
		UUT SoftReset Check - TEST.PD.PROT.ALL.1#12 >>UUT sent SoftReset message at protocol index 163	PASS
		Rev2Src	PASS
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.1#3	PASS
		SinkCap retransmit check - TEST.PD.PROT.ALL.1#5	PASS
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.1#8	PASS
		SinkCap retransmit check - TEST.PD.PROT.ALL.1#10	PASS
		SinkCap retransmit messageId check - TEST.PD.PROT.ALL.1#11 >>Tester sent Get_Sink_Cap message Packet 253 Tester sent Get_Source_Cap message Packet 257	PASS
		UUT SoftReset Check - TEST.PD.PROT.ALL.1#12 >>UUT sent SoftReset message at protocol index 259	PASS
		Rev3ChkdSrc	PASS
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.1#3	PASS
		SinkCap retransmit check - TEST.PD.PROT.ALL.1#5	PASS

SI No	Test ID	Test Name	Test Result
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.1#8	PASS
		SinkCap retransmit check - TEST.PD.PROT.ALL.1#10	PASS
		SinkCap retransmit messageID check - TEST.PD.PROT.ALL.1#11 >>Tester sent Get_Sink_Cap message Packet 343 Tester sent Get_Source_Cap message Packet 347	PASS
		UUT SoftReset Check - TEST.PD.PROT.ALL.1#12 >>UUT sent SoftReset message at protocol index 349	PASS
12	TEST.PD.PROT.ALL.2	TEST.PD.PROT.ALL.2 Soft Reset and Hard Reset	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk >>SourceCap Packet14	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet16	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet80	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet82	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 15.151s and SourceCap time: 15.213s at protocol index #183 [PASS] Max = 250ms. Obtained time difference is 62.494ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS

SI No	Test ID	Test Name	Test Result
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 21.659s and SourceCap time: 21.722s at protocol index #277 [PASS] Max = 250ms. Obtained time difference is 63.327ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		Rev2Snk	PASS
		GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.2#2 >>UUT sent SinkCap at protocol index#27	PASS
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.2#3	PASS
		UUT retransmit check - TEST.PD.PROT.ALL.2#5 >>UUT retransmitted the SinkCap message 3 times at the protocol index 27.	PASS
		SoftReset from UUT - TEST.PD.PROT.ALL.2#7	PASS
		UUT Response check - TEST.PD.PROT.ALL.2#8 >>UUT sent Request message at protocol index : 38	PASS
		GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.2#12 >>UUT sent SinkCap at protocol index#47	PASS
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.2#13	PASS
		UUT retransmit check - TEST.PD.PROT.ALL.2#15 >>UUT retransmitted the SinkCap message 3 times at the protocol index 47.	PASS
		SoftReset from UUT - TEST.PD.PROT.ALL.2#17	PASS
		UUT retransmit check - TEST.PD.PROT.ALL.2#18 >>UUT retransmitted the SoftReset message 3 times at the protocol index 51.	PASS
		UUT Hard Reset message check - TEST.PD.PROT.ALL.2#19 >>UUT sent Hard_Reset message Packet 55 [PASS] Max = 6.1ms. Obtained time difference is 4.875ms	PASS
		Rev3ChkdSnk	PASS

SI No	Test ID	Test Name	Test Result
		GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.2#2 >>UUT sent SinkCap at protocol index#108	PASS
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.2#3	PASS
		UUT retransmit check - TEST.PD.PROT.ALL.2#5 >>UUT retransmitted the SinkCap message 2 times at the protocol index 108.	PASS
		SoftReset from UUT - TEST.PD.PROT.ALL.2#7	PASS
		UUT Response check - TEST.PD.PROT.ALL.2#8 >>UUT sent Request message at protocol index : 120	PASS
		GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.2#12 >>UUT sent SinkCap at protocol index#133	PASS
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.2#13	PASS
		UUT retransmit check - TEST.PD.PROT.ALL.2#15 >>UUT retransmitted the SinkCap message 2 times at the protocol index 133.	PASS
		SoftReset from UUT - TEST.PD.PROT.ALL.2#17	PASS
		UUT retransmit check - TEST.PD.PROT.ALL.2#18 >>UUT retransmitted the SoftReset message 2 times at the protocol index 138.	PASS
		UUT Hard Reset message check - TEST.PD.PROT.ALL.2#19 >>UUT sent Hard_Reset message Packet 142 [PASS] Max = 6.1ms. Obtained time difference is 4.395ms	PASS
		Rev2Src	PASS
		GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.2#2	PASS
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.2#3 >>UUT is a DRP and sent SinkCap at the protocol index 209	PASS
		UUT retransmit check - TEST.PD.PROT.ALL.2#5 >>UUT retransmitted the SinkCap message 3 times at the protocol index 209.	PASS
		SoftReset from UUT - TEST.PD.PROT.ALL.2#9	PASS
		UUT Response check - TEST.PD.PROT.ALL.2#10 >>UUT sent Request message at protocol index : 219	PASS
		GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.2#12	PASS

SI No	Test ID	Test Name	Test Result
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.2#13 >>UUT is a DRP and sent SinkCap at the protocol index 228	PASS
		UUT retransmit check - TEST.PD.PROT.ALL.2#15 >>UUT retransmitted the SinkCap message 3 times at the protocol index 228.	PASS
		SoftReset from UUT - TEST.PD.PROT.ALL.2#17	PASS
		UUT retransmit check - TEST.PD.PROT.ALL.2#18 >>UUT retransmitted the SoftReset message 3 times at the protocol index 232.	PASS
		UUT Hard Reset message check - TEST.PD.PROT.ALL.2#19 >>UUT sent Hard_Reset message Packet 236 [PASS] Max = 6.1ms. Obtained time difference is 3.346ms	PASS
		Rev3ChkdSrc	PASS
		GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.2#2	PASS
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.2#3 >>UUT is a DRP and sent SinkCap at the protocol index 305	PASS
		UUT retransmit check - TEST.PD.PROT.ALL.2#5 >>UUT retransmitted the SinkCap message 2 times at the protocol index 305.	PASS
		SoftReset from UUT - TEST.PD.PROT.ALL.2#9	PASS
		UUT Response check - TEST.PD.PROT.ALL.2#10 >>UUT sent Request message at protocol index : 314	PASS
		GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.2#12	PASS
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.2#13 >>UUT is a DRP and sent SinkCap at the protocol index 323	PASS
		UUT retransmit check - TEST.PD.PROT.ALL.2#15 >>UUT retransmitted the SinkCap message 2 times at the protocol index 323.	PASS
		SoftReset from UUT - TEST.PD.PROT.ALL.2#17	PASS
		UUT retransmit check - TEST.PD.PROT.ALL.2#18 >>UUT retransmitted the SoftReset message 2 times at the protocol index 326.	PASS

SI No	Test ID	Test Name	Test Result
		UUT Hard Reset message check - TEST.PD.PROT.ALL.2#19 >>UUT sent Hard_Reset message Packet 329 [PASS] Max = 6.1ms. Obtained time difference is 3.669ms	PASS
13	TEST.PD.PROT.ALL.3	TEST.PD.PROT.ALL.3 Soft Reset response	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk >>SourceCap Packet14	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet16	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet82	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet84	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 11.232s and SourceCap time: 11.294s at protocol index #188 [PASS] Max = 250ms. Obtained time difference is 61.661ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 > Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 15.78s and SourceCap time: 15.843s at protocol index #275 [PASS] Max = 250ms. Obtained time difference is 63.327ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 > Please check the capture and confirm	PASS

SI No	Test ID	Test Name	Test Result
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		Rev2Snk	PASS
		GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.3#2 >>UUT is a DRP and it sent SinkCap message at the protocol index 27	PASS
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.3#3	PASS
		Soft Reset message validation - TEST.PD.PROT.ALL.3#4	PASS
		UUT Request message check - TEST.PD.PROT.ALL.3#5 >>DUT sent Request message at protocol index: 56	PASS
		Source Capabilities message validation - TEST.PD.PROT.ALL.3#6	PASS
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.3#8 >>DUT responded with SinkCap to Get_Sink_Cap at protocol index : 65	PASS
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.3#9	PASS
		Rev3ChkdSnk	PASS
		GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.3#2 >>UUT is a DRP and it sent SinkCap message at the protocol index 111	PASS
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.3#3	PASS
		Soft Reset message validation - TEST.PD.PROT.ALL.3#4	PASS
		UUT Request message check - TEST.PD.PROT.ALL.3#5 >>DUT sent Request message at protocol index: 150	PASS
		Source Capabilities message validation - TEST.PD.PROT.ALL.3#6	PASS
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.3#8 >>DUT responded with SinkCap to Get_Sink_Cap at protocol index : 163	PASS
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.3#9	PASS
		Rev2Src	PASS
		GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.3#2	PASS
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.3#3 >>UUT is a DRP and it sent SinkCap message at the protocol index 214	PASS
		Soft Reset message validation - TEST.PD.PROT.ALL.3#4	PASS
		UUT Request message check - TEST.PD.PROT.ALL.3#5	PASS
		Source Capabilities message validation - TEST.PD.PROT.ALL.3#6 >>SourceCap message at protocol index: 244 received within the 250ms	PASS
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.3#8	PASS

SI No	Test ID	Test Name	Test Result
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.3#9 >>DUT responded with SinkCap to Get_Sink_Cap at protocol index : 255	PASS
		Rev3ChkdSrc	PASS
		GetSinkCap response Sink UUT - TEST.PD.PROT.ALL.3#2	PASS
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.3#3 >>UUT is a DRP and it sent SinkCap message at the protocol index 303	PASS
		Soft Reset message validation - TEST.PD.PROT.ALL.3#4	PASS
		UUT Request message check - TEST.PD.PROT.ALL.3#5	PASS
		Source Capabilities message validation - TEST.PD.PROT.ALL.3#6 >>SourceCap message at protocol index: 333 received within the 250ms	PASS
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.3#8	PASS
		GetSinkCap response Source UUT - TEST.PD.PROT.ALL.3#9 >>DUT responded with SinkCap to Get_Sink_Cap at protocol index : 344	PASS
14	TEST.PD.PROT.ALL.4	TEST.PD.PROT.ALL.4 Reset Signals and MessageID	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk >>SourceCap Packet14	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet16	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet87	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet89	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 11.515s and SourceCap time: 11.577s at protocol index #218 [PASS] Max = 250ms. Obtained time difference is 62.494ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 > Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS

SI No	Test ID	Test Name	Test Result
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 16.188s and SourceCap time: 16.25s at protocol index #324 [PASS] Max = 250ms. Obtained time difference is 62.494ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		Rev2Snk >> Tester sent Hard_Reset message Packet 49	PASS
		Get Sink Cap response check - TEST.PD.PROT.ALL.4#2 >>UUT initiated SinkCap for tester initiated Get_Sink_Capability, at protocol index 31	PASS
		UUT Request check - TEST.PD.PROT.ALL.4#4 >>UUT Responded with Request message at protocol index 54	PASS
		Get Sink Cap response check - TEST.PD.PROT.ALL.4#9 >>UUT initiated SinkCap for tester initiated Get_Sink_Capability, at protocol index 63	PASS
		Get Sink Cap response check - TEST.PD.PROT.ALL.4#11 >>UUT ignored tester initiated Get_Sink_Capability at protocol index 66	PASS
		Get Sink Cap response check - TEST.PD.PROT.ALL.4#13 >>UUT initiated SinkCap for tester initiated Get_Sink_Capability, at protocol index 71	PASS
		Rev3ChkdSnk >> Tester sent Hard_Reset message Packet 148	PASS
		Get Sink Cap response check - TEST.PD.PROT.ALL.4#2 >>UUT initiated SinkCap for tester initiated Get_Sink_Capability, at protocol index 125	PASS
		UUT Request check - TEST.PD.PROT.ALL.4#4 >>UUT Responded with Request message at protocol index 156	PASS

SI No	Test ID	Test Name	Test Result
		Get Sink Cap response check - TEST.PD.PROT.ALL.4#9 >>UUT initiated SinkCap for tester initiated Get_Sink_Capability, at protocol index 175	PASS
		Get Sink Cap response check - TEST.PD.PROT.ALL.4#11 >>UUT ignored tester initiated Get_Sink_Capability at protocol index 183	PASS
		Get Sink Cap response check - TEST.PD.PROT.ALL.4#13 >>UUT initiated SinkCap for tester initiated Get_Sink_Capability, at protocol index 193	PASS
		Rev2Src >> Tester sent Hard_Reset message Packet 270	PASS
		Get Sink Cap response check - TEST.PD.PROT.ALL.4#3 >>UUT is a DRP and sent SinkCap at the protocol index 248	PASS
		HardReset response check - TEST.PD.PROT.ALL.4#5	PASS
		Source Capability timing check - TEST.PD.PROT.ALL.4#6 >>DUT initiate first source cap within 250ms. Obtained time difference is 69.1597500000007ms	PASS
		Get Sink Cap response check - TEST.PD.PROT.ALL.4#10 >>UUT is a DRP and sent SinkCap at the protocol index 296	PASS
		Get Sink Cap response check - TEST.PD.PROT.ALL.4#11 >>UUT ignored tester initiated Get_Sink_Capability at protocol index 299	PASS
		Get Sink Cap response check - TEST.PD.PROT.ALL.4#14 >>UUT is a DRP and sent SinkCap at the protocol index 304	PASS
		Rev3ChkdSrc >> Tester sent Hard_Reset message Packet 378	PASS
		Get Sink Cap response check - TEST.PD.PROT.ALL.4#3 >>UUT is a DRP and sent SinkCap at the protocol index 356	PASS
		HardReset response check - TEST.PD.PROT.ALL.4#5	PASS
		Source Capability timing check - TEST.PD.PROT.ALL.4#6 >>DUT initiate first source cap within 250ms. Obtained time difference is 71.6594999999991ms	PASS
		Get Sink Cap response check - TEST.PD.PROT.ALL.4#10 >>UUT is a DRP and sent SinkCap at the protocol index 406	PASS

SI No	Test ID	Test Name	Test Result
		Get Sink Cap response check - TEST.PD.PROT.ALL.4#11 >>UUT ignored tester initiated Get_Sink_Capability at protocol index 409	PASS
		Get Sink Cap response check - TEST.PD.PROT.ALL.4#14 >>UUT is a DRP and sent SinkCap at the protocol index 414	PASS
15	TEST.PD.PROT.ALL.5	TEST.PD.PROT.ALL.5 Unrecognized Message	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk >>SourceCap Packet14	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet16	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet43	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet45	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 7.196s and SourceCap time: 7.258s at protocol index #97 [PASS] Max = 250ms. Obtained time difference is 61.661ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 > Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 9.742s and SourceCap time: 9.804s at protocol index #143 [PASS] Max = 250ms. Obtained time difference is 61.661ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS

SI No	Test ID	Test Name	Test Result
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		Rev2Snk	PASS
		Source or Sink UUT Response Check - TEST.PD.PROT.ALL.5#2 >>DUT responded with Reject message, Packet index : 27	PASS
		Rev3ChkdSnk	PASS
		Source or Sink UUT Response Check - TEST.PD.PROT.ALL.5#2 >>DUT responded with Not_Supported message, Packet index : 71	PASS
		Rev2Src	PASS
		Source or Sink UUT Response Check - TEST.PD.PROT.ALL.5#2 >>DUT responded with Reject message, Packet index : 123	PASS
		Rev3ChkdSrc	PASS
		Source or Sink UUT Response Check - TEST.PD.PROT.ALL.5#2 >>DUT responded with Not_Supported message, Packet index : 171	PASS
16	TEST.PD.PROT.ALL3.1	TEST.PD.PROT.ALL3.1 Get_Status Response	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet15	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet17	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3UnchkdSnk >>SourceCap Packet65	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet67	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 7.354s and SourceCap time: 7.417s at protocol index #119 [PASS] Max = 250ms. Obtained time difference is 63.327ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS

SI No	Test ID	Test Name	Test Result
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 9.945s and SourceCap time: 10.009s at protocol index #167 [PASS] Max = 250ms. Obtained time difference is 63.327ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		Rev3ChkdSnk	PASS
		Get_Status message response check - TEST.PD.PROT.ALL3.1#3 >>DUT sent Status message for the Get_Status at protocol index 44	PASS
		Status message field check - TEST.PD.PROT.ALL3.1#4 >>[PASS] DUTs current port power role is set to Sink and Bits 0-7 should be zeros	PASS
		Rev3UnchkdSnk	PASS
		Get_Status message response check - TEST.PD.PROT.ALL3.1#3 >>DUT sent Status message for the Get_Status at protocol index 94	PASS
		Status message field check - TEST.PD.PROT.ALL3.1#4 >>[PASS] DUTs current port power role is set to Sink and Bits 0-7 should be zeros	PASS
		Rev3ChkdSrc	PASS
		Get_Status message response check - TEST.PD.PROT.ALL3.1#3 >>DUT sent Status message for the Get_Status at protocol index 147	PASS
		Status message field check - TEST.PD.PROT.ALL3.1#4	PASS
		Rev3UnchkdSrc	PASS
		Get_Status message response check - TEST.PD.PROT.ALL3.1#3 >>DUT sent Status message for the Get_Status at protocol index 195	PASS
		Status message field check - TEST.PD.PROT.ALL3.1#4	PASS
17	TEST.PD.PROT.ALL3.2	TEST.PD.PROT.ALL3.2 Get_Manufacturer_Info Response	PASS
		COMMON.PROC.BU.2	PASS

SI No	Test ID	Test Name	Test Result
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet16	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet18	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3UnchkdSnk >>SourceCap Packet65	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet67	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 7.208s and SourceCap time: 7.271s at protocol index #118 [PASS] Max = 250ms. Obtained time difference is 63.327ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 9.758s and SourceCap time: 9.822s at protocol index #166 [PASS] Max = 250ms. Obtained time difference is 64.16ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		Rev3ChkdSnk	NA
		Response Check - TEST.PD.PROT.ALL3.2#2 >>VIF value for Manufacturer_Info_Supported_Port is False but DUT sent Manufacturer_Info to the Get_Manufacturer_Info at ptotocol index 44	NA

SI No	Test ID	Test Name	Test Result
		VIF Check - TEST.PD.PROT.ALL3.2#3 >VIF value for Manufacturer_Info_VID_Port Please load the right VIF and try again VIF value for Manufacturer_Info_PID_Port is missing. Please load the right VIF and try again DUT Manufacture info VID value matching with VI file MANUFACTURER_INFO_VID field DUT decoded VID is 0x29cf and mentioned in VIF is 0x29cf DUT Manufacture info PID value matching with VI file MANUFACTURER_INFO_PID field DUT decoded PID is 0x6375 and mentioned in VIF is 0x6375	NA
		Rev3UnchkdSnk	NA
		Response Check - TEST.PD.PROT.ALL3.2#2 >>VIF value for Manufacturer_Info_Supported_Port is False but DUT sent Manufacturer_Info to the Get_Manufacturer_Info at ptotocol index 93	NA
		VIF Check - TEST.PD.PROT.ALL3.2#3 >>VIF value for Manufacturer_Info_VID_Port is missing. Please load the right VIF and try again VIF value for Manufacturer_Info_PID_Port . Please load the right VIF and try again DUT Manufacture info VID value matching with VI file MANUFACTURER_INFO_VID field DUT decoded VID is 0x29cf and mentioned in VIF is 0x29cf DUT Manufacture info PID value matching with VI file MANUFACTURER_INFO_PID field DUT decoded PID is 0x6375 and mentioned in VIF is 0x6375	NA
		Rev3ChkdSrc	NA
		Response Check - TEST.PD.PROT.ALL3.2#2 >>VIF value for Manufacturer_Info_Supported_Port is False but DUT sent Manufacturer_Info to the Get_Manufacturer_Info at ptotocol index 146	NA

SI No	Test ID	Test Name	Test Result
		VIF Check - TEST.PD.PROT.ALL3.2#3 >VIF value for Manufacturer_Info_VID_Port . Please load the right VIF and try again VIF value for Manufacturer_Info_PID_Port is missing. Please load the right VIF and try again DUT Manufacture info VID value matching with VI file MANUFACTURER_INFO_VID field DUT decoded VID is 0x29cf and mentioned in VIF is 0x29cf DUT Manufacture info PID value matching with VI file MANUFACTURER_INFO_PID field DUT decoded PID is 0x6375 and mentioned in VIF is 0x6375	NA
		Rev3UnchkdSrc	NA
		Response Check - TEST.PD.PROT.ALL3.2#2 >>VIF value for Manufacturer_Info_Supported_Port is False but DUT sent Manufacturer_Info to the Get_Manufacturer_Info at ptotocol index 194	NA
		VIF Check - TEST.PD.PROT.ALL3.2#3 >VIF value for Manufacturer_Info_VID_Port . Please load the right VIF and try again VIF value for Manufacturer_Info_PID_Port is missing. Please load the right VIF and try again DUT Manufacture info VID value matching with VI file MANUFACTURER_INFO_VID field DUT decoded VID is 0x29cf and mentioned in VIF is 0x29cf DUT Manufacture info PID value matching with VI file MANUFACTURER_INFO_PID field DUT decoded PID is 0x6375 and mentioned in VIF is 0x6375	NA
18	TEST.PD.PROT.ALL3.3	TEST.PD.PROT.ALL3.3 Invalid Manufacturer Info Target	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet15	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet17	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3UnchkdSnk >>SourceCap Packet64	PASS

SI No	Test ID	Test Name	Test Result
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet66	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 7.25s and SourceCap time: 7.313s at protocol index #117 [PASS] Max = 250ms. Obtained time difference is 63.327ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 9.796s and SourceCap time: 9.86s at protocol index #165 [PASS] Max = 250ms. Obtained time difference is 63.327ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		Rev3ChkdSnk	PASS
		Response Check - TEST.PD.PROT.ALL3.3#2 >>DUT sent Manufacturer_Info message for the Get_Manufacturer_Info at protocol index #43	PASS
		Manufacturer String Check - TEST.PD.PROT.ALL3.3#3 >>DUT manufacture info string matched with specified format	PASS
		Rev3UnchkdSnk	PASS
		Response Check - TEST.PD.PROT.ALL3.3#2 >>DUT sent Manufacturer_Info message for the Get_Manufacturer_Info at protocol index #92	PASS

SI No	Test ID	Test Name	Test Result
		Manufacturer String Check - TEST.PD.PROT.ALL3.3#3 >>DUT manufacture info string matched with specified format	PASS
		Rev3ChkdSrc	PASS
		Response Check - TEST.PD.PROT.ALL3.3#2 >>DUT sent Manufacturer_Info message for the Get_Manufacturer_Info at protocol index #145	PASS
		Manufacturer String Check - TEST.PD.PROT.ALL3.3#3 >>DUT manufacture info string matched with specified format	PASS
		Rev3UnchkdSrc	PASS
		Response Check - TEST.PD.PROT.ALL3.3#2 >>DUT sent Manufacturer_Info message for the Get_Manufacturer_Info at protocol index #193	PASS
		Manufacturer String Check - TEST.PD.PROT.ALL3.3#3 >>DUT manufacture info string matched with specified format	PASS
19	TEST.PD.PROT.ALL3.4	TEST.PD.PROT.ALL3.4 Invalid Manufacturer Info Ref	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet15	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet17	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3UnchkdSnk >>SourceCap Packet64	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet66	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 7.247s and SourceCap time: 7.311s at protocol index #117 [PASS] Max = 250ms. Obtained time difference is 63.327ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS

SI No	Test ID	Test Name	Test Result
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 9.791s and SourceCap time: 9.855s at protocol index #165 [PASS] Max = 250ms. Obtained time difference is 64.16ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		Rev3ChkdSnk	PASS
		Response Check - TEST.PD.PROT.ALL3.4#2 >>DUT sent Manufacturer_Info message for the Get_Manufacturer_Info	PASS
		Manufacturer String Check - TEST.PD.PROT.ALL3.4#3 >>DUT manufacture info string matched with specified format	PASS
		Rev3UnchkdSnk	PASS
		Response Check - TEST.PD.PROT.ALL3.4#2 >>DUT sent Manufacturer_Info message for the Get_Manufacturer_Info	PASS
		Manufacturer String Check - TEST.PD.PROT.ALL3.4#3 >>DUT manufacture info string matched with specified format	PASS
		Rev3ChkdSrc	PASS
		Response Check - TEST.PD.PROT.ALL3.4#2 >>DUT sent Manufacturer_Info message for the Get_Manufacturer_Info	PASS
		Manufacturer String Check - TEST.PD.PROT.ALL3.4#3 >>DUT manufacture info string matched with specified format	PASS
		Rev3UnchkdSrc	PASS
		Response Check - TEST.PD.PROT.ALL3.4#2 >>DUT sent Manufacturer_Info message for the Get_Manufacturer_Info	PASS
		Manufacturer String Check - TEST.PD.PROT.ALL3.4#3 >>DUT manufacture info string matched with specified format	PASS
20	TEST.PD.PROT.ALL3.5	TEST.PD.PROT.ALL3.5 Chunked Extended Message Response	PASS
		COMMON.PROC.BU.2	PASS

SI No	Test ID	Test Name	Test Result
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet15	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet17	PASS
		Rev3ChkdSnk	PASS
		Chunk Response - TEST.PD.PROT.ALL3.5#2 >UUT respond with Supported and the VIF value for Chunking_Implemented is True [PASS]UUT sent Not_Supported mesage Obtained time difference is 46.415ms, Expected time limit 40ms to 50ms	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 4.516s and SourceCap time: 4.582s at protocol index #69 [PASS] Max = 250ms. Obtained time difference is 65.827ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm failure	PASS
		Rev3ChkdSrc	PASS
		Chunk Response - TEST.PD.PROT.ALL3.5#2 >UUT respond with Supported and the VIF value for Chunking_Implemented is True [PASS]UUT sent Not_Supported mesage Obtained time difference is 45.963ms, Expected time limit 40ms to 50ms	PASS
21	TEST.PD.PROT.ALL3.6	TEST.PD.PROT.ALL3.6 ChunkSenderResponseTimer Timeout	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet15	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet17	PASS
		Rev3ChkdSnk	PASS

SI No	Test ID	Test Name	Test Result
		Chunk Response - TEST.PD.PROT.ALL3.6#2 >>UUT respond with Not_Supported for the Tester initiated Chunk extended message at protocol index: 43 [PASS]UUT sent Not_Supported message Obtained time difference is 47.945ms, Expected time limit 40ms to 50ms	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 4.418s and SourceCap time: 4.48s at protocol index #69 [PASS] Max = 250ms. Obtained time difference is 62.494ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		Rev3ChkdSrc	PASS
		Chunk Response - TEST.PD.PROT.ALL3.6#2 >>UUT respond with Not_Supported for the Tester initiated Chunk extended message at protocol index: 97 [PASS]UUT sent Not_Supported message Obtained time difference is 45.993ms, Expected time limit 40ms to 50ms	PASS
22	TEST.PD.PROT.ALL3.7	TEST.PD.PROT.ALL3.7 Security Messages Supported	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet15	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet17	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3UnchkdSnk >>SourceCap Packet66	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet68	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS

SI No	Test ID	Test Name	Test Result
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 8.342s and SourceCap time: 8.405s at protocol index #120 [PASS] Max = 250ms. Obtained time difference is 63.327ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 11.448s and SourceCap time: 11.512s at protocol index #168 [PASS] Max = 250ms. Obtained time difference is 64.16ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		Rev3ChkdSnk	PASS
		Security Request message response check - TEST.PD.PROT.ALL3.7#1 >>VIF field Security_Msgs_Supported_SOP is No. and UUT respond with Not_Supported message at protocol index 43	PASS
		Rev3UnchkdSnk	PASS
		Security Request message response check - TEST.PD.PROT.ALL3.7#1 >>VIF field Security_Msgs_Supported_SOP is No. and UUT respond with Not_Supported message at protocol index 94	PASS
		Rev3ChkdSrc	PASS
		Security Request message response check - TEST.PD.PROT.ALL3.7#1 >>VIF field Security_Msgs_Supported_SOP is No. and UUT respond with Not_Supported message at protocol index 148	PASS
		Rev3UnchkdSrc	PASS
		Security Request message response check - TEST.PD.PROT.ALL3.7#1 >>VIF field Security_Msgs_Supported_SOP is No. and UUT respond with Not_Supported message at protocol index 196	PASS

SI No	Test ID	Test Name	Test Result
23	TEST.PD.PROT.ALL3.8	TEST.PD.PROT.ALL3.8 Get Revision Response	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet15	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet17	PASS
		Rev3ChkdSnk	PASS
		Get_Revision response check - TEST.PD.PROT.ALL3.8#1 >UUT responded with Supported message for Tester's Get_Revision message	PASS
		Revision message details check - TEST.PD.PROT.ALL3.8#2	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 4.15s and SourceCap time: 4.213s at protocol index #69 [PASS] Max = 250ms. Obtained time difference is 63.327ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		Rev3ChkdSrc	PASS
		Get_Revision response check - TEST.PD.PROT.ALL3.8#1 >>UUT responded with Not_Supported message for Tester's Get_Revision message	PASS
		Revision message details check - TEST.PD.PROT.ALL3.8#2	PASS
24	TEST.PD.PROT.PORT3.1	TEST.PD.PROT.PORT3.1 Get Battery Status Response	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet15	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet17	PASS
		Rev3ChkdSnk	PASS

SI No	Test ID	Test Name	Test Result
		Get_Sink_Cap_Ext response check - TEST.PD.PROT.PORT3.1#1 >UUT respond Supported to Get_Sink_Cap_Ext message	PASS
		Get_Battery_Status response check - TEST.PD.PROT.PORT3.1#2 >>UUT respond Battery_Status PD Message.Packet54 UUT respond Battery_Status PD Message.Packet59 UUT respond Battery_Status PD Message.Packet64 UUT respond Battery_Status PD Message.Packet69 UUT respond Battery_Status PD Message.Packet74 UUT respond Battery_Status PD Message.Packet79 UUT respond Battery_Status PD Message.Packet84 UUT respond Battery_Status PD Message.Packet89	PASS

[illegible]

SI No	Test ID	Test Name	Test Result
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 4.275s and SourceCap time: 4.339s at protocol index #110 [PASS] Max = 250ms. Obtained time difference is 63.327ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 > Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		Rev3ChkdSrc	PASS
		Get_SourceCap_Extended response check - TEST.PD.PROT.PORT3.1#1 >>UUT respond Source_Cap_Extended to Get_SourceCap_Extended message	PASS
		Get_Battery_Status response check - TEST.PD.PROT.PORT3.1#2 >>UUT respond Battery_Status PD Message.Packet143 UUT respond Battery_Status PD Message.Packet148 UUT respond Battery_Status PD Message.Packet153 UUT respond Battery_Status PD Message.Packet158 UUT respond Battery_Status PD Message.Packet163 UUT respond Battery_Status PD Message.Packet168 UUT respond Battery_Status PD Message.Packet173 UUT respond Battery_Status PD Message.Packet178	PASS

SI No	Test ID	Test Name	Test Result
		Battery_Status message check - TEST.PD.PROT.PORT3.1#4 >>[PASS]Battery Info Field : BSDO bits zero [PASS]Battery Info Field : Reserved bits zero UUT responded with Source_Cap_Extended to Get_SourceCap_Extended message. [PASS]The values of VIF fields Num_Fixed_Batteries(Expected) : 1, Fixed_Batteries(Obtained) : 1 Num_Swappable_Battery_Slots(Expected) : 0, Hot_Swap_Batteries(Obtained) : 0 [PASS]In BSDO Invalid Battery Reference bit[0] is 0.Battery present bit[1] is 1.In GBSDB Battery status ref field is 0 [PASS]In BSDO Battery present bit[1] is 1.Battery charging status bit[3:2] is 1 [PASS]Battery Info Field : BSDO bits zero [PASS]Battery Info Field : Reserved bits zero UUT responded with Source_Cap_Extended to Get_SourceCap_Extended message. [PASS]The values of VIF fields Num_Fixed_Batteries(Expected) : 1, Fixed_Batteries(Obtained) : 1 Num_Swappable_Battery_Slots(Expected) : 0, Hot_Swap_Batteries(Obtained) : 0 [PASS]In BSDO Invalid Battery Reference bit[0] is 1.Battery present bit[1] is 0.Battery charging status bit[3:2] is 0 [PASS]In BSDO Battery present bit[1] is 0.Battery charging status bit[3:2] is 0 [PASS]Battery Info Field : BSDO bits zero [PASS]Battery Info Field : Reserved bits zero UUT responded with Source_Cap_Extended to Get_SourceCap_Extended message. [PASS]The values of VIF fields Num_Fixed_Batteries(Expected) : 1, Fixed_Batteries(Obtained) : 1 Num_Swappable_Battery_Slots(Expected) : 0, Hot_Swap_Batteries(Obtained) : 0 [PASS]In BSDO Invalid Battery Reference bit[0] is 1.Battery present bit[1] is 0.Battery charging status bit[3:2] is 0 [PASS]In BSDO Battery present bit[1] is 0.Battery charging status bit[3:2] is 0 [PASS]Battery Info Field : BSDO bits zero [PASS]Battery Info Field : Reserved bits zero UUT responded with Source_Cap_Extended to Get_SourceCap_Extended message.	PASS
This report is generated using QTS Test Automation Framework v6.7.0-rc1f7c1e3449dda8c6f1136fe3b3788240412)	(Date: 2025-06-15 16:34:09)	[PASS]Battery Info Field : Reserved bits zero UUT responded with Source_Cap_Extended to Get_SourceCap_Extended message. [PASS]The values of VIF fields Num_Fixed_Batteries(Expected) : 1,	Page: 39

SI No	Test ID	Test Name	Test Result
25	TEST.PD.PROT.PORT3.2	TEST.PD.PROT.PORT3.2 Invalid Battery Status	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet15	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet17	PASS
		Rev3ChkdSnk	PASS
		Get_Sink_Cap_Ext response check - TEST.PD.PROT.PORT3.2#1 >UUT respond Supported to Get_Sink_Cap_Ext message	PASS
		Battery_Status message check - TEST.PD.PROT.PORT3.2#4 >>Battery Info Field : BSDO bits are zero In Battery_Status message Invalid_Battery_Ref field is correct. Battery_Info field is correct from 1 to 7 bits.	PASS
		Get_Battery_Status response check - TEST.PD.PROT.PORT3.2#2 >>UUT respond Battery_Status to Get_Battery_Status message	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 4.45s and SourceCap time: 4.513s at protocol index #79 [PASS] Max = 250ms. Obtained time difference is 62.494ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		Rev3ChkdSrc	PASS
		Get_SourceCap_Extended response check - TEST.PD.PROT.PORT3.2#1 >>UUT respond Source_Cap_Extended to Get_SourceCap_Extended message	PASS
		Battery_Status message check - TEST.PD.PROT.PORT3.2#4 >>Battery Info Field : BSDO bits are zero In Battery_Status message Invalid_Battery_Ref field is correct. Battery_Info field is correct from 1 to 7 bits.	PASS

SI No	Test ID	Test Name	Test Result
		Get_Battery_Status response check - TEST.PD.PROT.PORT3.2#2 >>UUT respond Battery_Status to Get_Battery_Status message	PASS
26	TEST.PD.PROT.PORT3.3	TEST.PD.PROT.PORT3.3 Get Battery Cap Response	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet15	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet17	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3UnchkdSnk >>SourceCap Packet145	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet147	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 12.163s and SourceCap time: 12.226s at protocol index #279 [PASS] Max = 250ms. Obtained time difference is 63.327ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 > Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc >>Tester failed to initiate request	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 17.117s and SourceCap time: 17.182s at protocol index #367 [PASS] Max = 250ms. Obtained time difference is 64.994ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		Rev3ChkdSnk	PASS

SI No	Test ID	Test Name	Test Result
		Get_Sink_Cap_Ext check - TEST.PD.PROT.PORT3.3#1 >UUT respond Supported to Get_Sink_Cap_Ext message	PASS
		Get_Battery_Cap check - TEST.PD.PROT.PORT3.3#2	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#0 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#1 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#2 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#3 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#4 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#5 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS

SI No	Test ID	Test Name	Test Result
		Get_Battery_Cap check for Battery_Cap_Ref_#6 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#7 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Battery_Capabilities check - TEST.PD.PROT.PORT3.3#3	PASS
		Battery_Capabilities check for Battery_Cap_Ref_#0 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 0 at protocol index 54 Battery type bit[1..7] is zero	PASS
		Battery_Capabilities check for Battery_Cap_Ref_#1 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 1 at protocol index 64 Battery type bit[1..7] is zero	PASS
		Battery_Capabilities check for Battery_Cap_Ref_#2 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 1 at protocol index 74 Battery type bit[1..7] is zero	PASS
		Battery_Capabilities check for Battery_Cap_Ref_#3 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 1 at protocol index 84 Battery type bit[1..7] is zero	PASS
		Battery_Capabilities check for Battery_Cap_Ref_#4 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 1 at protocol index 94 Battery type bit[1..7] is zero	PASS

SI No	Test ID	Test Name	Test Result
		Battery_Capabilities check for Battery_Cap_Ref_#5 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 1 at protocol index 104 Battery type bit[1..7] is zero	PASS
		Battery_Capabilities check for Battery_Cap_Ref_#6 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 1 at protocol index 114 Battery type bit[1..7] is zero	PASS
		Battery_Capabilities check for Battery_Cap_Ref_#7 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 1 at protocol index 124 Battery type bit[1..7] is zero	PASS
		Rev3UnchkdSnk	PASS
		Get_Sink_Cap_Ext check - TEST.PD.PROT.PORT3.3#1 >UUT respond Supported to Get_Sink_Cap_Ext message	PASS
		Get_Battery_Cap check - TEST.PD.PROT.PORT3.3#2	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#0 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#1 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#2 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS

SI No	Test ID	Test Name	Test Result
		Get_Battery_Cap check for Battery_Cap_Ref_#3 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#4 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#5 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#6 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#7 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Battery_Capabilities check - TEST.PD.PROT.PORT3.3#3	PASS
		Battery_Capabilities check for Battery_Cap_Ref_#0 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 0 at protocol index 184 Battery type bit[1..7] is zero	PASS
		Battery_Capabilities check for Battery_Cap_Ref_#1 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 1 at protocol index 194 Battery type bit[1..7] is zero	PASS

SI No	Test ID	Test Name	Test Result
		Battery_Capabilities check for Battery_Cap_Ref_#2 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 1 at protocol index 204 Battery type bit[1..7] is zero	PASS
		Battery_Capabilities check for Battery_Cap_Ref_#3 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 1 at protocol index 214 Battery type bit[1..7] is zero	PASS
		Battery_Capabilities check for Battery_Cap_Ref_#4 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 1 at protocol index 224 Battery type bit[1..7] is zero	PASS
		Battery_Capabilities check for Battery_Cap_Ref_#5 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 1 at protocol index 234 Battery type bit[1..7] is zero	PASS
		Battery_Capabilities check for Battery_Cap_Ref_#6 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 1 at protocol index 244 Battery type bit[1..7] is zero	PASS
		Battery_Capabilities check for Battery_Cap_Ref_#7 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 1 at protocol index 254 Battery type bit[1..7] is zero	PASS
		Rev3ChkdSrc	PASS
		Get_SourceCap_Extended check - TEST.PD.PROT.PORT3.3#1 >>UUT respond Source_Cap_Extended to Get_SourceCap_Extended message	PASS
		Get_Battery_Cap check - TEST.PD.PROT.PORT3.3#2	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#0 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS

SI No	Test ID	Test Name	Test Result
		Get_Battery_Cap check for Battery_Cap_Ref_#1 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#2 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#3 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#4 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#5 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#6 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS

SI No	Test ID	Test Name	Test Result
		Get_Battery_Cap check for Battery_Cap_Ref_#7 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Battery_Capabilities check - TEST.PD.PROT.PORT3.3#3	PASS
		Battery_Capabilities check for Battery_Cap_Ref_#0 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 0 at protocol index 312 Battery type bit[1..7] is zero	PASS
		Battery_Capabilities check for Battery_Cap_Ref_#1 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 1 at protocol index 317 Battery type bit[1..7] is zero	PASS
		Battery_Capabilities check for Battery_Cap_Ref_#2 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 1 at protocol index 322 Battery type bit[1..7] is zero	PASS
		Battery_Capabilities check for Battery_Cap_Ref_#3 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 1 at protocol index 327 Battery type bit[1..7] is zero	PASS
		Battery_Capabilities check for Battery_Cap_Ref_#4 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 1 at protocol index 332 Battery type bit[1..7] is zero	PASS
		Battery_Capabilities check for Battery_Cap_Ref_#5 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 1 at protocol index 337 Battery type bit[1..7] is zero	PASS
		Battery_Capabilities check for Battery_Cap_Ref_#6 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 1 at protocol index 342 Battery type bit[1..7] is zero	PASS

SI No	Test ID	Test Name	Test Result
		Battery_Capabilities check for Battery_Cap_Ref_#7 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 1 at protocol index 347 Battery type bit[1..7] is zero	PASS
		Rev3UnchkdSrc	PASS
		Get_SourceCap_Extended check - TEST.PD.PROT.PORT3.3#1 >>UUT respond Source_Cap_Extended to Get_SourceCap_Extended message	PASS
		Get_Battery_Cap check - TEST.PD.PROT.PORT3.3#2	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#0 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#1 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#2 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#3 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#4 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS

SI No	Test ID	Test Name	Test Result
		Get_Battery_Cap check for Battery_Cap_Ref_#5 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#6 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Get_Battery_Cap check for Battery_Cap_Ref_#7 - TEST.PD.PROT.PORT3.3#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message The values of VIF fields Num_Fixed_Batteries is 1 and Num_Swappable_Battery_Slots is 0	PASS
		Battery_Capabilities check - TEST.PD.PROT.PORT3.3#3	PASS
		Battery_Capabilities check for Battery_Cap_Ref_#0 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 0 at protocol index 400 Battery type bit[1..7] is zero	PASS
		Battery_Capabilities check for Battery_Cap_Ref_#1 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 1 at protocol index 405 Battery type bit[1..7] is zero	PASS
		Battery_Capabilities check for Battery_Cap_Ref_#2 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 1 at protocol index 410 Battery type bit[1..7] is zero	PASS
		Battery_Capabilities check for Battery_Cap_Ref_#3 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 1 at protocol index 415 Battery type bit[1..7] is zero	PASS

SI No	Test ID	Test Name	Test Result
		Battery_Capabilities check for Battery_Cap_Ref_#4 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 1 at protocol index 420 Battery type bit[1..7] is zero	PASS
		Battery_Capabilities check for Battery_Cap_Ref_#5 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 1 at protocol index 425 Battery type bit[1..7] is zero	PASS
		Battery_Capabilities check for Battery_Cap_Ref_#6 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 1 at protocol index 430 Battery type bit[1..7] is zero	PASS
		Battery_Capabilities check for Battery_Cap_Ref_#7 - TEST.PD.PROT.PORT3.3#3 >>Obtained Invalid Battery Reference field value: 1 at protocol index 435 Battery type bit[1..7] is zero	PASS
27	TEST.PD.PROT.PORT3.4	TEST.PD.PROT.PORT3.4 Invalid Battery Capabilities Reference	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet15	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet17	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3UnchkdSnk >>SourceCap Packet75	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet77	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 7.895s and SourceCap time: 7.958s at protocol index #139 [PASS] Max = 250ms. Obtained time difference is 63.327ms	PASS

SI No	Test ID	Test Name	Test Result
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 10.743s and SourceCap time: 10.806s at protocol index #192 [PASS] Max = 250ms. Obtained time difference is 63.327ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		Rev3ChkdSnk	PASS
		Get_Sink_Cap_Ext check - TEST.PD.PROT.PORT3.4#1 >UUT respond Supported to Get_Sink_Cap_Ext message	PASS
		Get_Battery_Cap check - TEST.PD.PROT.PORT3.4#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message	PASS
		Battery_Capabilities check - TEST.PD.PROT.PORT3.4#3 >>[15:0] Vendor_ID field Exp:0xFFFF but Obt:0xFFFF [Bit 0]:Invalid battery reference field is 0 [Bit 1..7]:Battery type bit is 1	PASS
		Rev3UnchkdSnk	PASS
		Get_Sink_Cap_Ext check - TEST.PD.PROT.PORT3.4#1 >>UUT respond Not_Supported to Get_Sink_Cap_Ext message	PASS
		Get_Battery_Cap check - TEST.PD.PROT.PORT3.4#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message	PASS
		Battery_Capabilities check - TEST.PD.PROT.PORT3.4#3 >>[15:0] Vendor_ID field Exp:0xFFFF but Obt:0xFFFF [Bit 0]:Invalid battery reference field is 0 [Bit 1..7]:Battery type bit is 1	PASS
		Rev3ChkdSrc	PASS

SI No	Test ID	Test Name	Test Result
		Get_SourceCap_Extended check - TEST.PD.PROT.PORT3.4#1 >>UUT respond Source_Cap_Extended to Get_SourceCap_Extended message	PASS
		Get_Battery_Cap check - TEST.PD.PROT.PORT3.4#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message	PASS
		Battery_Capabilities check - TEST.PD.PROT.PORT3.4#3 >>[15:0] Vendor_ID field Exp:0xFFFF but Obt:0xFFFF [Bit 0]:Invalid battery reference field is 0 [Bit 1..7]:Battery type bit is 1	PASS
		Rev3UnchkdSrc	PASS
		Get_SourceCap_Extended check - TEST.PD.PROT.PORT3.4#1 >>UUT respond Source_Cap_Extended to Get_SourceCap_Extended message	PASS
		Get_Battery_Cap check - TEST.PD.PROT.PORT3.4#2 >>UUT respond Battery_Capabilities to Get_Battery_Cap message	PASS
		Battery_Capabilities check - TEST.PD.PROT.PORT3.4#3 >>[15:0] Vendor_ID field Exp:0xFFFF but Obt:0xFFFF [Bit 0]:Invalid battery reference field is 0 [Bit 1..7]:Battery type bit is 1	PASS
28	TEST.PD.PROT.PORT3.5	TEST.PD.PROT.PORT3.5 Get Country Codes Response	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet15	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet17	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3UnchkdSnk >>SourceCap Packet65	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet67	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS

SI No	Test ID	Test Name	Test Result
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 7.764s and SourceCap time: 7.827s at protocol index #119 [PASS] Max = 250ms. Obtained time difference is 63.327ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 10.568s and SourceCap time: 10.631s at protocol index #167 [PASS] Max = 250ms. Obtained time difference is 62.494ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		Rev3ChkdSnk	PASS
		Country_Codes check - TEST.PD.PROT.PORT3.5#1 >>UUT respond Not_Supported to Get_Country_Codes message	PASS
		Rev3UnchkdSnk	PASS
		Country_Codes check - TEST.PD.PROT.PORT3.5#1 >>UUT respond Not_Supported to Get_Country_Codes message	PASS
		Rev3ChkdSrc	PASS
		Country_Codes check - TEST.PD.PROT.PORT3.5#1 >>UUT respond Not_Supported to Get_Country_Codes message	PASS
		Rev3UnchkdSrc	PASS
		Country_Codes check - TEST.PD.PROT.PORT3.5#1 >>UUT respond Not_Supported to Get_Country_Codes message	PASS
29	TEST.PD.PROT.PORT3.6	TEST.PD.PROT.PORT3.6 Get Country Info Response	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet15	PASS

SI No	Test ID	Test Name	Test Result
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet17	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3UnchkdSnk >>SourceCap Packet65	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet67	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 7.772s and SourceCap time: 7.837s at protocol index #119 [PASS] Max = 250ms. Obtained time difference is 64.16ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 10.575s and SourceCap time: 10.638s at protocol index #167 [PASS] Max = 250ms. Obtained time difference is 63.327ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		Rev3ChkdSnk	PASS
		Country_Codes check - TEST.PD.PROT.PORT3.6#1 >>UUT respond Not_Supported to Get_Country_Codes message	PASS
		Rev3UnchkdSnk	PASS
		Country_Codes check - TEST.PD.PROT.PORT3.6#1 >>UUT respond Not_Supported to Get_Country_Codes message	PASS
		Rev3ChkdSrc	PASS

SI No	Test ID	Test Name	Test Result
		Country_Codes check - TEST.PD.PROT.PORT3.6#1 >>UUT respond Not_Supported to Get_Country_Codes message	PASS
		Rev3UnchkdSrc	PASS
		Country_Codes check - TEST.PD.PROT.PORT3.6#1 >>UUT respond Not_Supported to Get_Country_Codes message	PASS
30	TEST.PD.PROT.PORT3.7	TEST.PD.PROT.PORT3.7 Unchunked Extended Message Supported	NA
		--- In VIF Unchunked_Extended_Messages_Supported field is NO	
31	TEST.PD.PROT.SRC.1	TEST.PD.PROT.SRC.1 Get_Source_Cap Response	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.109s and SourceCap time: 1.171s at protocol index #19 [PASS] Max = 250ms. Obtained time difference is 61.661ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 > Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 4.194s and SourceCap time: 4.258s at protocol index #72 [PASS] Max = 250ms. Obtained time difference is 64.16ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 > Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		Rev2Src	PASS
		Source_Cap message check - TEST.PD.PROT.SRC.1#1 >>UUT is successfully respond to Get_Source_Cap message.Protocol index #45	PASS
		Rev3ChkdSrc	PASS

SI No	Test ID	Test Name	Test Result
		Source_Cap message check - TEST.PD.PROT.SRC.1#1 >>UUT is successfully respond to Get_Source_Cap message.Protocol index #100	PASS
32	TEST.PD.PROT.SRC.2	TEST.PD.PROT.SRC.2 Get_Source_Cap No Request	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.166s and SourceCap time: 1.228s at protocol index #19 [PASS] Max = 250ms. Obtained time difference is 61.66ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 5.625s and SourceCap time: 5.689s at protocol index #88 [PASS] Max = 250ms. Obtained time difference is 64.16ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		Rev2Src	PASS
		Source_Cap message check - TEST.PD.PROT.SRC.2#1 >>UUT successfully respond to Get_Source_Cap message.Protocol index #45	PASS
		Hard_Reset message check - TEST.PD.PROT.SRC.2#2 >>UUT responded with Hard_Reset within 0.024~0.03s.Obtained interval is 0.02729s.Protocol index #47	PASS
		Rev3ChkdSrc	PASS

SI No	Test ID	Test Name	Test Result
		Source_Cap message check - TEST.PD.PROT.SRC.2#1 >>UUT successfully respond to Get_Source_Cap message.Protocol index #116	PASS
		Hard_Reset message check - TEST.PD.PROT.SRC.2#2 >>UUT responded with Hard_Reset within 0.027~0.033s.Obtained interval is 0.02742s.Protocol index #118	PASS
33	TEST.PD.PROT.SRC.3	TEST.PD.PROT.SRC.3 Sender Response Timer Deadline	PASS
		Rev2Src	PASS
		tFirstSourceCap timer check - TEST.PD.PROT.SRC.3#1 >>start time: 1.28144179 VBusUp time: 1.09396054s Obt time:0.1875s [PASS] Max = 250ms. Obtained time difference is 187.481ms	PASS
		Request message response check - TEST.PD.PROT.SRC.3#2 >>UUT respond Accept to Request message	PASS
		Rev3ChkdSrc	PASS
		tFirstSourceCap timer check - TEST.PD.PROT.SRC.3#1 >>start time: 4.30023473 VBusUp time: 4.09858822s Obt time:0.2016s [PASS] Max = 250ms. Obtained time difference is 201.647ms	PASS
		Request message response check - TEST.PD.PROT.SRC.3#2 >>UUT respond Accept to Request message	PASS
34	TEST.PD.PROT.SRC.4	TEST.PD.PROT.SRC.4 Reject Request	PASS
		Rev2Src	PASS
		PDO#1	PASS
		tFirstSourceCap timer check - TEST.PD.PROT.SRC.4#1 >>start time: 1.26967435 VBusUp time: 1.07969335s Obt time:0.19s [PASS] Max = 250ms. Obtained time difference is 189.981ms	PASS
		Reject check - TEST.PD.PROT.SRC.4#2 >>UUT sent Reject message at Protocol index 34	PASS
		Rev3ChkdSrc	PASS
		PDO#1	PASS
		tFirstSourceCap timer check - TEST.PD.PROT.SRC.4#1 >>start time: 6.24370612 VBusUp time: 6.05289187s Obt time:0.1908s [PASS] Max = 250ms. Obtained time difference is 190.814ms	PASS
		Reject check - TEST.PD.PROT.SRC.4#2 >>UUT sent Reject message at Protocol index 69	PASS

SI No	Test ID	Test Name	Test Result
35	TEST.PD.PROT.SRC.5	TEST.PD.PROT.SRC.5 Reject Request Invalid Object Position	PASS
		Rev2Src	PASS
		Source_Cap check - TEST.PD.PROT.SRC.5#1 >>start time: 1.21037643 VBusUp time: 1.14871592s Obt time:0.0617s [PASS] Max = 250ms. Obtained time difference is 61.661ms	PASS
		Reject check - TEST.PD.PROT.SRC.5#2 >>UUT sent Reject message at protocol index 34	PASS
		Rev3ChkdSrc	PASS
		Source_Cap check - TEST.PD.PROT.SRC.5#1 >>start time: 6.17152164 VBusUp time: 6.10902789s Obt time:0.0625s [PASS] Max = 250ms. Obtained time difference is 62.494ms	PASS
		Reject check - TEST.PD.PROT.SRC.5#2 >>UUT sent Reject message at protocol index 69	PASS
36	TEST.PD.PROT.SRC.6	TEST.PD.PROT.SRC.6 Atomic Message Sequence – Request	PASS
		Rev2Src	PASS
		tFirstSourceCap timer check - TEST.PD.PROT.SRC.6#1 >>start time: 1.14346578 VBusUp time: 1.08263853s Obt time:0.0608s [PASS] Max = 250ms. Obtained time difference is 60.827ms	PASS
		tProtErrSoftReset timer check - TEST.PD.PROT.SRC.6#2 >>UUT sent SoftReset message received within tSoftReset_Max 0.015s.Protocol index #34	PASS
		tTypeCSinkWaitCap_Max check - TEST.PD.PROT.SRC.6#3 >>UUT sent Source_Cap message after Soft_Reset within tTypeCSinkWaitCap_Max 0.62s.Protocol index #38 Tester sent Accept message	PASS
		Rev3ChkdSrc	PASS
		tFirstSourceCap timer check - TEST.PD.PROT.SRC.6#1 >>start time: 4.1421387 VBusUp time: 4.07964495s Obt time:0.0625s [PASS] Max = 250ms. Obtained time difference is 62.494ms	PASS
		tProtErrSoftReset timer check - TEST.PD.PROT.SRC.6#2 >>UUT sent SoftReset message received within tSoftReset_Max 0.015s.Protocol index #84	PASS

SI No	Test ID	Test Name	Test Result
		tTypeCSinkWaitCap_Max check - TEST.PD.PROT.SRC.6#3 >>UUT sent Source_Cap message after Soft_Reset within tTypeCSinkWaitCap_Max 0.62s.Protocol index #88 Tester sent Accept message	PASS
37	TEST.PD.PROT.SRC.7	TEST.PD.PROT.SRC.7 DR_Swap	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.14s and SourceCap time: 1.202s at protocol index #19 [PASS] Max = 250ms. Obtained time difference is 62.494ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 7.597s and SourceCap time: 7.661s at protocol index #70 [PASS] Max = 250ms. Obtained time difference is 64.16ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		Rev2Src	PASS
		DR_Swap Response Check - TEST.PD.PROT.SRC.7#1 >>UUT respond Accept to DR_Swap message and DR_Swap_To_UFP_Supported field is Yes	PASS
		DR_Swap Response Check - TEST.PD.PROT.SRC.7#2 >>UUT respond Accept to DR_Swap message and DR_Swap_To_DFP_Supported field is Yes	PASS
		Rev3ChkdSrc	PASS

SI No	Test ID	Test Name	Test Result
		DR_Swap Response Check - TEST.PD.PROT.SRC.7#1 >>UUT respond Accept to DR_Swap message and DR_Swap_To_UFP_Supported field is Yes	PASS
		DR_Swap Response Check - TEST.PD.PROT.SRC.7#2 >>UUT respond Accept to DR_Swap message and DR_Swap_To_DFP_Supported field is Yes	PASS
38	TEST.PD.PROT.SRC.8	TEST.PD.PROT.SRC.8 VCONN_Swap Response	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.129s and SourceCap time: 1.192s at protocol index #19 [PASS] Max = 250ms. Obtained time difference is 63.327ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 9.611s and SourceCap time: 9.673s at protocol index #102 [PASS] Max = 250ms. Obtained time difference is 62.494ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		Rev2Src	PASS
		VCONN_Swap response check - TEST.PD.PROT.SRC.8#1 >>UUT respond Accept to VCONN_Swap message at protocol index 45 and VCONN_Swap_To_Off_Supported field is NO	PASS
		tVONNSourceOff timer check - TEST.PD.PROT.SRC.8#2	NA
		Second VCONN_Swap response check - TEST.PD.PROT.SRC.8#3	NA

SI No	Test ID	Test Name	Test Result
		PS_RDY check - TEST.PD.PROT.SRC.8#4	NA
		VCONN present check - TEST.PD.PROT.SRC.8#5	NA
		Third VCONN_Swap response check - TEST.PD.PROT.SRC.8#6	NA
		PS_RDY holding check - TEST.PD.PROT.SRC.8#7	NA
		Rev3ChkdSrc	NA
		VCONN_Swap response check - TEST.PD.PROT.SRC.8#1 >>UUT respond Accept to VCONN_Swap message at protocol index 130 and VCONN_Swap_To_Off Supported field is NO	NA
		tVONNSourceOff timer check - TEST.PD.PROT.SRC.8#2	NA
		Second VCONN_Swap response check - TEST.PD.PROT.SRC.8#3	NA
		PS_RDY check - TEST.PD.PROT.SRC.8#4	NA
		VCONN present check - TEST.PD.PROT.SRC.8#5	NA
		Third VCONN_Swap response check - TEST.PD.PROT.SRC.8#6	NA
		PS_RDY holding check - TEST.PD.PROT.SRC.8#7	NA
39	TEST.PD.PROT.SRC.9	TEST.PD.PROT.SRC.9 PR_Swap Response	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.113s and SourceCap time: 1.176s at protocol index #19 [PASS] Max = 250ms. Obtained time difference is 63.327ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 7.611s and SourceCap time: 7.674s at protocol index #110 [PASS] Max = 250ms. Obtained time difference is 63.327ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS

SI No	Test ID	Test Name	Test Result
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		Rev2Src	PASS
		PR_Swap response check - TEST.PD.PROT.SRC.9#1 >>UUT respond Accept to PR_Swap message.The VIF field PD_Port_Type is DRP.The VIF field Accepts_PR_Swap_As_Src is YES at protocol index 45.	PASS
		UUT PS_RDY vSafe0V check - TEST.PD.PROT.SRC.9#2 >>UUT respond PS_RDY message to PR_Swap after VBUS voltage to vSafe0V(0V - 0.8V).The present voltage is 0.0427V at protocol index 47.	PASS
		tPSSourceOff timer check - TEST.PD.PROT.SRC.9#3 >>UUT respond PS_RDY within tPSSourceOff_Min(750ms) time.The present interval is 0.0473s at protocol index 47. Tester respond PS_RDY message to UUT message within tNewSrc_Max(275ms).The interval is 0.0411s at protocol index 52.	PASS
		PD contract check - TEST.PD.PROT.SRC.9#4 >>UUT respond Request to SourceCap message at protocol index 57.	PASS
		PR_Swap response check - TEST.PD.PROT.SRC.9#5 >>UUT respond Accept to PR_Swap message.The VIF field Accept_PR_Swap_As_Snk is YES.	PASS
		UUT Rp check - TEST.PD.PROT.SRC.9#6 >>UUT asserts Rp at protocol index 72.	PASS
		UUT PSRDY vSafe5V check - TEST.PD.PROT.SRC.9#7 >>UUT respond PS_RDY message to Tester message.The present voltage is 5.0521V	PASS
		tPSSourceOn timer check - TEST.PD.PROT.SRC.9#8 >>UUT respond PS_RDY message to Tester message within tPSSourceOn_Min(390ms).The interval is 0.0755s	PASS
		tFirstSourceCap timer check - TEST.PD.PROT.SRC.9#9 >>[PASS] Min= 20ms - Max = 250ms. Obtained time difference is 68.109ms	PASS
		Rev3ChkdSrc	PASS

SI No	Test ID	Test Name	Test Result
		PR_Swap response check - TEST.PD.PROT.SRC.9#1 >>UUT respond Accept to PR_Swap message.The VIF field PD_Port_Type is DRP.The VIF field Accepts_PR_Swap_As_Src is YES at protocol index 138.	PASS
		UUT PS_RDY vSafe0V check - TEST.PD.PROT.SRC.9#2 >>UUT respond PS_RDY message to PR_Swap after VBUS voltage to vSafe0V(0V - 0.8V).The present voltage is 0.0324V at protocol index 140.	PASS
		tPSSourceOff timer check - TEST.PD.PROT.SRC.9#3 >>UUT respond PS_RDY within tPSSourceOff_Min(750ms) time.The present interval is 0.0477s at protocol index 140. Tester respond PS_RDY message to UUT message within tNewSrc_Max(275ms).The interval is 0.0434s at protocol index 145.	PASS
		PD contract check - TEST.PD.PROT.SRC.9#4 >>UUT respond Request to SourceCap message at protocol index 150.	PASS
		PR_Swap response check - TEST.PD.PROT.SRC.9#5 >>UUT respond Accept to PR_Swap message.The VIF field Accept_PR_Swap_As_Snk is YES.	PASS
		UUT Rp check - TEST.PD.PROT.SRC.9#6 >>UUT asserts Rp at protocol index 175.	PASS
		UUT PSRDY vSafe5V check - TEST.PD.PROT.SRC.9#7 >>UUT respond PS_RDY message to Tester message.The present voltage is 5.0604V	PASS
		tPSSourceOn timer check - TEST.PD.PROT.SRC.9#8 >>UUT respond PS_RDY message to Tester message within tPSSourceOn_Min(390ms).The interval is 0.0757s	PASS
		tFirstSourceCap timer check - TEST.PD.PROT.SRC.9#9 >>[PASS] Min= 20ms - Max = 250ms. Obtained time difference is 77.921ms	PASS
40	TEST.PD.PROT.SRC.10	TEST.PD.PROT.SRC.10 PR_Swap – PSSourceOnTimer Timeout	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src	PASS

SI No	Test ID	Test Name	Test Result
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.07s and SourceCap time: 1.131s at protocol index #19 [PASS] Max = 250ms. Obtained time difference is 60.258ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 5.58s and SourceCap time: 5.644s at protocol index #85 [PASS] Max = 250ms. Obtained time difference is 63.344ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		Rev2Src	PASS
		PR_Swap response check - TEST.PD.PROT.SRC.10#1 >>UUT respond Accept to PR_Swap message.The VIF field PD_Port_Type is set to DRP	PASS
		PS_RDY message check - TEST.PD.PROT.SRC.10#2 >>PS_RDY message recieved at 0.4492 V UUT sent PS_RDY message to PR_Swap response after VBUS voltage is with in vSafe0V(0V-0.8V) UUT sent PS_RDY within tSrcTransition_Max(35ms) + tSrcSwapStdby_Max(650ms) time.The time interval is 0.0462s, start time 2.2914s, stop time 2.3376s	PASS
		Hard_Reset message check - TEST.PD.PROT.SRC.10#3 >>UUT sent Type-C Error Recovery within tPSSourceOn[390ms - 480ms].The time interval is 0.4136s	PASS
		Rev3ChkdSrc	PASS
		PR_Swap response check - TEST.PD.PROT.SRC.10#1 >>UUT respond Accept to PR_Swap message.The VIF field PD_Port_Type is set to DRP	PASS

SI No	Test ID	Test Name	Test Result
		PS_RDY message check - TEST.PD.PROT.SRC.10#2 >>PS_RDY message recieved at 0.422 V UUT sent PS_RDY message to PR_Swap response after VBUS voltage is with in vSafe0V(0V-0.8V) UUT sent PS_RDY within tSrcTransition_Max(35ms) + tSrcSwapStdby_Max(650ms) time.The time interval is 0.0466s, start time 6.801s, stop time 6.8475s	PASS
		Hard_Reset message check - TEST.PD.PROT.SRC.10#3 >>UUT sent Type-C Error Recovery within tPSSourceOn[390ms - 480ms].The time interval is 0.4125s	PASS
41	TEST.PD.PROT.SRC.11	TEST.PD.PROT.SRC.11 Unexpected Message Received in Ready State	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.086s and SourceCap time: 1.149s at protocol index #19 [PASS] Max = 250ms. Obtained time difference is 62.494ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 4.592s and SourceCap time: 4.655s at protocol index #75 [PASS] Max = 250ms. Obtained time difference is 63.327ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		Rev2Src	PASS

SI No	Test ID	Test Name	Test Result
		Soft_Reset check - TEST.PD.PROT.SRC.11#1 >>UUT is sent SoftReset message within tProtErrSoftReset_Max(15ms).The obtained interval is 0.0045s.Protocol index #45	PASS
		Soft_Reset check - TEST.PD.PROT.SRC.11#1 >>UUT is sent SoftReset message within tProtErrSoftReset_Max(15ms).The obtained interval is 0.0045s.Protocol index #45	PASS
		Rev3ChkdSrc	PASS
		Soft_Reset check - TEST.PD.PROT.SRC.11#1 >>UUT is sent SoftReset message within tProtErrSoftReset_Max(15ms).The obtained interval is 0.0049s.Protocol index #103	PASS
		Soft_Reset check - TEST.PD.PROT.SRC.11#1 >>UUT is sent SoftReset message within tProtErrSoftReset_Max(15ms).The obtained interval is 0.0049s.Protocol index #103	PASS
42	TEST.PD.PROT.SRC.12	TEST.PD.PROT.SRC.12 Get_Sink_Cap Response	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.11s and SourceCap time: 1.173s at protocol index #19 [PASS] Max = 250ms. Obtained time difference is 63.327ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 3.617s and SourceCap time: 3.679s at protocol index #65 [PASS] Max = 250ms. Obtained time difference is 62.494ms	PASS

SI No	Test ID	Test Name	Test Result
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		Rev2Src	PASS
		Get_Sink_Cap response check - TEST.PD.PROT.SRC.12#1 >>UUT respond SinkCap to Get_Sink_Cap message.Protocol index #45	PASS
		Rev3ChkdSrc	PASS
		Get_Sink_Cap response check - TEST.PD.PROT.SRC.12#1 >>UUT respond SinkCap to Get_Sink_Cap message.Protocol index #93	PASS
43	TEST.PD.PROT.SRC.13	TEST.PD.PROT.SRC.13 PR Swap GoodCRC not sent in Response to PS_RDY	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.092s and SourceCap time: 1.155s at protocol index #19 [PASS] Max = 250ms. Obtained time difference is 62.494ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 5.652s and SourceCap time: 5.716s at protocol index #87 [PASS] Max = 250ms. Obtained time difference is 63.327ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		Rev2Src	PASS

SI No	Test ID	Test Name	Test Result
		PR_Swap response check - TEST.PD.PROT.SRC.13#1 >>UUT respond Accept to PR_Swap message.The VIF field PD_Port_Type is set to DRP	PASS
		PS_RDY message check - TEST.PD.PROT.SRC.13#2 >>UUT sent PS_RDY message to PR_SWAp response after VBUS voltage to vSafe0V(0V-0.8V).The present voltage is 0.3549V.Protocol index #50 UUT sent PS_RDY within tSrcTransition_Max(35ms) + tSrcSwapStdby_Max(650ms) time.The time interval is 0.051s.Protocol index #50	PASS
		USB Type-C Error_Recovery check - TEST.PD.PROT.SRC.13#3 >>Expected nRetryCount is 3.Obtained retry count is 3 DUT response time:(6.06582 mS),spec limit time interval is:[<= 15.000000 mS]	PASS
		Rev3ChkdSrc	PASS
		PR_Swap response check - TEST.PD.PROT.SRC.13#1 >>UUT respond Accept to PR_Swap message.The VIF field PD_Port_Type is set to DRP	PASS
		PS_RDY message check - TEST.PD.PROT.SRC.13#2 >>UUT sent PS_RDY message to PR_SWAp response after VBUS voltage to vSafe0V(0V-0.8V).The present voltage is 0.4151V.Protocol index #119 UUT sent PS_RDY within tSrcTransition_Max(35ms) + tSrcSwapStdby_Max(650ms) time.The time interval is 0.0474s.Protocol index #119	PASS
		USB Type-C Error_Recovery check - TEST.PD.PROT.SRC.13#3 >>Expected nRetryCount is 2.Obtained retry count is 2 DUT response time:(5.71741 mS),spec limit time interval is:[<= 15.000000 mS]	PASS
44	TEST.PD.PROT.SRC3.1	TEST.PD.PROT.SRC3.1 SourceCapabilityTimer Timeout	PASS
		Rev3ChkdSrc	PASS
		tFirstSourceCap timer check - TEST.PD.PROT.SRC3.1#1 >>start time: 1.16249711 VBusUp time: 1.10083661s Obt time:0.0617s [PASS] Max = 250ms. Obtained time difference is 61.661ms	PASS

SI No	Test ID	Test Name	Test Result
		tTypeCSendSourceCap timer check - TEST.PD.PROT.SRC3.1#2 >>SourceCap[1-2]:Min= 0ms - Max= 1.295ms.Obtained value 1.0362ms SourceCap[2-3]:Min= 0ms - Max= 1.295ms.Obtained value 1.0364ms SourceCap[3-4]:Min= 100.9ms - Max= 201.1ms.Obtained value 124.04745ms SourceCap[4-5]:Min= 0ms - Max= 1.295ms.Obtained value 1.0366ms	PASS
45	TEST.PD.PROT.SRC3.2	TEST.PD.PROT.SRC3.2 SenderResponseTimer Timeout	PASS
		Rev3ChkdSrc	PASS
		Source_Cap check - TEST.PD.PROT.SRC3.2#1 >>start time: 1.18505581 VBusUp time: 1.1233953s Obt time:0.0617s [PASS] Max = 250ms. Obtained time difference is 61.661ms	PASS
		Hard_Reset check - TEST.PD.PROT.SRC3.2#2 >DUT sent Hard_Reset message,within tSenderResponse Min(27ms) and Max(33ms) timer.The obtained time interval is 27.0268s	PASS
46	TEST.PD.PROT.SRC3.3	TEST.PD.PROT.SRC3.3 Get_Source_Cap_Extended Response	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.268s and SourceCap time: 1.332s at protocol index #19 [PASS] Max = 250ms. Obtained time difference is 64.16ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc >>Tester failed to initiate request	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 5.737s and SourceCap time: 5.799s at protocol index #67 [PASS] Max = 250ms. Obtained time difference is 61.661ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 > Please check the capture and confirm	PASS

SI No	Test ID	Test Name	Test Result
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		Rev3ChkdSrc	PASS
		Source_Cap check - [TEST.PD.PROT.SRC3.3#1 >>UUT respond Source_Cap_Extended to Get_Source_Cap_Extended message.	PASS
		Rev3UnchkdSrc	PASS
		Source_Cap check - [TEST.PD.PROT.SRC3.3#1 >>UUT respond Source_Cap_Extended to Get_Source_Cap_Extended message.	PASS
47	TEST.PD.PROT.SRC3.4	TEST.PD.PROT.SRC3.4 Alert Response Source Input Change	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.093s and SourceCap time: 1.156s at protocol index #19 [PASS] Max = 250ms. Obtained time difference is 63.327ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc >>Tester failed to initiate request	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 4.603s and SourceCap time: 4.664s at protocol index #71 [PASS] Max = 250ms. Obtained time difference is 61.661ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		Rev3ChkdSrc >> UUT respond to Alert within 500 ms .Obtained time difference is 24ms	PASS

SI No	Test ID	Test Name	Test Result
		Rev3UnchkdSrc >> UUT respond to Alert within 500 ms .Obtained time difference is 24ms	PASS
48	TEST.PD.PROT.SRC3.5	TEST.PD.PROT.SRC3.5 Alert Response Battery Status Change	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.091s and SourceCap time: 1.154s at protocol index #19 [PASS] Max = 250ms. Obtained time difference is 63.327ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc >>Tester failed to initiate request	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 4.194s and SourceCap time: 4.255s at protocol index #67 [PASS] Max = 250ms. Obtained time difference is 61.661ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		Rev3ChkdSrc	PASS
		Get_Battery_Status check - TEST.PD.PROT.SRC3.5#1 >>UUT is not respond to Alert message	PASS
		Rev3UnchkdSrc	PASS
		Get_Battery_Status check - TEST.PD.PROT.SRC3.5#1 >>UUT is not respond to Alert message	PASS
49	TEST.PD.PROT.SRC3.6	TEST.PD.PROT.SRC3.6 Soft_Reset Sent when SinkTxOK	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS

SI No	Test ID	Test Name	Test Result
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.103s and SourceCap time: 1.166s at protocol index #19 [PASS] Max = 250ms. Obtained time difference is 63.327ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		Rev3ChkdSrc	PASS
		Soft_Reset check - TEST.PD.PROT.SRC3.6#1 >>UUT is respond message within tReceiveMax(1.1ms) + tSoftResetMax(15ms).The interval is 0.0048s	PASS
50	TEST.PD.PROT.SRC3.7	TEST.PD.PROT.SRC3.7 Get_PPS_Status Response	NA
		--- UUT does not support PPS APDO in Source Caps	
51	TEST.PD.PROT.SRC3.8	TEST.PD.PROT.SRC3.8 SourcePPSCCommTimer Deadline	NA
		--- UUT does not support PPS APDO in Source Caps	
52	TEST.PD.PROT.SRC3.9	TEST.PD.PROT.SRC3.9 SourcePPSCCommTimer Timeout	NA
		--- UUT does not support PPS APDO in Source Caps	
53	TEST.PD.PROT.SRC3.10	TEST.PD.PROT.SRC3.10 SourcePPSCCommTimer Stopped	NA
		--- UUT does not support PPS APDO in Source Caps	
54	TEST.PD.PROT.SRC3.11	TEST.PD.PROT.SRC3.11 GoodCRC Specification Revision Compatibility	PASS
		Rev3ChkdSrc	PASS
		1.SourceCap Check - TEST.PD.PROT.SRC3.11#1	PASS
		1.GoodCRC Specification Revision with 00b - TEST.PD.PROT.SRC3.11#2	PASS
		2.SourceCap Check - TEST.PD.PROT.SRC3.11#1	PASS
		2.GoodCRC Specification Revision with 01b - TEST.PD.PROT.SRC3.11#2	PASS
		3.SourceCap Check - TEST.PD.PROT.SRC3.11#1	PASS
		3.GoodCRC Specification Revision with 10b - TEST.PD.PROT.SRC3.11#2	PASS
55	TEST.PD.PROT.SRC3.12	TEST.PD.PROT.SRC3.12 FR Swap Without Signaling	PASS
		COMMON.PROC.BU.1	PASS

SI No	Test ID	Test Name	Test Result
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.136s and SourceCap time: 1.199s at protocol index #19 [PASS] Max = 250ms. Obtained time difference is 62.494ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		Rev3ChkdSrc	PASS
		FR_Swap response check - TEST.PD.PROT.SRC3.12#1 >>DUT respond Not_Supported to FR_Swap message	PASS
56	TEST.PD.PROT.SRC3.13	TEST.PD.PROT.SRC3.13 Cable Type Detection	PASS
		Rev3ChkdSrc	PASS
		Source_Cap PDO check - TEST.PD.PROT.SRC3.13#1 >>UUT sent SourceCap message.Protocol index #30 UUT SourceCap message offering current <=3A or voltage <=20V	PASS
		Source_Cap PDO check - TEST.PD.PROT.SRC3.13#2 >>UUT sent SourceCap message.Protocol index #67 UUT SourceCap message offering current <=3A or voltage <=20V	PASS
		Source_Cap PDO check - TEST.PD.PROT.SRC3.13#3 >>UUT sent SourceCap message.Protocol index #102 UUT SourceCap message offering current <=3A or voltage <=20V	PASS
57	TEST.PD.PROT.SRC3.14	TEST.PD.PROT.SRC3.14 Source Info	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.105s and SourceCap time: 1.169s at protocol index #19 [PASS] Max = 250ms. Obtained time difference is 64.16ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS

SI No	Test ID	Test Name	Test Result
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 > Please check the capture and confirm	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 3.633s and SourceCap time: 3.695s at protocol index #67 [PASS] Max = 250ms. Obtained time difference is 61.66ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 > Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 6.177s and SourceCap time: 6.233s at protocol index #114 [PASS] Max = 250ms. Obtained time difference is 56.661ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 8.725s and SourceCap time: 8.788s at protocol index #161 [PASS] Max = 250ms. Obtained time difference is 63.327ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc	PASS

SI No	Test ID	Test Name	Test Result
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 11.274s and SourceCap time: 11.34s at protocol index #209 [PASS] Max = 250ms. Obtained time difference is 65.827ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 13.822s and SourceCap time: 13.879s at protocol index #256 [PASS] Max = 250ms. Obtained time difference is 57.494ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		Rev3ChkdSrc	PASS
		First Source_Info field check - TEST.PD.PROT.SRC3.14#1	NA
		First Get_Source_Info response check - TEST.PD.PROT.SRC3.14#2 >>Tester sent Get_Source_Info message Packet 45 UUT responded with Not_Supported at protocol index #47	PASS
		Rev3ChkdSrc	PASS
		Second Get_Source_Info response check - TEST.PD.PROT.SRC3.14#3 >>Tester sent Get_Source_Info message Packet 93 UUT responded with Not_Supported at protocol index #95	PASS
		Second Source_Info field check - TEST.PD.PROT.SRC3.14#4	NA
		Rev3ChkdSrc	PASS

SI No	Test ID	Test Name	Test Result
		Third Get_Source_Info response check - TEST.PD.PROT.SRC3.14#5 >>Tester sent Get_Source_Info message Packet 139 UUT responded with Not_Supported at protocol index #141	PASS
		Third Source_Info field check - TEST.PD.PROT.SRC3.14#6	NA
		Rev3UnchkdSrc	PASS
		First Source_Info field check - TEST.PD.PROT.SRC3.14#1	NA
		First Get_Source_Info response check - TEST.PD.PROT.SRC3.14#2 >>Tester sent Get_Source_Info message Packet 187 UUT responded with Not_Supported at protocol index #189	PASS
		Rev3UnchkdSrc	PASS
		Second Get_Source_Info response check - TEST.PD.PROT.SRC3.14#3 >>Tester sent Get_Source_Info message Packet 235 UUT responded with Not_Supported at protocol index #237	PASS
		Second Source_Info field check - TEST.PD.PROT.SRC3.14#4	NA
		Rev3UnchkdSrc	PASS
		Third Get_Source_Info response check - TEST.PD.PROT.SRC3.14#5 >>Tester sent Get_Source_Info message Packet 281 UUT responded with Not_Supported at protocol index #283	PASS
		Third Source_Info field check - TEST.PD.PROT.SRC3.14#6	NA
58	TEST.PD.PROT.SRC3.15	TEST.PD.PROT.SRC3.15 Alert Response Extended Alert	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.125s and SourceCap time: 1.189s at protocol index #19 [PASS] Max = 250ms. Obtained time difference is 64.16ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS

SI No	Test ID	Test Name	Test Result
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		Rev3ChkdSrc >> Tester sent Alert message Packet 45	PASS
		Accept message check - TEST.PD.PROT.SRC3.15#1 >>Tester sent Request message Packet 50 UUT responded with Accept message at Protocol Index 52	PASS
59	TEST.PD.PROT.SNK.1	TEST.PD.PROT.SNK.1 Get_Sink_Cap Response	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk >>SourceCap Packet15	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet17	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet44	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet46	PASS
		Rev2Snk	PASS
		Get_Sink_Cap Response Check - TEST.PD.PROT.SNK.1#1 >>DUT sent Sink_Cap message at protocol index 28	PASS
		Rev3ChkdSnk	PASS
		Get_Sink_Cap Response Check - TEST.PD.PROT.SNK.1#1 >>DUT sent Sink_Cap message at protocol index 72	PASS
60	TEST.PD.PROT.SNK.2	TEST.PD.PROT.SNK.2 Get_Source_Cap Response	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk >>SourceCap Packet14	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet16	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet43	PASS

SI No	Test ID	Test Name	Test Result
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet45	PASS
		Rev2Snk	PASS
		Get_Source_Cap Response Check - TEST.PD.PROT.SNK.2#1 >>DUT responded with SourceCap message at protocol index27	PASS
		Rev3ChkdSnk	PASS
		Get_Source_Cap Response Check - TEST.PD.PROT.SNK.2#1 >>DUT responded with SourceCap message at protocol index71	PASS
61	TEST.PD.PROT.SNK.3	TEST.PD.PROT.SNK.3 SinkWaitCapTimer Deadline	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk >>SourceCap Packet14	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet16	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet49	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet51	PASS
		Rev2Snk	PASS
		Hard_Reset check - TEST.PD.PROT.SNK.3#1 >>Tester sent Hard_Reset message Packet 25 Tester sent SourceCap message Packet 27 Tester transmits SourceCap within tTypeCSinkWaitCap min (0.31) S UUT sent Request message at protocol index 29	PASS
		Request message check - TEST.PD.PROT.SNK.3#2	NA
		Rev3ChkdSnk	PASS

SI No	Test ID	Test Name	Test Result
		Hard_Reset check - TEST.PD.PROT.SNK.3#1 >>Tester sent Hard_Reset message Packet 75 Tester sent SourceCap message Packet 78 Tester transmits SourceCap within tTypeCSinkWaitCap min (0.31) S Tester Rp set to SinkTxNG(1.5A) UUT sent Request message at protocol index 80	PASS
		Request message check - TEST.PD.PROT.SNK.3#2	NA
62	TEST.PD.PROT.SNK.4	TEST.PD.PROT.SNK.4 SinkWaitCapTimer Timeout	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk >>SourceCap Packet14	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet16	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet53	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet55	PASS
		Rev2Snk	PASS
		SinkWaitCapTimer Timeout - TEST.PD.PROT.SNK.4#1 >>UUT sent HardReset within 0.39974749s	PASS
		Rev3ChkdSnk	PASS
		SinkWaitCapTimer Timeout - TEST.PD.PROT.SNK.4#1 >>UUT sent HardReset within 0.398690670000001s	PASS
63	TEST.PD.PROT.SNK.5	TEST.PD.PROT.SNK.5 SenderResponseTimer Deadline	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk >>SourceCap Packet14	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet16	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet47	PASS

SI No	Test ID	Test Name	Test Result
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet49	PASS
		Rev2Snk	PASS
		SenderResponseTimer Deadline - TEST.PD.PROT.SNK.5#1 >>Tester sent SourceCap message Packet 25 UUT sent Request message Packet 27 Tester send an Accept message at tCtsSrcAccept 22.531 ms and Max time 22.76 ms at protocol index #29	PASS
		Rev3ChkdSnk	PASS
		SenderResponseTimer Deadline - TEST.PD.PROT.SNK.5#1 >>Tester sent SourceCap message Packet 73 UUT sent Request message Packet 75 Tester send an Accept message at tCtsSrcAccept 25.533 ms and Max time 25.76 ms at protocol index #77	PASS
64	TEST.PD.PROT.SNK.6	TEST.PD.PROT.SNK.6 SenderResponseTimer Timeout	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk >>SourceCap Packet14	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet16	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet54	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet56	PASS
		Rev2Snk	PASS

SI No	Test ID	Test Name	Test Result
		SenderResponseTimer Timeout - TEST.PD.PROT.SNK.6#1 >>UUT sent Request message Packet 27 UUT sent Hard_Reset message Packet 29 [PASS] Min= 24ms - Max = 30ms. Obtained time difference is 26.963ms	PASS
		Rev3ChkdSnk	PASS
		SenderResponseTimer Timeout - TEST.PD.PROT.SNK.6#1 >>UUT sent Request message Packet 82 UUT sent Hard_Reset message Packet 84 [PASS] Min= 27ms - Max = 33ms. Obtained time difference is 27.052ms	PASS
65	TEST.PD.PROT.SNK.7	TEST.PD.PROT.SNK.7 PStTransitionTimer Timeout	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk >>SourceCap Packet14	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet16	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet56	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet58	PASS
		Rev2Snk	PASS
		Request message check - TEST.PD.PROT.SNK.7#1 >>UUT sent Request at protocol index 27	PASS
		PStTransitionTimer timeout delay check - TEST.PD.PROT.SNK.7#2 >>Hard_Reset is detected within 0.4732s at protocol index 31	PASS
		Rev3ChkdSnk	PASS
		Request message check - TEST.PD.PROT.SNK.7#1 >>UUT sent Request at protocol index 84	PASS
		PStTransitionTimer timeout delay check - TEST.PD.PROT.SNK.7#2 >>Hard_Reset is detected within 0.4732s at protocol index 88	PASS
66	TEST.PD.PROT.SNK.8	TEST.PD.PROT.SNK.8 Atomic Message Sequence – Accept	PASS

SI No	Test ID	Test Name	Test Result
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk >>SourceCap Packet14	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet16	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet60	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet62	PASS
		Rev2Snk	PASS
		UUT Request message check - TEST.PD.PROT.SNK.8#1 >>UUT respond Request to SourceCap message	PASS
		SoftReset response check - TEST.PD.PROT.SNK.8#2 >>UUT respond SoftReset message within 0.0064 S	PASS
		UUT Request message check - TEST.PD.PROT.SNK.8#3 >>UUT respond Request to SourceCap message	PASS
		Rev3ChkdSnk	PASS
		UUT Request message check - TEST.PD.PROT.SNK.8#1 >>UUT respond Request to SourceCap message	PASS
		SoftReset response check - TEST.PD.PROT.SNK.8#2 >>UUT respond SoftReset message within 0.0031 S	PASS
		UUT Request message check - TEST.PD.PROT.SNK.8#3 >>UUT respond Request to SourceCap message	PASS
67	TEST.PD.PROT.SNK.9	TEST.PD.PROT.SNK.9 Atomic Message Sequence – PS_RDY	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk >>SourceCap Packet14	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet16	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet61	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet63	PASS
		Rev2Snk	PASS

SI No	Test ID	Test Name	Test Result
		UUT Request message check - TEST.PD.PROT.SNK.9#1 >>UUT respond Request to SourceCap message	PASS
		HardReset check - TEST.PD.PROT.SNK.9#2 >>[PASS] Max = 325ms. Obtained time difference is 320.284ms Packet 33 UUT respond Hard_Reset message.The obtained interval 0.004032s	PASS
		Rev3ChkdSnk	PASS
		UUT Request message check - TEST.PD.PROT.SNK.9#1 >>UUT respond Request to SourceCap message	PASS
		HardReset check - TEST.PD.PROT.SNK.9#2 >>[PASS] Max = 325ms. Obtained time difference is 320.949ms Packet 96 UUT respond Hard_Reset message.The obtained interval 0.004177s	PASS
68	TEST.PD.PROT.SNK.10	TEST.PD.PROT.SNK.10 DR_Swap Request	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk >>SourceCap Packet14	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet16	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet52	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet54	PASS
		Rev2Snk	PASS
		First DR_Swap response check - TEST.PD.PROT.SNK.10#1 >>UUT sent Accept for DR_Swap message at protocol index 27,In VIF DR_Swap_To_DFP_Supported field updated as YES	PASS
		Second DR_Swap response check - TEST.PD.PROT.SNK.10#2 >>UUT sent Accept for DR_Swap message at protocol index 36,In VIF DR_Swap_To_UFP_Supported field updated as YES	PASS
		Rev3ChkdSnk	PASS
		First DR_Swap response check - TEST.PD.PROT.SNK.10#1 >>UUT sent Accept for DR_Swap message at protocol index 80,In VIF DR_Swap_To_DFP_Supported field updated as YES	PASS

SI No	Test ID	Test Name	Test Result
		Second DR_Swap response check - TEST.PD.PROT.SNK.10#2 >>UUT sent Accept for DR_Swap message at protocol index 90,In VIF DR_Swap_To_UFP_Supported field updated as YES	PASS
69	TEST.PD.PROT.SNK.11	TEST.PD.PROT.SNK.11 VCONN_Swap Request	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk >>SourceCap Packet15	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet17	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet53	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet55	PASS
		Rev2Snk	PASS
		VCONN present check - TEST.PD.PROT.SNK.11#1 >>Tester VCONN not present at non CC line.The measured VBUS voltage is 0.008314V.	PASS
		VCONN_Swap response check - TEST.PD.PROT.SNK.11#2 >>UUT respond Accept to VCONN_Swap message and VCONN_Swap_To_On_Supported field is NO	NA
		UUT PS_RDY message check - TEST.PD.PROT.SNK.11#3 >>UUT respond Accept to VCONN_Swap message and VCONN_Swap_To_On_Supported field is NO	NA
		VCONN present check - TEST.PD.PROT.SNK.11#4 >>UUT respond Accept to VCONN_Swap message and VCONN_Swap_To_On_Supported field is NO	NA
		Second VCONN_Swap response check - TEST.PD.PROT.SNK.11#5 >>UUT respond Accept to VCONN_Swap message and VCONN_Swap_To_On_Supported field is NO	NA
		tVCONNSourceOff timer check - TEST.PD.PROT.SNK.11#6 >>UUT respond Accept to VCONN_Swap message and VCONN_Swap_To_On_Supported field is NO	NA
		Rev3ChkdSnk	NA

SI No	Test ID	Test Name	Test Result
		VCONN present check - TEST.PD.PROT.SNK.11#1 >>Tester VCONN not present at non CC line.The measured VBUS voltage is 0.008314V.	PASS
		VCONN_Swap response check - TEST.PD.PROT.SNK.11#2 >>UUT respond Accept to VCONN_Swap message and VCONN_Swap_To_On_Supported field is NO	NA
		UUT PS_RDY message check - TEST.PD.PROT.SNK.11#3 >>UUT respond Accept to VCONN_Swap message and VCONN_Swap_To_On_Supported field is NO	NA
		VCONN present check - TEST.PD.PROT.SNK.11#4 >>UUT respond Accept to VCONN_Swap message and VCONN_Swap_To_On_Supported field is NO	NA
		Second VCONN_Swap response check - TEST.PD.PROT.SNK.11#5 >>UUT respond Accept to VCONN_Swap message and VCONN_Swap_To_On_Supported field is NO	NA
		tVCONNSourceOff timer check - TEST.PD.PROT.SNK.11#6 >>UUT respond Accept to VCONN_Swap message and VCONN_Swap_To_On_Supported field is NO	NA
70	TEST.PD.PROT.SNK.12	TEST.PD.PROT.SNK.12 PR_Swap – PSSourceOffTimer Timeout	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk >>SourceCap Packet14	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet16	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet58	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet60	PASS
		Rev2Snk	PASS
		PR_Swap response check - TEST.PD.PROT.SNK.12#1 >>UUT respond Accept to PR_Swap message.The VIF field Accept_PR_Swap_As_Snk is set to YES	PASS

SI No	Test ID	Test Name	Test Result
		USB Type-C Error Recovery check - TEST.PD.PROT.SNK.12#2 >>UUT sent Type-C Error Recovery within tPSSourceOff[750ms - 920ms].The time interval is 0.7901s	PASS
		Rev3ChkdSnk	PASS
		PR_Swap response check - TEST.PD.PROT.SNK.12#1 >>UUT respond Accept to PR_Swap message.The VIF field Accept_PR_Swap_As_Snk is set to YES	PASS
		USB Type-C Error Recovery check - TEST.PD.PROT.SNK.12#2 >>UUT sent Type-C Error Recovery within tPSSourceOff[750ms - 920ms].The time interval is 0.7893s	PASS
71	TEST.PD.PROT.SNK.13	TEST.PD.PROT.SNK.13 PR_Swap – Request SenderResponseTimer Timeout	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk >>SourceCap Packet14	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet16	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet94	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet96	PASS
		Rev2Snk	PASS
		PR_Swap response check - TEST.PD.PROT.SNK.13#1 >>UUT respond Accept to PR_Swap message.The VIF field PD_Port_Type is DRP The VIF field Accepts_PR_Swap_As_Snk is YES	PASS
		UUT PS_RDY check - TEST.PD.PROT.SNK.13#2 >>UUT sent PS_RDY message after VBUS voltage to vSafe5V(4.75V - 5.5V).The present voltage is 5.042436V	PASS
		tPSSourceOn timer check - TEST.PD.PROT.SNK.13#3 >>UUT respond PS_RDY within tPSSourceOn_Min(390ms) time.The present interval is 0.39s	PASS
		tSwapSourceStart timer check - TEST.PD.PROT.SNK.13#4 >>UUT sent SourceCap message after tSwapSourceStart(20ms).Obtained time interval 0.066569s	PASS

SI No	Test ID	Test Name	Test Result
		SourceCap message check - TEST.PD.PROT.SNK.13#5 >>UUT respond SourceCap message to Get_Source_Cap message	PASS
		HardReset message check - TEST.PD.PROT.SNK.13#6 >>UUT sent Hard_Reset within tSenderResponse(24ms - 30ms).Obtained time interval 0.02681s	PASS
		Rev3ChkdSnk	PASS
		PR_Swap response check - TEST.PD.PROT.SNK.13#1 >>UUT respond Accept to PR_Swap message.The VIF field PD_Port_Type is DRP The VIF field Accepts_PR_Swap_As_Snk is YES	PASS
		UUT PS_RDY check - TEST.PD.PROT.SNK.13#2 >>UUT sent PS_RDY message after VBUS voltage to vSafe5V(4.75V - 5.5V).The present voltage is 5.061882V	PASS
		tPSSourceOn timer check - TEST.PD.PROT.SNK.13#3 >>UUT respond PS_RDY within tPSSourceOn_Min(390ms) time.The present interval is 0.39s	PASS
		tSwapSourceStart timer check - TEST.PD.PROT.SNK.13#4 >>UUT sent SourceCap message after tSwapSourceStart(20ms).Obtained time interval 0.024213s	PASS
		SourceCap message check - TEST.PD.PROT.SNK.13#5 >>UUT respond SourceCap message to Get_Source_Cap message	PASS
		HardReset message check - TEST.PD.PROT.SNK.13#6 >>UUT sent Hard_Reset within tSenderResponse(27ms - 33ms).Obtained time interval 0.027167s	PASS
72	TEST.PD.PROT.SNK.14	TEST.PD.PROT.SNK.14 Valid Use of GoodCRC on Power up	PASS
		Rev2Snk	PASS
		UUT Response with Request message - TEST.PD.PROT.SNK.14#1 >>UUT respond with a Request message within tReceiverResponse_Max 15ms at protocol index #22 [PASS] Max = 325ms. Obtained time difference is 320.264ms Packet 26	PASS
		Rev3ChkdSnk	PASS

SI No	Test ID	Test Name	Test Result
		UUT Response with Request message - TEST.PD.PROT.SNK.14#1 >>UUT respond with a Request message within tReceiverResponse_Max 15ms at protocol index #50 [PASS] Max = 325ms. Obtained time difference is 321.952ms Packet 54	PASS
73	TEST.PD.PROT.SNK3.1	TEST.PD.PROT.SNK3.1 Get_Source_Cap_Extended	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet16	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet18	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3UnchkdSnk >>SourceCap Packet65	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet67	PASS
		Rev3ChkdSnk	PASS
		Get_Source_Cap_Extended - Unchunked Extended Support 0 - TEST.PD.PROT.SNK3.1#1 >>Source_Cap_Extended Packet44	PASS
		Rev3UnchkdSnk	PASS
		Get_Source_Cap_Extended - Unchunked Extended Support 1 - TEST.PD.PROT.SNK3.1#1 >>Source_Cap_Extended Packet93	PASS
74	TEST.PD.PROT.SNK3.2	TEST.PD.PROT.SNK3.2 Alert Response Source Input Change	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet15	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet17	PASS
		Rev3ChkdSnk	PASS
		Alert Response Source Input Change - Unchunked Extended Support 0 - [TEST.PD.PROT.SNK3.2#1] >>DUT responded with Get_Status message at protocol index 45. The obtained interval 0.00601225999999988s	PASS

SI No	Test ID	Test Name	Test Result
75	TEST.PD.PROT.SNK3.3	TEST.PD.PROT.SNK3.3 Alert Response Battery Status Change	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet15	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet17	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3UnchkdSnk >>SourceCap Packet62	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet64	PASS
		Rev3ChkdSnk	PASS
		Alert Response Battery Status Change - Unchunked Extended Support 0 - [TEST.PD.PROT.SNK3.3#1] >>UUT not responded to Alert message	PASS
		Rev3UnchkdSnk	PASS
		Alert Response Battery Status Change - Unchunked Extended Support 1 - [TEST.PD.PROT.SNK3.3#1] >>UUT not responded to Alert message	PASS
76	TEST.PD.PROT.SNK3.4	TEST.PD.PROT.SNK3.4 Soft_Reset Sent Regardless of Rp Value	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet15	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet17	PASS
		Rev3ChkdSnk	PASS
		Soft_Reset timing check - [TEST.PD.PROT.SNK3.4#1]	PASS
77	TEST.PD.PROT.SNK3.5	TEST.PD.PROT.SNK3.5 Sink PPS Normal Operation	PASS
		COMMON.PROC.BU.5	PASS
		COMMON.PROC.BU.5 - REVISION_3_0 Snk >>[PASS] Max = 250ms. Obtained time difference is 48.329ms Packet19 [PASS] Max = 325ms. Obtained time difference is 320.954ms Packet 21	PASS

SI No	Test ID	Test Name	Test Result
		UUT should respond with request - COMMON.PROC.BU.5#1 >>Packet17	PASS
		Rev3ChkdSnk >> UUT responded Request for Source_Cap message.	PASS
		Request message check - [TEST.PD.PROT.SNK3.5#1] >>tPPSRequest max time is: 10s. Obtained time difference is 3.231s	PASS
		Request data object check - [TEST.PD.PROT.SNK3.5#2]	PASS
		Object Position Check >>Request PDO object position updated as 2 in Request message.Protocol index 60	PASS
78	TEST.PD.PROT.SNK3.6	TEST.PD.PROT.SNK3.6 Revision Number Test	PASS
		Rev3ChkdSnk	PASS
		Revision Number Test - [TEST.PD.PROT.SNK3.6#1]	PASS
79	TEST.PD.PROT.SNK3.7	TEST.PD.PROT.SNK3.7 GoodCRC Specification Revision Compatibility	PASS
		Rev3ChkdSnk	PASS
		GoodCRC revision 1 Response Check - TEST.PD.PROT.SNK3.7#1	PASS
		GoodCRC revision 1 Retransmission check - TEST.PD.PROT.SNK3.7#2	PASS
		GoodCRC revision 2 Response Check - TEST.PD.PROT.SNK3.7#1	PASS
		GoodCRC revision 2 Retransmission check - TEST.PD.PROT.SNK3.7#2	PASS
		GoodCRC revision 3 Response Check - TEST.PD.PROT.SNK3.7#1	PASS
		GoodCRC revision 3 Retransmission check - TEST.PD.PROT.SNK3.7#2	PASS
80	TEST.PD.PROT.SNK3.9	TEST.PD.PROT.SNK3.9 Alert Response Extended Alert	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet15	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet17	PASS
		Rev3ChkdSnk >> Tester sent Alert message Packet 41	PASS

SI No	Test ID	Test Name	Test Result
		Request message check - TEST.PD.PROT.SNK3.9#1 >>Tester sent SourceCap message Packet 49 UUT sent Request message Packet 51	PASS
81	TEST.PD.VDM.SNK.1	TEST.PD.VDM.SNK.1 Discovery Process and Enter Mode	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk >>SourceCap Packet14	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet16	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet73	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet75	PASS
		Rev2Snk	PASS
		Discover ID request Check - TEST.PD.VDM.SNK.1#1 >>DUT sent Responder ACK for Discover ID at the protocol index 27	PASS
		Discover ID response Check - TEST.PD.VDM.SNK.1#2	PASS
		Number of VDOs >>Product Type is AMA and Number of Data Obj is 4	PASS
		Data_Capable_as_USB_Host_SOP >>VIF data : YES and DUT data : YES	PASS
		Data_Capable_as_USB_Device_SOP >>VIF data : YES and DUT data : YES	PASS
		Product_Type_UFP_SOP >>VIF data : Peripheral and DUT data : AMA	PASS
		Modal_Operation_Supported_SOP >Check fails, B26 does match VIF field Modal_Operation_Supported_SOP VIF data : NO and DUT data : NO	PASS
		Check B25..16 is set to zero >>B25...16 is set to zero	PASS

SI No	Test ID	Test Name	Test Result
		Cert Sat VDO Check >>VIF data : 0 and DUT data : 0	PASS
		Product VDO Check >>PID_SOP VIF data : 0 and DUT data : 0 VIF data : 0 and DUT data : 0	PASS
		Discover SVID request Check - TEST.PD.VDM.SNK.1#3 >DUT sent Responder_ACK for Discover SVID Modal_Operation_Supported_SOP in VIF is yes	PASS
		Discover SVID response Check - TEST.PD.VDM.SNK.1#4	PASS
		Discover Mode for each SVID - TEST.PD.VDM.SNK.1#5	PASS
		Enter and Exit Mode for each Mode - TEST.PD.VDM.SNK.1#6	PASS
		Attention Request - TEST.PD.VDM.SNK.1#7	PASS
		Rev3ChkdSnk	PASS
		Discover ID request Check - TEST.PD.VDM.SNK.1#1 >>DUT sent Responder_ACK for Discover ID at the protocol index 101	PASS
		Discover ID response Check - TEST.PD.VDM.SNK.1#2	PASS
		Number of VDOs	PASS
		Data_Capable_as_USB_Host_SOP >>VIF data : YES and DUT data : YES	PASS
		Data_Capable_as_USB_Device_SOP >>VIF data : YES and DUT data : YES	PASS
		Product_Type_UFP_SOP >Check fails, B29...27 does match VIF field Product_Type_UFP_SOP VIF data : Peripheral and DUT data : Peripheral	PASS
		Modal_Operation_Supported_SOP >Check fails, B26 does match VIF field Modal_Operation_Supported_SOP VIF data : NO and DUT data : NO	PASS
		Product_Type_DFP_SOP >Check fails, B25...23 does match VIF field Product_Type_DFP_SOP VIF data : Host and DUT data : Host	PASS

SI No	Test ID	Test Name	Test Result
		ID_Header_Connector_Type >>Invalid Connector_Type sent by the DUT in B22..21, Decoded value is 0 and VIF value is 2	PASS
		Check B20..16 is set to zero >>B20...16 is set to zero	PASS
		Cert Sat VDO Check >>VIF data : 0 and DUT data : 0	PASS
		Product VDO Check >>PID_SOP VIF data : 0 and DUT data : 0 VIF data : 0 and DUT data : 0	PASS
		Discover SVID request Check - TEST.PD.VDM.SNK.1#3 >>DUT sent Responder_ACK for Discover SVID but Modal_Operation_Supported_SOP in VIF is No:	PASS
		Discover SVID response Check - TEST.PD.VDM.SNK.1#4	PASS
		Discover Mode for each SVID - TEST.PD.VDM.SNK.1#5	PASS
		Enter and Exit Mode for each Mode - TEST.PD.VDM.SNK.1#6	PASS
		Attention Request - TEST.PD.VDM.SNK.1#7	PASS
82	TEST.PD.VDM.SNK.2	TEST.PD.VDM.SNK.2 Exit Mode without Entering	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk >>SourceCap Packet14	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet16	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet47	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet49	PASS
		Rev2Snk	PASS
		SVID Response Check - TEST.PD.VDM.SNK.2#1 >>[PASS] Min= 0.025ms - Max = 15ms. Obtained time difference is 8.096ms Modal_Operation_Supported_SOP in VIF : 'NO' and in UUT response : 'NO'	PASS

SI No	Test ID	Test Name	Test Result
		Exit Mode Check - TEST.PD.VDM.SNK.2#2 >>[PASS] Min= 0.025ms - Max = 25ms. Obtained time difference is 5.843ms UUT respond with Exit Mode NAK	PASS
		Rev3ChkdSnk	PASS
		SVID Response Check - TEST.PD.VDM.SNK.2#1 >>[PASS] Min= 0.025ms - Max = 15ms. Obtained time difference is 8.399ms Modal_Operation_Supported_SOP in VIF : 'NO' and in UUT response : 'NO'	PASS
		Exit Mode Check - TEST.PD.VDM.SNK.2#2 >>[PASS] Min= 0.025ms - Max = 25ms. Obtained time difference is 6.698ms UUT respond with Exit Mode NAK	PASS
83	TEST.PD.VDM.SNK.5	TEST.PD.VDM.SNK.5 DR Swap in Modal Operation	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk >>SourceCap Packet14	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet16	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet69	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet71	PASS
		Rev2Snk	PASS
		SVID Response Check - TEST.PD.VDM.SNK.5#1 >>Modal_Operation_Supported_SOP in VIF : 'NO' and in UUT response : 'NO'	PASS
		Discover Mode Response Check - TEST.PD.VDM.SNK.5#2	PASS
		Enter Mode Response Check - TEST.PD.VDM.SNK.5#3 >>Tester initiated Discover Mode AMS	PASS
		Enter Mode Ack Check - TEST.PD.VDM.SNK.5#4 >>Hard_Reset message received within 0.0022 S	PASS
		Rev3ChkdSnk	PASS

SI No	Test ID	Test Name	Test Result
		SVID Response Check - TEST.PD.VDM.SNK.5#1 >>Modal_Operation_Supported_SOP in VIF : 'NO' and in UUT response : 'NO'	PASS
		Discover Mode Response Check - TEST.PD.VDM.SNK.5#2	PASS
		Enter Mode Response Check - TEST.PD.VDM.SNK.5#3 >>Tester initiated Discover Mode AMS	PASS
		Enter Mode Ack Check - TEST.PD.VDM.SNK.5#4 >>Hard_Reset message received within 0.0038 S	PASS
84	TEST.PD.VDM.SNK.6	TEST.PD.VDM.SNK.6 Structured VDM Revision Number Test	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk >>SourceCap Packet14	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet16	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet43	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet45	PASS
		Rev2Snk	PASS
		PD2 - Discover ID Response Check - TEST.PD.VDM.SNK.6#1 >>Response is sent after tInterFrameGap min but before tVDMReceiverResponse max DUT responded with Responder_ACK at the protocol index 27	PASS
		Rev3ChkdSnk	PASS
		PD3 - Discover ID Response Check - TEST.PD.VDM.SNK.6#1 >>Response is sent after tInterFrameGap min but before tVDMReceiverResponse max DUT responded with Responder_ACK at the protocol index 71	PASS
85	TEST.PD.VDM.SNK.7	TEST.PD.VDM.SNK.7 Unrecognized VID in Unstructured VDM	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk >>SourceCap Packet14	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet16	PASS

SI No	Test ID	Test Name	Test Result
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet41	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet43	PASS
		Rev2Snk	PASS
		PD2 - Unstructured VDM Header Response Check - TEST.PD.VDM.SNK.7#1 >>UUT ignored the Tester initiated Unstructured VDM message at protocol index 25	PASS
		Rev3ChkdSnk	PASS
		PD3 - Unstructured VDM Header Response Check - TEST.PD.VDM.SNK.7#1 >>UUT respond with Not_Supported for Tester initiated Unstructured VDM message at protocol index 67	PASS
86	TEST.PD.VDM.CBL.1	TEST.PD.VDM.CBL.1 Discovery Process and Enter Mode	NA
87	TEST.PD.VDM.SRC.1	TEST.PD.VDM.SRC.1 Discovery Process and Enter Mode	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.209s and SourceCap time: 1.27s at protocol index #19 [PASS] Max = 250ms. Obtained time difference is 60.827ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc >>Tester failed to initiate request	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 4.348s and SourceCap time: 4.409s at protocol index #72 [PASS] Max = 250ms. Obtained time difference is 61.661ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS

SI No	Test ID	Test Name	Test Result
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		Rev2Src	PASS
		Discover ID Response Check - TEST.PD.VDM.SRC.1#1 >>UUT ignored the Discover ID at protocol index 49, Responds_To_Discov_SOP_DFP value in VIF is 'YES',Attempts_Discov_SOP is 'YES' and Responds_To_Discov_SOP_UFP is 'YES'	PASS
		Discover ID ACK Response Check - TEST.PD.VDM.SRC.1#3	PASS
		Attention Request message - TEST.PD.VDM.SRC.1#4	PASS
		Rev3ChkdSrc	PASS
		Discover ID Response Check - TEST.PD.VDM.SRC.1#2 >>UUT responds with a "Responder_ACK" message at protocol index 106 and VIF field Responds_To_Discov_SOP_DFP = YES, Responds_To_Discov_SOP_UFP = YES and Attempts_Discov_SOP = YES.	PASS
		Discover ID ACK Check - TEST.PD.VDM.SRC.1#3	PASS
		Data_Capable_as_USB_Host_SOP >>VIF data : YES and DUT data : YES	PASS
		Data_Capable_as_USB_Device_SOP >>VIF data : YES and DUT data : YES	PASS
		Product_Type_UFP_SOP >>[PASS] B29...27 does match VIF field Product_Type_UFP_SOP VIF data : Peripheral and DUT data : Peripheral	PASS
		Modal_Operation_Supported_SOP >>[PASS] B[26] does match VIF field ModalOperation_supported VIF data : NO and DUT data : NO	PASS
		Product_Type_DFP_SOP >>[PASS] B25...23 does match VIF field Product_Type_DFP_SOP VIF data : Host and DUT data : Host	PASS
		ID_Header_Connector_Type >>Invalid Connector_Type sent by the DUT in B22..21	PASS
		B20...16 is set to zero	PASS
		USB_VID_SOP >>[PASS] B15...0 does not match VIF field USB_VID_SOP VIF data : 0 and DUT data : 0	PASS

SI No	Test ID	Test Name	Test Result
		Cert Sat VDO Check >>VIF data : 0 and DUT data : 0	PASS
		Product VDO Check >>[PASS] PID_SOP VIF data : 0 and DUT data : 0 VIF data : 0 and DUT data : 0	PASS
		Attention Request message - TEST.PD.VDM.SRC.1#4	PASS
88	TEST.PD.VDM.SRC.2	TEST.PD.VDM.SRC.2 Invalid Fields – Discover Identity	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.14s and SourceCap time: 1.203s at protocol index #20 [PASS] Max = 250ms. Obtained time difference is 62.494ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 4.258s and SourceCap time: 4.322s at protocol index #72 [PASS] Max = 250ms. Obtained time difference is 64.16ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		Rev2Src	PASS
		Discover_ID Response Check - TEST.PD.VDM.SRC.2#1 >>UUT responded with Responder_NAK at protocol index 52	PASS
		Rev3ChkdSrc	PASS
		Discover_ID Response Check - TEST.PD.VDM.SRC.2#1 >>UUT responded with Responder_NAK at protocol index 106	PASS

SI No	Test ID	Test Name	Test Result
89	TEST.PD.VDM.CBL3.1	TEST.PD.VDM.CBL3.1 Revision Number Test	NA
90	TEST.PD.PS.SRC.1	TEST.PD.PS.SRC.1 Multiple Request Messages	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.125s and SourceCap time: 1.186s at protocol index #19 [PASS] Max = 250ms. Obtained time difference is 60.44ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm failure	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 9.03s and SourceCap time: 9.094s at protocol index #132 [PASS] Max = 250ms. Obtained time difference is 63.937ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		Rev2Src >> Rev2Src sequence starts from protocol index 5	PASS
		>>PDO : 1 transition with operating current 0	PASS
		>>PDO : 1 transition with operating current 0.12	PASS
		>>PDO : 1 transition with operating current 0.25	PASS
		>>PDO : 1 transition with operating current 0.37	PASS

SI No	Test ID	Test Name	Test Result
		>>PDO : 1 transition with operating current 0.5	PASS
		>>PDO : 1 transition with operating current 0.37	PASS
		>>PDO : 1 transition with operating current 0.25	PASS
		>>PDO : 1 transition with operating current 0.12	PASS
		>>PDO : 1 transition with operating current 0	PASS
		Transition (no PDO change) - Current Decrease - TEST.PD.PS.SRC.1#1 >>Load set to 0.37A: [PASS] Vbus voltage before load decrease: 5V , Limit:[4.75V - 5.5V] at Protocol index : 83. Measurement after timestamp : 5.32547465S] Load set to 0.25A: [PASS] Vbus voltage before load decrease: 5.02V , Limit:[4.75V - 5.5V] at Protocol index : 91. Measurement after timestamp : 5.92947272S] Load set to 0.12A: [PASS] Vbus voltage before load decrease: 5.04V , Limit:[4.75V - 5.5V] at Protocol index : 99. Measurement after timestamp : 6.53347398S] Load set to 0A: [PASS] Vbus voltage before load decrease: 5.07V , Limit:[4.75V - 5.5V] at Protocol index : 107. Measurement after timestamp : 7.13747525S]	PASS
		Transition (no PDO change) - Current Increase - TEST.PD.PS.SRC.1#2 >>Load set to 0.12A: [PASS] Vbus voltage before load increase: 5.04V , Limit:[4.75V - 5.5V] at Protocol index : 51. Measurement after timestamp : 2.90946963S] Load set to 0.25A: [PASS] Vbus voltage before load increase: 5.02V , Limit:[4.75V - 5.5V] at Protocol index : 59. Measurement after timestamp : 3.51346770S] Load set to 0.37A: [PASS] Vbus voltage before load increase: 5V , Limit:[4.75V - 5.5V] at Protocol index : 67. Measurement after timestamp : 4.11747214S] Load set to 0.5A: [PASS] Vbus voltage before load increase: 4.98V , Limit:[4.75V - 5.5V] at Protocol index : 75. Measurement after timestamp : 4.72147340S]	PASS
		Transition (PDO change) - TEST.PD.PS.SRC.1#3	PASS

SI No	Test ID	Test Name	Test Result
		Vbus transition - Slew measurement - TEST.PD.PS.SRC.1#4	PASS
		VSrcValid limit - TEST.PD.PS.SRC.1#5	PASS
		Vbus voltage measurement - TEST.PD.PS.SRC.1#6	PASS
		Validate PS_RDY before Vbus - TEST.PD.PS.SRC.1#7	PASS
		Vbus voltage measurement - TEST.PD.PS.SRC.1#8	PASS
		PPS Transition - Current Decrease - TEST.PD.PS.SRC.1#9	PASS
		Validate Request Sequence - TEST.PD.PS.SRC.1#10 >>DUT responded with Accept at the protocol index 45	PASS
		Validate PS_RDY message - TEST.PD.PS.SRC.1#11 >>[PASS] Max = 325ms. Obtained time difference is 30.778ms Packet 47	PASS
		Validate Source_Capability message - TEST.PD.PS.SRC.1#12	PASS
		Validate PS_RDY message - TEST.PD.PS.SRC.1#13	PASS
		Primary Check	PASS
		Load Check >>Configured Eload value is 0.125 A at packet index 57 and measured is 0.1308 A at time 2.94731683s	PASS
		Load Check >>Configured Eload value is 0.25 A at packet index 65 and measured is 0.2653 A at time 3.55144616s	PASS
		Load Check >>Configured Eload value is 0.375 A at packet index 73 and measured is 0.3898 A at time 4.15501036s	PASS
		Load Check >>Configured Eload value is 0.5 A at packet index 81 and measured is 0.5145 A at time 4.76048176s	PASS
		Load Check >>Configured Eload value is 0.375 A at packet index 87 and measured is 0.3899 A at time 5.33289808s	PASS
		Load Check >>Configured Eload value is 0.25 A at packet index 95 and measured is 0.2654 A at time 5.93670095s	PASS

SI No	Test ID	Test Name	Test Result
		Load Check >>Configured Eload value is 0.125 A at packet index 103 and measured is 0.131 A at time 6.53995593s	PASS
		Rev3ChkdSrc >> Rev3ChkdSrc sequence starts from protocol index 118	PASS
		>>PDO : 1 transition with operating current 0	PASS
		>>PDO : 1 transition with operating current 0.12	PASS
		>>PDO : 1 transition with operating current 0.25	PASS
		>>PDO : 1 transition with operating current 0.37	PASS
		>>PDO : 1 transition with operating current 0.5	PASS
		>>PDO : 1 transition with operating current 0.37	PASS
		>>PDO : 1 transition with operating current 0.25	PASS
		>>PDO : 1 transition with operating current 0.12	PASS
		>>PDO : 1 transition with operating current 0	PASS

SI No	Test ID	Test Name	Test Result
		Transition (no PDO change) - Current Decrease - TEST.PD.PS.SRC.1#1 >>Load set to 0.37A: [PASS] Vbus voltage before load decrease: 5V , Limit:[4.75V - 5.5V] at Protocol index : 198. Measurement after timestamp : 13.2814467S] Load set to 0.25A: [PASS] Vbus voltage before load decrease: 5.02V , Limit:[4.75V - 5.5V] at Protocol index : 206. Measurement after timestamp : 13.8854479S] Load set to 0.12A: [PASS] Vbus voltage before load decrease: 5.04V , Limit:[4.75V - 5.5V] at Protocol index : 214. Measurement after timestamp : 14.4894492S] Load set to 0A: [PASS] Vbus voltage before load decrease: 5.07V , Limit:[4.75V - 5.5V] at Protocol index : 222. Measurement after timestamp : 15.0934505S]	PASS
		Transition (no PDO change) - Current Increase - TEST.PD.PS.SRC.1#2 >>Load set to 0.12A: [PASS] Vbus voltage before load increase: 5.04V , Limit:[4.75V - 5.5V] at Protocol index : 166. Measurement after timestamp : 10.8654448S] Load set to 0.25A: [PASS] Vbus voltage before load increase: 5.02V , Limit:[4.75V - 5.5V] at Protocol index : 174. Measurement after timestamp : 11.4694428S] Load set to 0.37A: [PASS] Vbus voltage before load increase: 5V , Limit:[4.75V - 5.5V] at Protocol index : 182. Measurement after timestamp : 12.0734441S] Load set to 0.5A: [PASS] Vbus voltage before load increase: 4.98V , Limit:[4.75V - 5.5V] at Protocol index : 190. Measurement after timestamp : 12.6774454S]	PASS
		Transition (PDO change) - TEST.PD.PS.SRC.1#3	PASS
		Vbus transition - Slew measurement - TEST.PD.PS.SRC.1#4	PASS
		VSrcValid limit - TEST.PD.PS.SRC.1#5	PASS
		Vbus voltage measurement - TEST.PD.PS.SRC.1#6	PASS
		Validate PS_RDY before Vbus - TEST.PD.PS.SRC.1#7	PASS
		Vbus voltage measurement - TEST.PD.PS.SRC.1#8	PASS
		PPS Transition - Current Decrease - TEST.PD.PS.SRC.1#9	PASS
		Validate Request Sequence - TEST.PD.PS.SRC.1#10 >>DUT responded with Accept at the protocol index 160	PASS

SI No	Test ID	Test Name	Test Result
		Validate PS_RDY message - TEST.PD.PS.SRC.1#11 >>[PASS] Max = 325ms. Obtained time difference is 31.61ms Packet 162	PASS
		Validate Source_Capability message - TEST.PD.PS.SRC.1#12	PASS
		Validate PS_RDY message - TEST.PD.PS.SRC.1#13	PASS
		Primary Check	PASS
		Load Check >>Configured Eload value is 0.125 A at packet index 172 and measured is 0.131 A at time 10.903758s	PASS
		Load Check >>Configured Eload value is 0.25 A at packet index 180 and measured is 0.2651 A at time 11.5091937s	PASS
		Load Check >>Configured Eload value is 0.375 A at packet index 188 and measured is 0.39 A at time 12.11169357s	PASS
		Load Check >>Configured Eload value is 0.5 A at packet index 196 and measured is 0.5145 A at time 12.71561511s	PASS
		Load Check >>Configured Eload value is 0.375 A at packet index 202 and measured is 0.39 A at time 13.288564s	PASS
		Load Check >>Configured Eload value is 0.25 A at packet index 210 and measured is 0.2652 A at time 13.89237044s	PASS
		Load Check >>Configured Eload value is 0.125 A at packet index 218 and measured is 0.1309 A at time 14.49651777s	PASS
91	TEST.PD.PS.SRC.2	TEST.PD.PS.SRC.2 PDO Transition	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.179s and SourceCap time: 1.24s at protocol index #19 [PASS] Max = 250ms. Obtained time difference is 61.496ms	PASS

SI No	Test ID	Test Name	Test Result
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 4.31s and SourceCap time: 4.372s at protocol index #67 [PASS] Max = 250ms. Obtained time difference is 62.04ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		Rev2Src	PASS
		PDO Transistion in PD2.0 Mode	PASS
			PASS
		>>PDO Transition 1 to 1	
		Check Accept - TEST.PD.PS.SRC.2#1	PASS
		Check PsRdy - TEST.PD.PS.SRC.2#2 >>[PASS] Max = 325ms. Obtained time difference is 29.725ms Packet 33	PASS
		Check Vbus is within the vSrcNew or vPpsNew - TEST.PD.PS.SRC.2#3	PASS
		Vbus transition - TEST.PD.PS.SRC.2#4	PASS
		Vbus transition - TEST.PD.PS.SRC.2#5	PASS
		Vbus transition - TEST.PD.PS.SRC.2#6	PASS
		UUT does not send PS_RDY before the VBUS is within vSrcNew or vPpsNew - TEST.PD.PS.SRC.2#7	PASS
		Check Source Capability matches VIF - TEST.PD.PS.SRC.2#8	PASS
		Check Accept - TEST.PD.PS.SRC.2#9	PASS
		Rev3ChkdSrc	PASS
		PDO Transistion in PD3.0 Mode	PASS
			PASS
		>>PDO Transition 1 to 1	
		Check Accept - TEST.PD.PS.SRC.2#1	PASS

SI No	Test ID	Test Name	Test Result
		Check PsRdy - TEST.PD.PS.SRC.2#2 >>[PASS] Max = 325ms. Obtained time difference is 29.943ms Packet 81	PASS
		Check Vbus is within the vSrcNew or vPpsNew - TEST.PD.PS.SRC.2#3	PASS
		Vbus transition - TEST.PD.PS.SRC.2#4	PASS
		Vbus transition - TEST.PD.PS.SRC.2#5	PASS
		Vbus transition - TEST.PD.PS.SRC.2#6	PASS
		UUT does not send PS_RDY before the VBUS is within vSrcNew or vPpsNew - TEST.PD.PS.SRC.2#7	PASS
		Check Source Capability matches VIF - TEST.PD.PS.SRC.2#8	PASS
		Check Accept - TEST.PD.PS.SRC.2#9	PASS
92	TEST.PD.PS.SRC.3	TEST.PD.PS.SRC.3 Initial Source PDO Transition Post PR Swap	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.106s and SourceCap time: 1.17s at protocol index #19 [PASS] Max = 250ms. Obtained time difference is 64.16ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 20.071s and SourceCap time: 20.134s at protocol index #104 [PASS] Max = 250ms. Obtained time difference is 63.327ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		Rev2Src	PASS

SI No	Test ID	Test Name	Test Result
		PR_Swap Response Check - TEST.PD.PS.SRC.3#1 >>DRP UUT sent Accept for PR_Swap message.	PASS
		UUT PS_RDY Check - TEST.PD.PS.SRC.3#2 >>UUT respond PS_RDY message to PR_SWAP after VBUS voltage to vSafe0V(0V - 0.8V).The present voltage is 0.314V	PASS
		Tester PS_RDY Check - TEST.PD.PS.SRC.3#3 >>UUT sent PS_RDY within tSrcTransition_Max(35ms) + tSrcSwapStdbby_Max(650ms) time.The time interval is 0.0485s, start time 2.3299s, stop time 2.3784s	PASS
		Source capability check after PR_SWAP - TEST.PD.PS.SRC.3#4	PASS
		Accept Check for PR_Swap - TEST.PD.PS.SRC.3#5	PASS
		Accept Check for PR_Swap - TEST.PD.PS.SRC.3#6	PASS
		Accept Check for PR_Swap - TEST.PD.PS.SRC.3#7	PASS
		Current drawn by the DUT - TEST.PD.PS.SRC.3#8 >>Supply Type is Fixed	PASS
		Request Check - TEST.PD.PS.SRC.3#9	PASS
		Accept Check - TEST.PD.PS.SRC.3#10	PASS
		Accept Check - TEST.PD.PS.SRC.3#11	PASS
		Accept Check - TEST.PD.PS.SRC.3#12 >>Current drawn by UUT did not exceed previously contracted current (2.01mA) measured from time 8.10293571s to 8.30293571s	PASS
		Current drawn by the DUT - TEST.PD.PS.SRC.3#13 >>Supply Type is Fixed	PASS
		Request Check - TEST.PD.PS.SRC.3#14 >>Tester sent SourceCap message Packet 78 UUT sent Request message Packet 80	PASS
		Accept Check - TEST.PD.PS.SRC.3#17 >>Tester sent Accept message Packet 82	PASS

SI No	Test ID	Test Name	Test Result
		Current drawn by the DUT - TEST.PD.PS.SRC.3#18 >>Tester sent PS_RDY message Packet 84 Supply Type is Fixed	PASS
		Current drawn by the DUT - TEST.PD.PS.SRC.3#19 >UUT is drawing power less than pSnkSusp max 25mW	PASS
		Rev3ChkdSrc	PASS
		PR_Swap Response Check - TEST.PD.PS.SRC.3#1 >>DRP UUT sent Accept for PR_Swap message.	PASS
		UUT PS_RDY Check - TEST.PD.PS.SRC.3#2 >>UUT respond PS_RDY message to PR_Swap after VBUS voltage to vSafe0V(0V - 0.8V).The present voltage is 0.3628V	PASS
		Tester PS_RDY Check - TEST.PD.PS.SRC.3#3 >>UUT sent PS_RDY within tSrcTransition_Max(35ms) + tSrcSwapStdbby_Max(650ms) time.The time interval is 0.0487s, start time 21.3356s, stop time 21.3843s	PASS
		Source capability check after PR_SWAP - TEST.PD.PS.SRC.3#4	PASS
		Accept Check for PR_Swap - TEST.PD.PS.SRC.3#5	PASS
		Accept Check for PR_Swap - TEST.PD.PS.SRC.3#6	PASS
		Accept Check for PR_Swap - TEST.PD.PS.SRC.3#7	PASS
		Current drawn by the DUT - TEST.PD.PS.SRC.3#8 >>Supply Type is Fixed	PASS
		Request Check - TEST.PD.PS.SRC.3#9	PASS
		Accept Check - TEST.PD.PS.SRC.3#10	PASS
		Accept Check - TEST.PD.PS.SRC.3#11	PASS
		Accept Check - TEST.PD.PS.SRC.3#12 >>Current drawn by UUT did not exceed previously contracted current (2.01mA) measured from time 27.13780461s to 27.33780461s	PASS
		Current drawn by the DUT - TEST.PD.PS.SRC.3#13 >>Supply Type is Fixed	PASS

SI No	Test ID	Test Name	Test Result
		Request Check - TEST.PD.PS.SRC.3#14 >>Tester sent SourceCap message Packet 180 UUT sent Request message Packet 182	PASS
		Accept Check - TEST.PD.PS.SRC.3#17 >>Tester sent Accept message Packet 184	PASS
		Current drawn by the DUT - TEST.PD.PS.SRC.3#18 >>Tester sent PS_RDY message Packet 186 Supply Type is Fixed	PASS
		Current drawn by the DUT - TEST.PD.PS.SRC.3#19 >UUT is drawing power less than pSnkSusp max 25mW	PASS
93	TEST.PD.PS.SRC.4	TEST.PD.PS.SRC.4 Source Behavior with Capability Mismatch Bit	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.111s and SourceCap time: 1.172s at protocol index #19 [PASS] Max = 250ms. Obtained time difference is 60.827ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 > Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 6.633s and SourceCap time: 6.696s at protocol index #67 [PASS] Max = 250ms. Obtained time difference is 62.494ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS

SI No	Test ID	Test Name	Test Result
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		Rev2Src	PASS
		Check Accept - TEST.PD.PS.SRC.4#1	NA
		Check PS_RDY - TEST.PD.PS.SRC.4#2	NA
		Check PS_RDY recive time - TEST.PD.PS.SRC.4#3	NA
		Check Accept - TEST.PD.PS.SRC.4#4 >>UUT sent Accept message at protocol index 45	PASS
		Check PS_RDY - TEST.PD.PS.SRC.4#5 >>UUT sent PS_RDY message at protocol index 47	PASS
		Check PS_RDY receive time - TEST.PD.PS.SRC.4#6 >>[PASS] Max = 325ms. Obtained time difference is 31.338ms Packet 47	PASS
		Check SourceCap matches VIF - TEST.PD.PS.SRC.4#7 >DUT to send the SourceCap within 2s	PASS
		Rev3ChkdSrc	PASS
		Check Accept - TEST.PD.PS.SRC.4#1	NA
		Check PS_RDY - TEST.PD.PS.SRC.4#2	NA
		Check PS_RDY recive time - TEST.PD.PS.SRC.4#3	NA
		Check Accept - TEST.PD.PS.SRC.4#4 >>UUT sent Accept message at protocol index 95	PASS
		Check PS_RDY - TEST.PD.PS.SRC.4#5 >>UUT sent PS_RDY message at protocol index 97	PASS
		Check PS_RDY receive time - TEST.PD.PS.SRC.4#6 >>[PASS] Max = 325ms. Obtained time difference is 30.528ms Packet 97	PASS
		Check SourceCap matches VIF - TEST.PD.PS.SRC.4#7 >UUT to send the SourceCap message	PASS
94	TEST.PD.PS.SRC.5	TEST.PD.PS.SRC.5 Source Hard Reset Test	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_2_0 Rev2Src	PASS

SI No	Test ID	Test Name	Test Result
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.17s and SourceCap time: 1.234s at protocol index #19 [PASS] Max = 250ms. Obtained time difference is 64.16ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	NA
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	NA
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	NA
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 5.659s and SourceCap time: 5.722s at protocol index #84 [PASS] Max = 250ms. Obtained time difference is 63.327ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	NA
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	NA
		Rev2Src	PASS
		Check VBUS stays within present valid voltage range - TEST.PD.PS.SRC.5#1	NA
		Check VBUS reaches vSafe0V max - TEST.PD.PS.SRC.5#2	NA
		Check VBUS rises above vSafe0V max - TEST.PD.PS.SRC.5#3	NA
		Check VBUS reaches vSafe5V - TEST.PD.PS.SRC.5#4	NA
		Source Capabilities message - TEST.PD.PS.SRC.5#5	NA
		Highest Fixed PDO Contract check - TEST.PD.PS.SRC.5#6 >>DUT has no highest fixed PDO availability	PASS
		Check VBUS stays within present valid voltage range - TEST.PD.PS.SRC.5#7	PASS
		Check VBUS reaches vSafe5V max - TEST.PD.PS.SRC.5#8	PASS
		Check VBUS reaches vSafe0V max - TEST.PD.PS.SRC.5#9	PASS
		Check VBUS rises above vSafe0V max - TEST.PD.PS.SRC.5#10	PASS
		Check VBUS reaches vSafe5V - TEST.PD.PS.SRC.5#11	PASS
		Source Capabilities message - TEST.PD.PS.SRC.5#12	PASS
		Rev3ChkdSrc	PASS

SI No	Test ID	Test Name	Test Result
		Check VBUS stays within present valid voltage range - TEST.PD.PS.SRC.5#1	NA
		Check VBUS reaches vSafe0V max - TEST.PD.PS.SRC.5#2	NA
		Check VBUS rises above vSafe0V max - TEST.PD.PS.SRC.5#3	NA
		Check VBUS reaches vSafe5V - TEST.PD.PS.SRC.5#4	NA
		Source Capabilities message - TEST.PD.PS.SRC.5#5	NA
		Highest Fixed PDO Contract check - TEST.PD.PS.SRC.5#6 >>DUT has no highest fixed PDO availability	PASS
		Check VBUS stays within present valid voltage range - TEST.PD.PS.SRC.5#7	PASS
		Check VBUS reaches vSafe5V max - TEST.PD.PS.SRC.5#8	PASS
		Check VBUS reaches vSafe0V max - TEST.PD.PS.SRC.5#9	PASS
		Check VBUS rises above vSafe0V max - TEST.PD.PS.SRC.5#10	PASS
		Check VBUS reaches vSafe5V - TEST.PD.PS.SRC.5#11	PASS
		Source Capabilities message - TEST.PD.PS.SRC.5#12	PASS
95	TEST.PD.PS.SNK.1	TEST.PD.PS.SNK.1 PDO Transition	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk >>SourceCap Packet14	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet16	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet61	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet63	PASS
		Rev2Snk	PASS
		Get_Sink_Cap response check - TEST.PD.PS.SNK.1#1 >>UUT successfully respond to Get_Sink_Cap message	PASS
		UUT Request message check - TEST.PD.PS.SNK.1#2	PASS
		Contracted current level check - TEST.PD.PS.SNK.1#5 >>Tester sent PS_RDY message Packet 36 UUT is drawing current less than previously contracted current (100mA)	PASS

SI No	Test ID	Test Name	Test Result
		Current level check(5Sec) - TEST.PD.PS.SNK.1#6	PASS
		UUT Request message check - TEST.PD.PS.SNK.1#7	PASS
		After tSrcTransition_Min iSnkSusp_Max check - TEST.PD.PS.SNK.1#10	PASS
		Current level check(5Sec) - TEST.PD.PS.SNK.1#11	PASS
		UUT Request position check - TEST.PD.PS.SNK.1#12	PASS
		UUT Request PDP check - TEST.PD.PS.SNK.1#13	PASS
		EPR Mode Capable bit check - TEST.PD.PS.SNK.1#14	NA
		UUT EPR Mode check - TEST.PD.PS.SNK.1#15	PASS
		SoftReset check - TEST.PD.PS.SNK.1#16 >>UUT didn't initiated the EPR_Mode_Enter AMS and VIF field is EPR_Supported_As_Snk set to NO.	PASS
		Rev3ChkdSnk	PASS
		Get_Sink_Cap response check - TEST.PD.PS.SNK.1#1 >>UUT successfully respond to Get_Sink_Cap message	PASS
		UUT Request message check - TEST.PD.PS.SNK.1#2	PASS
		Contracted current level check - TEST.PD.PS.SNK.1#5 >>Tester sent PS_RDY message Packet 103 UUT is drawing current less than previously contracted current (100mA)	PASS
		Current level check(5Sec) - TEST.PD.PS.SNK.1#6	PASS
		UUT Request message check - TEST.PD.PS.SNK.1#7 >UUT to respond SourceCap message. Packet297	PASS
		UUT Request position check - TEST.PD.PS.SNK.1#12	PASS
		UUT Request PDP check - TEST.PD.PS.SNK.1#13	PASS
		EPR Mode Capable bit check - TEST.PD.PS.SNK.1#14	PASS
		UUT EPR Mode check - TEST.PD.PS.SNK.1#15	PASS
		SoftReset check - TEST.PD.PS.SNK.1#16 >>UUT didn't initiated the EPR_Mode_Enter AMS and VIF field is EPR_Supported_As_Snk set to NO.	PASS
96	TEST.PD.PS.SNK.2	TEST.PD.PS.SNK.2 Initial Sink PDO Transition	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk >>SourceCap Packet14	PASS

SI No	Test ID	Test Name	Test Result
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet16	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet73	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet75	PASS
		Rev2Snk	PASS
		PR_Swap message response check - TEST.PD.PS.SNK.2#1 >>UUT respond Accept to PR_Swap message.Accepts_PR_Swap_As_Snk field value is YES	PASS
		UUT vSafe5V check - TEST.PD.PS.SNK.2#2 >>UUT applied vSafe5V before sending PS_RDY.The Obtained VBUS 05.062571V at 3.6546534	PASS
		UUT tNewSrc check - TEST.PD.PS.SNK.2#3 >>UUT sent PS_RDY within tNewSrc [275ms].Obtained interval 0.073974	PASS
		UUT Accept message check - TEST.PD.PS.SNK.2#4 >>PDO #1: UUT respond Accept to Request message	PASS
		tPSTransition timer check - TEST.PD.PS.SNK.2#5 >>PDO #1: UUT sent PS_RDY message within 450ms. The obtained interval 31.5046399999996ms	PASS
		vSrcNew timer check - TEST.PD.PS.SNK.2#6 >>PDO #1: Measured VBUS voltage at Accept message: 5.07V. Expected range[4.75V ~ 5.5V]	PASS
		vSrcValid check - TEST.PD.PS.SNK.2#8 >>[PASS]:vSrcValid limits until tSrcSettle_Max(275ms): Obtained voltage = 5.069V, Expected voltage limit[4.75~5.5].vSrcValid Measured until 4.8780683s	PASS
		vSrcNew limits check - TEST.PD.PS.SNK.2#9 >>[PASS]:vSrcNew or vPpsNew limits between tSrcSettle_Max(275ms) and tSrcSettle_Max+100ms: Obtained voltage = 5.0687V, Expected voltage limit[4.75~5.5].vSrcNew or vPpsNew Measured from 4.8780683s to 5.2530683s	PASS
		UUT PS_RDY message check - TEST.PD.PS.SNK.2#10 >>PDO #1: Measured VBUS voltage at PS_RDY 5.07. Expected range[4.75V ~ 5.5V]	PASS
		Accept check - TEST.PD.PS.SNK.2#11	PASS

SI No	Test ID	Test Name	Test Result
		PS_RDY check - TEST.PD.PS.SNK.2#12	PASS
		PS_RDY check - TEST.PD.PS.SNK.2#13	PASS
		Rev3ChkdSnk	PASS
		PR_Swap message response check - TEST.PD.PS.SNK.2#1 >>UUT respond Accept to PR_Swap message.Accepts_PR_Swap_As_Snk field value is YES	PASS
		UUT vSafe5V check - TEST.PD.PS.SNK.2#2 >>UUT applied vSafe5V before sending PS_RDY.The Obtained VBUS 05.061957V at 9.31220184	PASS
		UUT tNewSrc check - TEST.PD.PS.SNK.2#3 >>UUT sent PS_RDY within tNewSrc [275ms].Obtained interval 0.067651	PASS
		UUT Accept message check - TEST.PD.PS.SNK.2#4 >>PDO #1: UUT respond Accept to Request message	PASS
		tPSTransition timer check - TEST.PD.PS.SNK.2#5 >>PDO #1: UUT sent PS_RDY message within 450ms. The obtained interval 31.2826699999995ms	PASS
		vSrcNew timer check - TEST.PD.PS.SNK.2#6 >>PDO #1: Measured VBUS voltage at Accept message: 5.07V. Expected range[4.75V ~ 5.5V]	PASS
		vSrcValid check - TEST.PD.PS.SNK.2#8 >>[PASS]:vSrcValid limits until tSrcSettle_Max(275ms): Obtained voltage = 5.0688V, Expected voltage limit[4.75~5.5].vSrcValid Measured until 10.54023079s	PASS
		vSrcNew limits check - TEST.PD.PS.SNK.2#9 >>[PASS]:vSrcNew or vPpsNew limits between tSrcSettle_Max(275ms) and tSrcSettle_Max+100ms: Obtained voltage = 5.0687V, Expected voltage limit[4.75~5.5].vSrcNew or vPpsNew Measured from 10.54023079s to 10.91523079s	PASS
		UUT PS_RDY message check - TEST.PD.PS.SNK.2#10 >>PDO #1: Measured VBUS voltage at PS_RDY 5.07. Expected range[4.75V ~ 5.5V]	PASS
		Accept check - TEST.PD.PS.SNK.2#11	PASS
		PS_RDY check - TEST.PD.PS.SNK.2#12	PASS
		PS_RDY check - TEST.PD.PS.SNK.2#13	PASS

SI No	Test ID	Test Name	Test Result
97	TEST.PD.PS.SNK.3	TEST.PD.PS.SNK.3 Multiple Request Load Test Post PR Swap	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_2_0 Rev2Snk >>SourceCap Packet14	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet16	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet138	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet140	PASS
		Rev2Snk	PASS
		PR_Swap message response check - [TEST.PD.PS.SNK.3#1 >>UUT respond Accept to PR_Swap message.Accepts_PR_Swap_As_Snk field value is YES	PASS
		UUT vSafe5V check - TEST.PD.PS.SNK.3#2 >>UUT applied vSafe5V before sending PS_RDY	PASS
		tNewSrc timer check - TEST.PD.PS.SNK.3#3 >>UUT sent PS_RDY within tNewSrc [275ms].Obtained interval 0.068485	PASS
		Current decrease transition check - TEST.PD.PS.SNK.3#4 >>[PASS]PDO #1[0.37A load]: Measured VBUS voltage after decrease current to new value: 5V at time 7.97585761s. Expected range[4.75V ~ 5.5V] [PASS]PDO #1[0.25A load]: Measured VBUS voltage after decrease current to new value: 5.02V at time 8.59871973s. Expected range[4.75V ~ 5.5V] [PASS]PDO #1[0.12A load]: Measured VBUS voltage after decrease current to new value: 5.04V at time 9.22295786s. Expected range[4.75V ~ 5.5V] [PASS]PDO #1[0A load]: Measured VBUS voltage after decrease current to new value: 5.07V at time 9.84536881s. Expected range[4.75V ~ 5.5V]	PASS

SI No	Test ID	Test Name	Test Result
		Current increase transition check - TEST.PD.PS.SNK.3#5 >>[PASS]PDO #1[0.12A load]: Measured VBUS voltage after increase current to new value: 5.04V at time 5.5149019s. Expected range[4.75V ~ 5.5V] [PASS]PDO #1[0.25A load]: Measured VBUS voltage after increase current to new value: 5.02V at time 6.13887766s. Expected range[4.75V ~ 5.5V] [PASS]PDO #1[0.37A load]: Measured VBUS voltage after increase current to new value: 5V at time 6.7616982s. Expected range[4.75V ~ 5.5V] [PASS]PDO #1[0.5A load]: Measured VBUS voltage after increase current to new value: 4.98V at time 7.38336038s. Expected range[4.75V ~ 5.5V]	PASS
		UUT Accept message check - TEST.PD.PS.SNK.3#12 >>PDO #1[0A load]: UUT respond Accept to Request message PDO #1[0.12A load]: UUT respond Accept to Request message PDO #1[0.25A load]: UUT respond Accept to Request message PDO #1[0.37A load]: UUT respond Accept to Request message PDO #1[0.5A load]: UUT respond Accept to Request message PDO #1[0.37A load]: UUT respond Accept to Request message PDO #1[0.25A load]: UUT respond Accept to Request message PDO #1[0.12A load]: UUT respond Accept to Request message PDO #1[0A load]: UUT respond Accept to Request message	PASS

SI No	Test ID	Test Name	Test Result
		tPSTransition timer check - TEST.PD.PS.SNK.3#13 >>PDO #1[0A load]: UUT respond PS_RDY message within 450ms. The obtained interval 31.6077ms PDO #1[0.12A load]: UUT respond PS_RDY message within 450ms. The obtained interval 31.6037ms PDO #1[0.25A load]: UUT respond PS_RDY message within 450ms. The obtained interval 31.5243ms PDO #1[0.37A load]: UUT respond PS_RDY message within 450ms. The obtained interval 31.4945ms PDO #1[0.5A load]: UUT respond PS_RDY message within 450ms. The obtained interval 29.9531ms PDO #1[0.37A load]: UUT respond PS_RDY message within 450ms. The obtained interval 31.5531ms PDO #1[0.25A load]: UUT respond PS_RDY message within 450ms. The obtained interval 31.4323ms PDO #1[0.12A load]: UUT respond PS_RDY message within 450ms. The obtained interval 31.6273ms PDO #1[0A load]: UUT respond PS_RDY message within 450ms. The obtained interval 31.5807ms	PASS
		tPSTransition timer check - TEST.PD.PS.SNK.3#14	PASS
		Rev3ChkdSnk	PASS
		PR_Swap message response check - [TEST.PD.PS.SNK.3#1 >>UUT respond Accept to PR_Swap message.Accepts_PR_Swap_As_Snk field value is YES	PASS
		UUT vSafe5V check - TEST.PD.PS.SNK.3#2 >>UUT applied vSafe5V before sending PS_RDY	PASS
		tNewSrc timer check - TEST.PD.PS.SNK.3#3 >>UUT sent PS_RDY within tNewSrc [275ms].Obtained interval 0.068429	PASS

SI No	Test ID	Test Name	Test Result
		Current decrease transition check - TEST.PD.PS.SNK.3#4 >>[PASS]PDO #1[0.37A load]: Measured VBUS voltage after decrease current to new value: 5V at time 18.61687241s. Expected range[4.75V ~ 5.5V] [PASS]PDO #1[0.25A load]: Measured VBUS voltage after decrease current to new value: 5.02V at time 19.24323216s. Expected range[4.75V ~ 5.5V] [PASS]PDO #1[0.12A load]: Measured VBUS voltage after decrease current to new value: 5.04V at time 19.86305109s. Expected range[4.75V ~ 5.5V] [PASS]PDO #1[0A load]: Measured VBUS voltage after decrease current to new value: 5.07V at time 20.48500124s. Expected range[4.75V ~ 5.5V]	PASS
		Current increase transition check - TEST.PD.PS.SNK.3#5 >>[PASS]PDO #1[0.12A load]: Measured VBUS voltage after increase current to new value: 5.04V at time 16.15554555s. Expected range[4.75V ~ 5.5V] [PASS]PDO #1[0.25A load]: Measured VBUS voltage after increase current to new value: 5.02V at time 16.77973888s. Expected range[4.75V ~ 5.5V] [PASS]PDO #1[0.37A load]: Measured VBUS voltage after increase current to new value: 5V at time 17.40277703s. Expected range[4.75V ~ 5.5V] [PASS]PDO #1[0.5A load]: Measured VBUS voltage after increase current to new value: 4.98V at time 18.02630156s. Expected range[4.75V ~ 5.5V]	PASS
		UUT Accept message check - TEST.PD.PS.SNK.3#12 >>PDO #1[0A load]: UUT respond Accept to Request message PDO #1[0.12A load]: UUT respond Accept to Request message PDO #1[0.25A load]: UUT respond Accept to Request message PDO #1[0.37A load]: UUT respond Accept to Request message PDO #1[0.5A load]: UUT respond Accept to Request message PDO #1[0.37A load]: UUT respond Accept to Request message PDO #1[0.25A load]: UUT respond Accept to Request message PDO #1[0.12A load]: UUT respond Accept to Request message PDO #1[0A load]: UUT respond Accept to Request message	PASS

SI No	Test ID	Test Name	Test Result
		tPSTransition timer check - TEST.PD.PS.SNK.3#13 >>PDO #1[0A load]: UUT respond PS_RDY message within 450ms. The obtained interval 31.0261ms PDO #1[0.12A load]: UUT respond PS_RDY message within 450ms. The obtained interval 30.6085ms PDO #1[0.25A load]: UUT respond PS_RDY message within 450ms. The obtained interval 30.6547ms PDO #1[0.37A load]: UUT respond PS_RDY message within 450ms. The obtained interval 30.8507ms PDO #1[0.5A load]: UUT respond PS_RDY message within 450ms. The obtained interval 31.9001ms PDO #1[0.37A load]: UUT respond PS_RDY message within 450ms. The obtained interval 31.4453ms PDO #1[0.25A load]: UUT respond PS_RDY message within 450ms. The obtained interval 33.7187ms PDO #1[0.12A load]: UUT respond PS_RDY message within 450ms. The obtained interval 32.3227ms PDO #1[0A load]: UUT respond PS_RDY message within 450ms. The obtained interval 30.5021ms	PASS
		tPSTransition timer check - TEST.PD.PS.SNK.3#14	PASS
98	TEST.PD.EPR.SRC3.1	TEST.PD.EPR.SRC3.1 EPR Entry Process - UUT as VCONN Source	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.234s and SourceCap time: 1.298s at protocol index #19 [PASS] Max = 250ms. Obtained time difference is 64.16ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3UnchkdSrc	PASS

SI No	Test ID	Test Name	Test Result
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 9.735s and SourceCap time: 9.797s at protocol index #84 [PASS] Max = 250ms. Obtained time difference is 62.494ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 > Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		Rev3ChkdSrc >> Rev3ChkdSrc sequence starts from protocol index 5	PASS
		EPR Mode check - TEST.PD.EPR.SRC3.1#2 >>Tester sent EPR_Mode Enter message Packet 49 UUT did respond with Not_Supported at the protocol index 51 and VIF field EPR_Supported_As_Src is NO Packet 51	PASS
		Vconn_Swap message - TEST.PD.EPR.SRC3.1#3	PASS
		Discover ID SOP1 message check - TEST.PD.EPR.SRC3.1#4	PASS
		EPR Mode Enter Succeeded message check - TEST.PD.EPR.SRC3.1#5	PASS
		EPR_Source_Capability message check - TEST.PD.EPR.SRC3.1#6	PASS
		Accept message check - TEST.PD.EPR.SRC3.1#7	PASS
		PS_Rdy message check - TEST.PD.EPR.SRC3.1#8	PASS
		Source Cap message check - TEST.PD.EPR.SRC3.1#9	PASS
		Source Cap message Detail check - TEST.PD.EPR.SRC3.1#10	PASS
		Source Cap message Detail check - TEST.PD.EPR.SRC3.1#11	PASS
		Wait response check - TEST.PD.EPR.SRC3.1#12	PASS
		EPR Get Sourcecap Check - TEST.PD.EPR.SRC3.1#13 >>Tester sent Extended_Control EPR_Get_Source_Cap message Packet 44 UUT responded with Not_Supported.UUT is DRP , VIF field EPR_Supported_As_Src is NO and VIF field EPR_Supported_As_Snk is NO	PASS
		Rev3UnchkdSrc >> Rev3UnchkdSrc sequence starts from protocol index 70	PASS

SI No	Test ID	Test Name	Test Result
		EPR Mode check - TEST.PD.EPR.SRC3.1#2 >>Tester sent EPR_Mode Enter message Packet 114 UUT did respond with Not_Supported at the protocol index 116 and VIF field EPR_Supported_As_Src is NO Packet 116	PASS
		Vconn_Swap message - TEST.PD.EPR.SRC3.1#3	PASS
		Discover ID SOP1 message check - TEST.PD.EPR.SRC3.1#4	PASS
		EPR Mode Enter Succeeded message check - TEST.PD.EPR.SRC3.1#5	PASS
		EPR_Source_Capability message check - TEST.PD.EPR.SRC3.1#6	PASS
		Accept message check - TEST.PD.EPR.SRC3.1#7	PASS
		PS_Rdy message check - TEST.PD.EPR.SRC3.1#8	PASS
		Source Cap message check - TEST.PD.EPR.SRC3.1#9	PASS
		Source Cap message Detail check - TEST.PD.EPR.SRC3.1#10	PASS
		Source Cap message Detail check - TEST.PD.EPR.SRC3.1#11	PASS
		Wait response check - TEST.PD.EPR.SRC3.1#12	PASS
		EPR Get Sourcecap Check - TEST.PD.EPR.SRC3.1#13 >>Tester sent Extended_Control EPR_Get_Source_Cap message Packet 109 UUT responded with Not_Supported.UUT is DRP , VIF field EPR_Supported_As_Src is NO and VIF field EPR_Supported_As_Snk is NO	PASS
99	TEST.PD.EPR.SRC3.2	TEST.PD.EPR.SRC3.2 EPR Entry Process - Tester as VCONN Source --- EPR_Supported_As_Src is set to NO in VIF	NA
100	TEST.PD.EPR.SRC3.3	TEST.PD.EPR.SRC3.3 EPR Entry failed - EPR Mode Capable bit not set in RDO --- EPR_Supported_As_Src is set to NO in VIF	NA
101	TEST.PD.EPR.SRC3.4	TEST.PD.EPR.SRC3.4 EPR Entry failed – Tester as VCONN source --- EPR_Supported_As_Src is set to NO in VIF	NA
102	TEST.PD.EPR.SRC3.5	TEST.PD.EPR.SRC3.5 EPR Entry Failed - EPR_Mode(Reserved) message --- EPR_Supported_As_Src is set to NO in VIF	NA
103	TEST.PD.EPR.SRC3.6	TEST.PD.EPR.SRC3.6 EPR Entry Failed - Cable not EPR capable --- EPR_Supported_As_Src is set to NO in VIF	NA
104	TEST.PD.EPR.SRC3.7	TEST.PD.EPR.SRC3.7 EPR Entry Failed - Interrupted by EPR_Get_Sink_Cap message	NA

SI No	Test ID	Test Name	Test Result
		--- EPR_Supported_As_Src is set to NO in VIF	
105	TEST.PD.EPR.SRC3.8	TEST.PD.EPR.SRC3.8 EPR mode - Request message response	NA
		--- EPR_Supported_As_Src is set to NO in VIF	
106	TEST.PD.EPR.SRC3.9	TEST.PD.EPR.SRC3.9 EPR mode - EPR_Get_Source_Cap message	NA
		--- EPR_Supported_As_Src is set to NO in VIF	
107	TEST.PD.EPR.SRC3.10	TEST.PD.EPR.SRC3.10 SPR mode - EPR_Get_Source_Cap message	PASS
		COMMON.PROC.BU.1	PASS
		COMMON.PROC.BU.1 - REVISION_3_0 Rev3ChkdSrc	PASS
		First source capability timer - COMMON.PROC.BU.1#1 >>Vbus up time: 1.138s and SourceCap time: 1.202s at protocol index #19 [PASS] Max = 250ms. Obtained time difference is 63.327ms	PASS
		DUT responded with accept message - COMMON.PROC.BU.1#2 >Please check the capture and confirm	PASS
		tSrcTransReq timer check - COMMON.PROC.BU.1#3 >Please check the capture and confirm	PASS
		Rev3ChkSrc	PASS
		EPR Mode Message Response - TEST.PD.EPR.SRC3.10#1 >>Tester sent Extended_Control EPR_Get_Source_Cap message Packet 44 UUT responded with Not_Supported.UUT is DRP , VIF field EPR_Supported_As_Src is NO and VIF field EPR_Supported_As_Snk is NO at protocol index 46	PASS
		DUT initiates Hard reset - TEST.PD.EPR.SRC3.10#2	NA
108	TEST.PD.EPR.SRC3.11	TEST.PD.EPR.SRC3.11 EPR Mode Exit by EPR_Mode_Exit message	NA
		--- EPR_Supported_As_Src is set to NO in VIF	
109	TEST.PD.EPR.SRC3.12	TEST.PD.EPR.SRC3.12 EPR mode - Get_Source_Cap message and Request message response	NA
		--- EPR_Supported_As_Src is set to NO in VIF	
110	TEST.PD.EPR.SRC3.13	TEST.PD.EPR.SRC3.13 EPR mode - tSourceEPRKeepAlive Timeout	NA
		--- EPR_Supported_As_Src is set to NO in VIF	
111	TEST.PD.EPR.SRC3.14	TEST.PD.EPR.SRC3.14 EPR mode - EPR_Request with Incorrect copy of PDO	NA
		--- EPR_Supported_As_Src is set to NO in VIF	

SI No	Test ID	Test Name	Test Result
112	TEST.PD.EPR.SRC3.15	TEST.PD.EPR.SRC3.15 DiscoverIdentityCounter and DiscoverIdentityTimer check for SOP1	NA
		--- EPR_Supported_As_Src is set to NO in VIF Captive_Cable is set to NO in VIF	
113	TEST.PD.EPR.SRC3.16	TEST.PD.EPR.SRC3.16 PR_Swap for the UUT as EPR Source	NA
		--- EPR_Supported_As_Src is set to NO in VIF	
114	TEST.PD.EPR.SNK3.1	TEST.PD.EPR.SNK3.1 EPR Entry Process - Success	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet15	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet17	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3UnchkdSnk >>SourceCap Packet61	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet63	PASS
		Rev3ChkdSnk >> Rev3ChkdSnk sequence starts from protocol index 5	PASS
		EPR Mode Capable check - TEST.PD.EPR.SNK3.1#1 >>EPR mode capable field is set to 0 in the Request message sent by UUT at the protocol index 17, VIF field EPR_Supported_As_Snk is set to NO	PASS
		Voltage value during the Accept at the protocol in index 19 >>Measured voltage value is 5.0134V at time 1.04707428s	PASS
		Voltage value during the PS_RDY at the protocol in index 21 >>Measured voltage value is 4.9991V at time 1.37007658s [PASS] Measured Vbus voltage is 4.999V and expected is [Min - 4.5 and Max - 5.5]V	PASS
		EPR Mode Enter check - TEST.PD.EPR.SNK3.1#2	PASS
		Discover ID SOP1 check - TEST.PD.EPR.SNK3.1#3	PASS
		tSinkEPRKeepAlive.max check - TEST.PD.EPR.SNK3.1#4	PASS
		EPR Keep_Alive message check - TEST.PD.EPR.SNK3.1#5	PASS
		EPR_Request message check - TEST.PD.EPR.SNK3.1#6	PASS
		SourceCap message check - TEST.PD.EPR.SNK3.1#7	PASS
		EPR contract negotiation check - TEST.PD.EPR.SNK3.1#8	PASS

SI No	Test ID	Test Name	Test Result
		SPR contract negotiation - TEST.PD.EPR.SNK3.1#9	PASS
		EPR_Source_Capabilities Message check - TEST.PD.EPR.SNK3.1#10	PASS
		Get_EPR_SinkCap Message check - TEST.PD.EPR.SNK3.1#11 >>UUT sent Get_SourceCap_Extended EPR_Get_Sink_Cap message Packet 29	PASS
		Rev3UnchkdSnk >> Rev3UnchkdSnk sequence starts from protocol index 51	PASS
		EPR Mode Capable check - TEST.PD.EPR.SNK3.1#1 >>EPR mode capable field is set to 0 in the Request message sent by UUT at the protocol index 63, VIF field EPR_Supported_As_Snk is set to NO	PASS
		Voltage value during the Accept at the protocol in index 65 >>Measured voltage value is 5V at time 9.66509245s	PASS
		Voltage value during the PS_RDY at the protocol in index 67 >>Measured voltage value is 4.9997V at time 9.98809471s [PASS] Measured Vbus voltage is 5V and expected is [Min - 4.5 and Max - 5.5]V	PASS
		EPR Mode Enter check - TEST.PD.EPR.SNK3.1#2	PASS
		Discover ID SOP1 check - TEST.PD.EPR.SNK3.1#3	PASS
		tSinkEPRKeepAlive.max check - TEST.PD.EPR.SNK3.1#4	PASS
		EPR Keep_Alive message check - TEST.PD.EPR.SNK3.1#5	PASS
		EPR_Request message check - TEST.PD.EPR.SNK3.1#6	PASS
		SourceCap message check - TEST.PD.EPR.SNK3.1#7	PASS
		EPR contract negotiation check - TEST.PD.EPR.SNK3.1#8	PASS
		SPR contract negotiation - TEST.PD.EPR.SNK3.1#9	PASS
		EPR_Source_Capabilities Message check - TEST.PD.EPR.SNK3.1#10	PASS
		Get_EPR_SinkCap Message check - TEST.PD.EPR.SNK3.1#11 >>UUT sent Get_SourceCap_Extended EPR_Get_Sink_Cap message Packet 75	PASS
115	TEST.PD.EPR.SNK3.2	TEST.PD.EPR.SNK3.2 EPR Entry Fail tEnterEPR Timer Timeout	NA
		--- EPR_Supported_As_Snk is set to NO in VIF	
116	TEST.PD.EPR.SNK3.3	TEST.PD.EPR.SNK3.3 EPR Fail by EPR Enter Failed Message	NA
		--- EPR_Supported_As_Snk is set to NO in VIF	
117	TEST.PD.EPR.SNK3.4	TEST.PD.EPR.SNK3.4 EPR Entry Fail tFirstSourceCap Timer Timeout	NA
		--- EPR_Supported_As_Snk is set to NO in VIF	

SI No	Test ID	Test Name	Test Result
118	TEST.PD.EPR.SNK3.5	TEST.PD.EPR.SNK3.5 EPR Exit by Incorrect EPR Source Cap	NA
		--- EPR_Supported_As_Snk is set to NO in VIF	
119	TEST.PD.EPR.SNK3.6	TEST.PD.EPR.SNK3.6 EPR Exit by EPR Exit Message	NA
		--- EPR_Supported_As_Snk is set to NO in VIF	
120	TEST.PD.EPR.SNK3.8	TEST.PD.EPR.SNK3.8 EPR Exit by Source Cap Message	NA
		--- EPR_Supported_As_Snk is set to NO in VIF	
121	TEST.PD.EPR.SNK3.9	TEST.PD.EPR.SNK3.9 EPR Entry failed due to SourceCap	NA
		--- EPR_Supported_As_Snk is set to NO in VIF	
122	TEST.PD.EPR.SNK3.10	TEST.PD.EPR.SNK3.10 EPR Exit fail due to SinkWaitCapTimer timeout	NA
		--- EPR_Supported_As_Snk is set to NO in VIF	
123	TEST.PD.EPR.SNK3.11	TEST.PD.EPR.SNK3.11 PR_Swap for the UUT as the EPR Sink	NA
		--- EPR_Supported_As_Snk is set to NO in VIF	
124	TEST.PD.PS.EPR.SRC3.1	TEST.PD.PS.EPR.SRC3.1 Multiple EPR Request Load Test	NA
		--- EPR_Supported_As_Src is set to NO in VIF	
125	TEST.PD.PS.EPR.SRC3.2	TEST.PD.PS.EPR.SRC3.2 PDO Transitions in EPR Mode	NA
		--- EPR_Supported_As_Src is set to NO in VIF	
126	TEST.PD.FRS.SRC3.1	TEST.PD.FRS.SRC3.1 Normal Conditions	NA
127	TEST.PD.FRS.SRC3.2	TEST.PD.FRS.SRC3.2 Provider Only Checks	NA
128	TEST.PD.FRS.SRC3.3	TEST.PD.FRS.SRC3.3 GoodCRC Not Sent In Response To Accept	NA
129	TEST.PD.FRS.SRC3.4	TEST.PD.FRS.SRC3.4 GoodCRC Not Sent In Response To PS_RDY	NA
130	TEST.PD.FRS.SRC3.5	TEST.PD.FRS.SRC3.5 PSSourceOnTimer Deadline	NA
131	TEST.PD.FRS.SRC3.6	TEST.PD.FRS.SRC3.6 PSSourceOnTimer Timeout	NA
132	TEST.PD.FRS.SNK3.1	TEST.PD.FRS.SNK3.1 Normal Conditions	PASS
		COMMON.PROC.BU.2	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk5V >>SourceCap Packet15	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet17	PASS
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnkHiV >>SourceCap Packet55	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet57	PASS
		Rev3ChkdSnk5V	PASS

SI No	Test ID	Test Name	Test Result
		UUT Get_Sink_Cap check - TEST.PD.FRS.SNK3.1#1 >>The VIF parameter FR_Swap_Type_C_Current_Capability_As_Initial_Sink is FR_Swap_Not_Supported Tester draws no current after dropped VBUS .Measured Voltage: 04.4699 and Current -00.1771 from 2.7913779 to 2.7915779. Limit <2.5W	PASS
		VBUS Electrical check - TEST.PD.FRS.SNK3.1#2	PASS
		PDMessage check - TEST.PD.FRS.SNK3.1#3 >>UUT not sending FR_Swap message. The VIF parameter FR_Swap_Type_C_Current_Capability_As_Initial_Sink is FR_Swap_Not_Supported	PASS
		UUT VBus Supply - TEST.PD.FRS.SNK3.1#8 >>The VIF parameter FR_Swap_Type_C_Current_Capability_As_Initial_Sink is FR_Swap_Not_Supported UUT does not supply VBUS	PASS
		Rev3ChkdSnkHiV	PASS
		UUT Get_Sink_Cap check - TEST.PD.FRS.SNK3.1#1 >>The VIF parameter FR_Swap_Type_C_Current_Capability_As_Initial_Sink is FR_Swap_Not_Supported	PASS
133	TEST.PD.FRS.SNK3.2	TEST.PD.FRS.SNK3.2 Normal Conditions, Consumer Only	NA
134	TEST.PD.FRS.SNK3.3	TEST.PD.FRS.SNK3.3 FR_Swap Not Sent --- VIF field FR_Swap_Type_C_Current_Capability_As_Initial_Sink set to 00b	PASS
135	TEST.PD.FRS.SNK3.4	TEST.PD.FRS.SNK3.4 SendResponseTimer Timeout --- VIF field FR_Swap_Type_C_Current_Capability_As_Initial_Sink set to 00b	PASS
136	TEST.PD.FRS.SNK3.5	TEST.PD.FRS.SNK3.5 PSSourceOffTimer Deadline --- VIF field FR_Swap_Type_C_Current_Capability_As_Initial_Sink set to 00b	PASS
137	TEST.PD.FRS.SNK3.6	TEST.PD.FRS.SNK3.6 PSSourceOffTimer Timeout --- VIF field FR_Swap_Type_C_Current_Capability_As_Initial_Sink set to 00b	PASS
138	TEST.PD.FRS.SNK3.7	TEST.PD.FRS.SNK3.7 GoodCRC Not Sent in Response to PS_RDY --- VIF field FR_Swap_Type_C_Current_Capability_As_Initial_Sink set to 00b	PASS
139	TEST.PD.USB4.DRST.1	TEST.PD.USB4.DRST.1 -Data_Reset command response of UFP UUT	PASS
		COMMON.PROC.BU.2	PASS

SI No	Test ID	Test Name	Test Result
		COMMON.PROC.BU.2 - REVISION_3_0 Rev3ChkdSnk >>SourceCap Packet15	PASS
		UUT should respond with request - - COMMON.PROC.BU.2#1 >>Request Packet17	PASS
		Rev3ChkdSnk	PASS
		Data_Reset command response check - TEST.PD.USB4.DRST.1#1 >>Tester sent Data_Reset message Packet 41 UUT sent Not_Supported message Packet 43	PASS
		Data_Reset_Complete response check - TEST.PD.USB4.DRST.1#4	NA
		Data role check - TEST.PD.USB4.DRST.1#5	NA
140	TEST.PD.USB4.DRST.2	TEST.PD.USB4.DRST.2 –Data_Reset command response of UFP UUT, Invalid Sequence	NA
		--- In VIF Data_Reset_Supported field is NO	
141	TEST.PD.USB4.DRST.3	TEST.PD.USB4.DRST.3 –Data_Reset command response of UFP UUT Sourcing Vconn	NA
		--- In VIF Data_Reset_Supported field is NO and VCONN_Swap_To_On_Supported field is NO	
142	TEST.PD.USB4.DRST.4	TEST.PD.USB4.DRST.4 –DataReset command response of UFP UUT Sourcing Vconn – Invalid Sequence	NA
		--- In VIF Data_Reset_Supported field is NO and VCONN_Swap_To_On_Supported field is NO	
143	TEST.PD.USB4.DRST.5	TEST.PD.USB4.DRST.5 –Data_Reset command response of DFP UUT Sourcing Vconn	NA
		--- In VIF Data_Reset_Supported field is NO	
144	TEST.PD.USB4.DRST.6	TEST.PD.USB4.DRST.6 –Data_Reset command response of DFP UUT, UFP Sourcing Vconn	NA
		--- In VIF VCONN_Swap_To_Off_Supported field is NO In VIF Data_Reset_Supported field is NO	
145	TEST.PD.USB4.DRST.7	TEST.PD.USB4.DRST.7 –Data_reset command response of DFP UUT, UFP Sourcing Vconn- VCONNDISCHARGE timer expiry check	NA
		--- In VIF VCONN_Swap_To_Off_Supported field is NO In VIF Data_Reset_Supported field is NO	

SI No	Test ID	Test Name	Test Result
146	TEST.PD.USB4.EUSB.1	TEST.PD.USB4.EUSB.1 – Enter_USB Message response of UFP UUT-Valid Mode	NA
		--- In VIF USB4_UFP_Supported field is NONE	
147	TEST.PD.USB4.EUSB.2	TEST.PD.USB4.EUSB.2 – Enter_USB Message response of UFP UUT-Invalid Mode	NA
		--- In VIF USB4_UFP_Supported field is NONE	
148	TEST.PD.USB4.EUSB.3	TEST.PD.USB4.EUSB.3 – Enter_USB Flow-USB4 DFP Connected to USB4 UFP using an Active Cable	NA
		--- In VIF USB4_DFP_Supported field is NONE	
149	TEST.PD.USB4.EUSB.4	TEST.PD.USB4.EUSB.4 – DR_Swap after Entering USB4 Mode entry	NA
		--- In VIF USB4_UFP_Supported field is NONE In VIF USB4_DFP_Supported field is NONE	
150	TEST.PD.USB4.EUSB.5	TEST.PD.USB4.EUSB.5 – tEnterUSBWait check for USB4 DFP	NA
		--- In VIF USB4_DFP_Supported field is NONE	
151	TEST.PD.USB4.CBL.1	TEST.PD.USB4.CBL.1 – Enter_USB Message response of cable UUT-Valid Mode	NA
152	TEST.PD.USB4.CBL.2	TEST.PD.USB4.CBL.2 – Enter_USB Message response of Cable UUT-Invalid Mode	NA
153	2.1	Common Checks	PASS
		Common_Check_PD_1_Check_Preamble - COMMON.CHECK.PD.1	PASS
		Check Preamble sequence and count - COMMON.CHECK.PD.1#1	PASS
		Common_Check_PD_2_Check_Message_Header - COMMON.CHECK.PD.2	PASS
		Check message header fields - COMMON.CHECK.PD.2#1 >>TEST.PD.PROT.SNK.13: Spec Revision is matching.expected:1, obtained:1. Packet35, TEST.PD.PS.SNK.2: Spec Revision is matching.expected:1, obtained:2. Packet35, TEST.PD.PS.SNK.3: Spec Revision is matching.expected:1, obtained:11. Packet35,	PASS
		Common_Check_PD_3_Check_GoodCRC - COMMON.CHECK.PD.3	PASS
		Check goodCRC response time - COMMON.CHECK.PD.3#1	PASS
		Check goodCRC message header fields - COMMON.CHECK.PD.3#2	PASS

SI No	Test ID	Test Name	Test Result
		Common_Check_PD_4_Check_Atomic_Message_Sequence - COMMON.CHECK.PD.4 >> TEST_PD_PROT_SRC_6_Atomic_Message_Sequence_Request: Check the PD message and confirm the failure.Packet index: 30 TEST_PD_PROT_SRC_6_Atomic_Message_Sequence_Request: Check the PD message and confirm the failure.Packet index: 80	PASS
		Check Atomic message sequence - COMMON.CHECK.PD.4#1 >>TEST.PD.PHY.ALL.2: Exp Time: 15ms and obt: 14.25164ms. Packet18, TEST.PD.PHY.ALL.3: Exp Time: 15ms and obt: 14.62524ms. Packet18,	PASS
		Common_Check_PD_5_Check_Unexpected_Messages_And_Signals - COMMON.CHECK.PD.5	PASS
		Unexpected Soft reset - COMMON.CHECK.PD.5#1	PASS
		Unexpected Hard Reset or a cable reset - COMMON.CHECK.PD.5#2 >>TEST.PD.PROT.SRC.8: Unexpected Hard Reset/Cable reset message. Packet61, 146,	PASS
		Unexpected messages - COMMON.CHECK.PD.5#4	PASS
		Common_Check_PD_6_Control_Message - COMMON.CHECK.PD.6	PASS
		Number of data objects in header should be zero - COMMON.CHECK.PD.6#1	PASS
		Common_Check_PD_7_Source_Capability_Message - COMMON.CHECK.PD.7	PASS
		Check Source Capability message - COMMON.CHECK.PD.7#1 >>TEST.PD.PROT.SNK.2: VIF Pdo's and SourceCap Pdo's are match. Packet27, 71,	PASS
		Check Source Capability message - COMMON.CHECK.PD.7#2	PASS
		Check Data Objects field - COMMON.CHECK.PD.7#3	PASS

SI No	Test ID	Test Name	Test Result
		Check First PDO - COMMON.CHECK.PD.7#4 >>TEST.PD.PHY.PORT.1: Bit[9:0] Max_Current : Expected val: 2 , Obtained val:2. Packet131, 137, TEST.PD.PROT.ALL.1: Bit[9:0] Max_Current : Expected val: 2 , Obtained val:2 Bit[9:0] Max_Current for PD2: Expected val: 2 , Obtained val:2 Bit[9:0] Max_Current for PD3: Expected val: 2 , Obtained val:2. Packet201, 207, 244, 263, 291, 297, 334, 353, TEST.PD.PROT.ALL.2: Bit[9:0] Max_Current : Expected val: 2 , Obtained val:2 Bit[9:0] Max_Current for PD2: Expected val: 2 , Obtained val:2 Bit[9:0] Max_Current for PD3: Expected val: 2 , Obtained val:2. Packet185, 191, 217, 247, 279, 285, 312, 340, TEST.PD.PROT.ALL.3: Bit[9:0] Max_Current : Expected val: 2 , Obtained val:2 Bit[9:0] Max_Current for PD2: Expected val: 2 , Obtained val:2 Bit[9:0] Max_Current for PD3: Expected val: 2 , Obtained val:2. Packet190, 196, 244, 277, 283, 333, TEST.PD.PROT.ALL.4: Bit[9:0] Max_Current : Expected val: 2 , Obtained val:2. Packet220, 226, 281, 326, 332, 389, TEST.PD.PROT.ALL.5: Bit[9:0] Max_Current : Expected val: 2 , Obtained val:2. Packet99, 105, 145, 151, TEST.PD.PROT.ALL3.1: Bit[9:0] Max_Current : Expected val: 2 , Obtained val:2. Packet121, 127, 169, 175, TEST.PD.PROT.ALL3.2: Bit[9:0] Max_Current : Expected val: 2 , Obtained val:2. Packet120, 126, 168, 174, TEST.PD.PROT.ALL3.3: Bit[9:0] Max_Current : Expected val: 2 , Obtained val:2. Packet119, 125, 167, 173, TEST.PD.PROT.ALL3.4: Bit[9:0] Max_Current : Expected val: 2 , Obtained val:2. Packet119, 125, 167, 173, TEST.PD.PROT.ALL3.5: Bit[9:0] Max_Current : Expected val: 2 , Obtained val:2. Packet71, 77, TEST.PD.PROT.ALL3.6: Bit[9:0] Max_Current : Expected val: 2 , Obtained val:2. Packet71, 77,	PASS
	This report is generated using GRL-USB-PD Compliance Test Solution (Version: 1.0.0+1d68c1f7c1e3449dda8c6f1136fe3b3788240412)	TEST.PD.PROT.ALL3.5: Bit[9:0] Max_Current : Expected val: 2 , Obtained val:2. Packet71, 77, TEST.PD.PROT.ALL3.6: Bit[9:0] Max_Current : Expected val: 2 , Obtained val:2. Packet71, 77,	Page: 132

SI No	Test ID	Test Name	Test Result
		Check Fixed PDO - COMMON.CHECK.PD.7#5	PASS
		Check PPS Validation - COMMON.CHECK.PD.7#6	PASS
		Check Power Rules - COMMON.CHECK.PD.7#7	PASS

SI No	Test ID	Test Name	Test Result
		<p>Check PDO Consistency - COMMON.CHECK.PD.7#8 >>TEST.PD.PHY.PORT.1: Bit[9:0] Max_Current : Expected val: 2 , Obtained val:2. Packet131, 137, TEST.PD.PROT.ALL.1: Bit[9:0] Max_Current : Expected val: 2 , Obtained val:2 Bit[9:0] Max_Current for PD2: Expected val: 2 , Obtained val:2 Bit[9:0] Max_Current for PD3: Expected val: 2 , Obtained val:2 Packet201, 207, 244, 263, 291, 297, 334, 353, TEST.PD.PROT.ALL.2: Bit[9:0] Max_Current : Expected val: 2 , Obtained val:2 Bit[9:0] Max_Current for PD2: Expected val: 2 , Obtained val:2 Bit[9:0] Max_Current for PD3: Expected val: 2 , Obtained val:2. Packet185, 191, 217, 247, 279, 285, 312, 340, TEST.PD.PROT.ALL.3: Bit[9:0] Max_Current : Expected val: 2 , Obtained val:2 Bit[9:0] Max_Current for PD2: Expected val: 2 , Obtained val:2 Bit[9:0] Max_Current for PD3: Expected val: 2 , Obtained val:2. Packet190, 196, 244, 277, 283, 333, TEST.PD.PROT.ALL.4: Bit[9:0] Max_Current : Expected val: 2 , Obtained val:2. Packet220, 226, 281, 326, 332, 389, TEST.PD.PROT.ALL.5: Bit[9:0] Max_Current : Expected val: 2 , Obtained val:2. Packet99, 105, 145, 151, TEST.PD.PROT.ALL3.1: Bit[9:0] Max_Current : Expected val: 2 , Obtained val:2. Packet121, 127, 169, 175, TEST.PD.PROT.ALL3.2: Bit[9:0] Max_Current : Expected val: 2 , Obtained val:2. Packet120, 126, 168, 174, TEST.PD.PROT.ALL3.3: Bit[9:0] Max_Current : Expected val: 2 , Obtained val:2. Packet119, 125, 167, 173, TEST.PD.PROT.ALL3.4: Bit[9:0] Max_Current : Expected val: 2 , Obtained val:2. Packet119, 125, 167, 173, TEST.PD.PROT.ALL3.5: Bit[9:0] Max_Current : Expected val: 2 , Obtained val:2. Packet71, 77, TEST.PD.PROT.ALL3.6: Bit[9:0] Max_Current : Expected val: 2 , Obtained val:2. Packet71, 77,</p>	PASS
	This report is generated using GRL-USB-PD Compliance Test Solution (Version: 1.0.0+1d68c1f7c1e3449dda8c6f1136fe3b3788240412)	<p>173, TEST.PD.PROT.ALL3.5: Bit[9:0] Max_Current : Expected val: 2 , Obtained val:2. Packet71, 77, TEST.PD.PROT.ALL3.6: Bit[9:0] Max_Current : Expected val: 2 , Obtained val:2. Packet71, 77,</p>	Page: 134

SI No	Test ID	Test Name	Test Result
		Check PDO Sequence - COMMON.CHECK.PD.7#9	PASS
		Check Fixed PDO Voltage - COMMON.CHECK.PD.7#10	PASS
		Check Variable PDO Voltage - COMMON.CHECK.PD.7#11	PASS
		Check Battery PDO Voltage - COMMON.CHECK.PD.7#12	PASS
		Check AVS Validation - COMMON.CHECK.PD.7#13	PASS
		Common_Check_PD_8_Request_Message - COMMON.CHECK.PD.8	PASS
		Request messages fields check - COMMON.CHECK.PD.8#1	PASS
		Common_Check_PD_9_Structured_VDM - COMMON.CHECK.PD.9	PASS

SI No	Test ID	Test Name	Test Result
		Structured VDM header field check - COMMON.CHECK.PD.9#1 >>TEST.PD.PHY.ALL.1: CommandVersion [b[12:11]] Obt:0 and Exp: 0. Packet31, TEST.PD.PHY.ALL.2: CommandVersion [b[12:11]] Obt:0 and Exp: 0. Packet31, TEST.PD.PHY.ALL.3: CommandVersion [b[12:11]] Obt:0 and Exp: 0. Packet31, TEST.PD.PHY.ALL.4: CommandVersion [b[12:11]] Obt:0 and Exp: 0. Packet31, TEST.PD.PHY.ALL.6: CommandVersion [b[12:11]] Obt:0 and Exp: 0. Packet31, TEST.PD.PHY.ALL.7: CommandVersion [b[12:11]] Obt:0 and Exp: 0. Packet32, TEST.PD.PHY.ALL.8: CommandVersion [b[12:11]] Obt:0 and Exp: 0. Packet31, TEST.PD.PHY.ALL.9: CommandVersion [b[12:11]] Obt:0 and Exp: 0. Packet31, 77, TEST.PD.PHY.PORT.1: CommandVersion [b[12:11]] Obt:0 and Exp: 0. Packet31, 125, 133, 147, TEST.PD.PROT.ALL.1: Specification Revision Obt:REVISION_3_0 and Exp:REVISION_2_0. Packet203, TEST.PD.PROT.ALL.1: CommandVersion [b[12:11]] Obt:0 and Exp: 0. Packet104, 195, 203, 285, 293, 307, TEST.PD.PROT.ALL.2: Specification Revision Obt:REVISION_3_0 and Exp:REVISION_2_0. Packet187, TEST.PD.PROT.ALL.2: CommandVersion [b[12:11]] Obt:0 and Exp: 0. Packet95, 157, 179, 187, 273, 281, 295, 349, TEST.PD.PROT.ALL.3: Specification Revision Obt:REVISION_3_0 and Exp:REVISION_2_0. Packet192, TEST.PD.PROT.ALL.3: CommandVersion [b[12:11]] Obt:0 and Exp: 0. Packet97, 184, 192, 271, 279, 293, TEST.PD.PROT.ALL.4: Specification Revision Obt:REVISION_3_0 and Exp:REVISION_2_0. Packet222, TEST.PD.PROT.ALL.4: CommandVersion [b[12:11]] Obt:0 and Exp: 0. Packet102, 164, 214, 222, 320, 328, 342, 398, TEST.PD.PROT.ALL.5:	PASS
	This report is generated using ComplianceChecker v1.0.3+06a17 Exp: 0. Packet102, 164, 214, 222, 320, 328, 342, 398, TEST.PD.PROT.ALL.5	Specification Revision Obt:REVISION_3_0 and Exp:REVISION_2_0. Packet222, TEST.PD.PROT.ALL.4: CommandVersion [b[12:11]] Obt:0 and Exp: 0. Packet102, 164, 214, 222, 320, 328, 342, 398, TEST.PD.PROT.ALL.5:	Page: 136

SI No	Test ID	Test Name	Test Result
		Common_Check_PD_10_Extended_Message_Header - COMMON.CHECK.PD.10	PASS
		Check Extended Message Header - COMMON.CHECK.PD.10#1 >>TEST.PD.PROT.PORT3.1: Source_Cap_Extended message: Expected value:25, Header value:25. Packet138, TEST.PD.PROT.PORT3.2: Source_Cap_Extended message: Expected value:25, Header value:25. Packet107, TEST.PD.PROT.PORT3.3: Source_Cap_Extended message: Expected value:25, Header value:25. Packet307, 395, TEST.PD.PROT.PORT3.4: Source_Cap_Extended message: Expected value:25, Header value:25. Packet167, 220, TEST.PD.PROT.SRC3.3: Source_Cap_Extended message: Expected value:25, Header value:25. Packet47, 95, TEST.PD.PROT.SNK3.1: Source_Cap_Extended message: Expected value:25, Header value:25. Packet44, 93,	PASS
		Common_Check_PD_11_Source_Capability_Extended_Message - COMMON.CHECK.PD.11	PASS

SI No	Test ID	Test Name	Test Result
		Source capabilities extended message fields check - COMMON.CHECK.PD.11#1 >>TEST.PD.PROT.PORT3.1: EPR_Support_As_Src is not set and SPR_Source_PDP field is not in consistent with PD_Power_As_Source Expected: 5 Obtained: 5. Packet138, TEST.PD.PROT.PORT3.2: EPR_Support_As_Src is not set and SPR_Source_PDP field is not in consistent with PD_Power_As_Source Expected: 5 Obtained: 5. Packet107, TEST.PD.PROT.PORT3.3: EPR_Support_As_Src is not set and SPR_Source_PDP field is not in consistent with PD_Power_As_Source Expected: 5 Obtained: 5. Packet307, 395, TEST.PD.PROT.PORT3.4: EPR_Support_As_Src is not set and SPR_Source_PDP field is not in consistent with PD_Power_As_Source Expected: 5 Obtained: 5. Packet167, 220, TEST.PD.PROT.SRC3.3: EPR_Support_As_Src is not set and SPR_Source_PDP field is not in consistent with PD_Power_As_Source Expected: 5 Obtained: 5. Packet47, 95, TEST.PD.PROT.SNK3.1: EPR_Support_As_Src is not set and SPR_Source_PDP field is not in consistent with PD_Power_As_Source Expected: 5 Obtained: 5. Packet44, 93,	PASS
		Common_Check_PD_12_Check_Sink_Capabilities - COMMON.CHECK.PD.12	PASS

SI No	Test ID	Test Name	Test Result
		<p>Sink capabilities fields check - COMMON.CHECK.PD.12#1 >>TEST.PD.PHY.ALL.8: Mismatch in number of Data object count: PD Message: 2 and VIF: 2. Packet44, TEST.PD.PHY.ALL.8: Bit[19:10] Voltage for PD3: Expected val: 9 , Obtained val:9 Bit[9:0] Operational_Current for PD3: Expected val: 3 , Obtained val:3. Packet44, TEST.PD.PHY.ALL.8: Two Fixed PDO's has same voltage. Packet44, TEST.PD.PROT.ALL.1: Mismatch in number of Data object count: PD Message: 2 and VIF: 2. Packet117, 121, 129, 133, 135, 157, 317, 319, 324, 326, 328, 345, TEST.PD.PROT.ALL.1: Bit[19:10] Voltage for PD2: Expected val: 9 , Obtained val:9 Bit[9:0] Operational_Current for PD2: Expected val: 3 , Obtained val:3 Bit[19:10] Voltage : Expected val: 9 , Obtained val:9 Bit[9:0] Operational_Current : Expected val: 3 , Obtained val:3 Bit[19:10] Voltage for PD3: Expected val: 9 , Obtained val:9 Bit[9:0] Operational_Current for PD3: Expected val: 3 , Obtained val:3. Packet27, 29, 34, 36, 38, 40, 58, 117, 121, 129, 133, 135, 157, 225, 227, 232, 234, 236, 238, 255, 317, 319, 324, 326, 328, 345, TEST.PD.PROT.ALL.1: Two Fixed PDO's has same voltage. Packet27, 29, 34, 36, 38, 40, 58, 117, 121, 129, 133, 135, 157, 225, 227, 232, 234, 236, 238, 255, 317, 319, 324, 326, 328, 345, TEST.PD.PROT.ALL.2: Mismatch in number of Data object count: PD Message: 2 and VIF: 2. Packet108, 111, 112, 133, 136, 137, 305, 306, 307, 323, 324, 325, TEST.PD.PROT.ALL.2: Bit[19:10] Voltage : Expected val: 9 , Obtained val:9 Bit[9:0] Operational_Current : Expected val: 3 , Obtained val:3 Bit[19:10] Voltage for PD2: Expected val: 9 , Obtained val:9 Bit[9:0] Operational_Current for PD2: Expected val: 3 , Obtained val:3 Bit[19:10] Voltage for PD3: Expected val: 9 , Obtained val:9 Bit[9:0] Operational_Current for PD3: Expected val: 3 , Obtained val:3. Packet27, 28, 29, 30, 47, 48, 49, 50, 108, 111, 112, 133, 136, 137, 209, 210, 211, 212, 228, 229, 230, 231, 305, 306, 307, 323, 324, 325, TEST.PD.PROT.ALL.2: Two Fixed PDO's has same voltage. Packet27, 28, 29, 30, 47, 48, 49, 50, 108, 111, 112, 133, 136, 137, 209, 210, 211, 212, 228, 229, 230, 231, 305, 306, 307, 323, 324, 325,</p>	PASS
This report is generated using GRL-USB-PD Compliance Test Solution Ver: 1.12+11031173-3437da2091121103b211322112)			Page: 139

SI No	Test ID	Test Name	Test Result
		Common_Check_PD_13_Check_Correct_Use_of_Rp - COMMON.CHECK.PD.13 >> No AMS sequence No AMS sequence	PASS
		Rp Level Validation - COMMON.CHECK.PD.13#1	PASS
		Common_Check_PD_14_Check_Hard_Reset - COMMON.CHECK.PD.14	PASS
		Check Hard_Reset basic timing - COMMON.CHECK.PD.14#1	PASS
		Common_Check_PD_15_Check_Sink_Capabilities_Extended_Message - COMMON.CHECK.PD.15	PASS
		Sink capabilities extended message fields check - COMMON.CHECK.PD.15#1	PASS
		COMMON_CHECK_PD3_1_Check_EPR_Request_Message - COMMON.CHECK.PD3.1	PASS
		EPR_Request messages fields check - COMMON.CHECK.PD3.1#1	PASS
		COMMON_CHECK_PD3_2_Check_EPR_Mode_Message - COMMON.CHECK.PD3.2	PASS
		EPR_Mode messages fields check - COMMON.CHECK.PD3.2#1	PASS
		COMMON_CHECK_PD3_3_Check_EPR_Source_Capabilities_Message - COMMON.CHECK.PD3.3	PASS
		VIF field EPR_Supported_As_Src check - COMMON.CHECK.PD3.3#1	PASS
		First Fixed PDO consistency check - COMMON.CHECK.PD3.3#2	PASS
		Fixed PDO check - COMMON.CHECK.PD3.3#3	PASS
		Programmable Power Supply APDO check - COMMON.CHECK.PD3.3#4	PASS
		EPR PDOs power rules check - COMMON.CHECK.PD3.3#5	PASS
		EPR PDOs consistency check - COMMON.CHECK.PD3.3#6	PASS
		Extended field check - COMMON.CHECK.PD3.3#8	PASS
		Data size extended header check - COMMON.CHECK.PD3.3#9	PASS
		SPR PDO check - COMMON.CHECK.PD3.3#10	PASS
		COMMON_CHECK_PD3_4_Check_EPR_Sink_Capabilities_Message - COMMON.CHECK.PD3.4	PASS
		EPR_Sink_Capabilities fields check - COMMON.CHECK.PD3.4#1	PASS
154	2.2	Common Procedures	PASS
		COMMON_PROC_PD_2_UUT_Sent_Get_Source_Cap - COMMON.PROC.PD.2	PASS

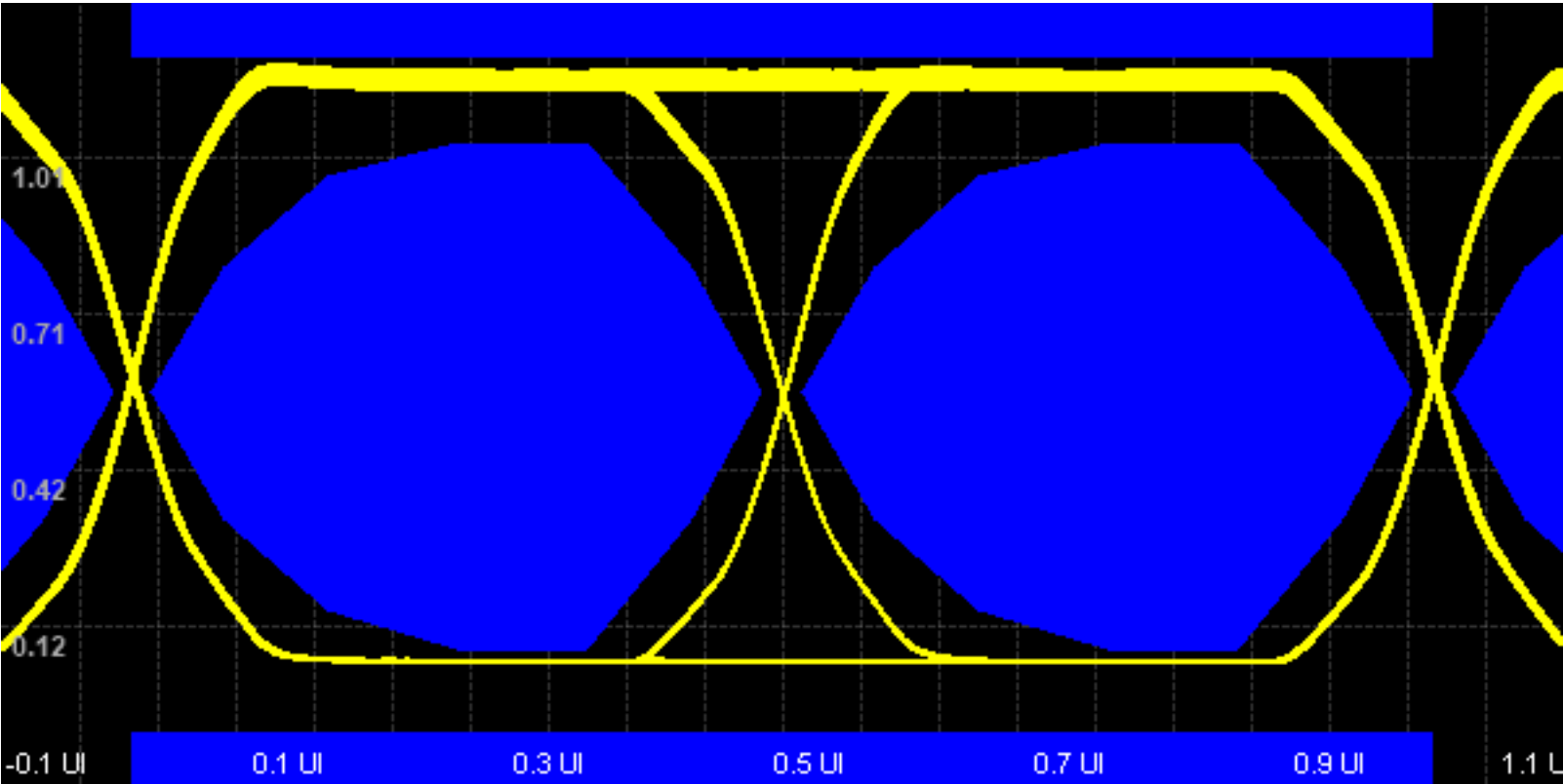
SI No	Test ID	Test Name	Test Result
		Validate Get source capabilities message initiated by DUT - COMMON.PROC.PD.2#1	PASS
		DUT's Request message validation - COMMON.PROC.PD.2#2	PASS
		COMMON_PROC_PD_3_UUT_Sent_Get_Sink_Cap - COMMON.PROC.PD.3	PASS
		Validate Get sink cap message initiated by DUT - COMMON.PROC.PD.3#1	PASS
		COMMON_PROC_PD_4_UUT_Sent_Ping - COMMON.PROC.PD.4	PASS
		Ping message initiated by DUT - COMMON.PROC.PD.4#1	PASS
		COMMON_PROC_PD_5_UUT_Sent_PR_Swap - COMMON.PROC.PD.5	PASS
		PR_Swap valid condition check - COMMON.PROC.PD.5#1	PASS
		PR_Swap init and VIF field value comparison - COMMON.PROC.PD.5#2	PASS
		PR_Swap init and VIF field value comparison - COMMON.PROC.PD.5#3	PASS
		COMMON_PROC_PD_6_UUT_Sent_VCONN_Swap - COMMON.PROC.PD.6	PASS
		Vconn_Swap valid condition check - Tester Vconn Source - COMMON.PROC.PD.6#1	PASS
		Vconn_Swap init and VIF field value comparison - COMMON.PROC.PD.6#2	PASS
		tVCONNSourceOn Timer Validation - COMMON.PROC.PD.6#3	PASS
		Vconn_Swap valid condition check - DUT Vconn Source - COMMON.PROC.PD.6#4	PASS
		COMMON_PROC_PD_7_UUT_Sent_Discover_Identity_Request - COMMON.PROC.PD.7	PASS
		Validate Discover ID request message initiated by DUT - COMMON.PROC.PD.7#1	PASS
		Structured VDM Message Header check - COMMON.PROC.PD.7#2	PASS
		Tester's VDM response check - COMMON.PROC.PD.7#3	PASS
		COMMON_PROC_PD_8_UUT_Sent_Discover_SVIDs_Request - COMMON.PROC.PD.8	PASS
		Validate Discover ID request message initiated by DUT - COMMON.PROC.PD.8#1	PASS
		Structured VDM Message Header check - COMMON.PROC.PD.8#2	PASS
		Tester's VDM response check - COMMON.PROC.PD.8#3	PASS
		COMMON_PROC_PD_9_UUT_Sent_Attention - COMMON.PROC.PD.9	PASS

SI No	Test ID	Test Name	Test Result
		Validate attention request message initiated by DUT - COMMON.PROC.PD.9#1	PASS
		Structured VDM message header check - COMMON.PROC.PD.9#2	PASS
		COMMON_PROC_PD_10_UUT_Sent_Request - COMMON.PROC.PD.10	PASS
		Validate request message initiated by DUT - COMMON.PROC.PD.10#1	PASS
		COMMON_PROC_PD_11_UUT_Sent_Source_Capabilities - COMMON.PROC.PD.11 > TEST_PD_PROT_SRC_6_Atomic_Message_Sequence_Request: Tester's request packet .Packet Index: 30 TEST_PD_PROT_SRC_6_Atomic_Message_Sequence_Request: Tester's request packet Packet Index: 80	PASS
		Validate Source capabilities message initiated by DUT - COMMON.PROC.PD.11#1	PASS
		DUT should respond with Accept - COMMON.PROC.PD.11#2	PASS
		DUT should send PS_RDY - COMMON.PROC.PD.11#3	PASS
		Wait Message - COMMON.PROC.PD.11#4	PASS
		COMMON_PROC_PD_12_UUT_Sent_DR_Swap - COMMON.PROC.PD.12	PASS
		Validate DR_Swap message initiated by DUT - COMMON.PROC.PD.12#1	PASS
		COMMON_PROC_PD_17_Tester_Sent_Vconn_swap_message - COMMON.PROC.PD.17	PASS
		VCONN present check - COMMON.PROC.PD.17#1	PASS
		PS_RDY is missing - COMMON.PROC.PD.17#2	PASS
		VCONN present check - COMMON.PROC.PD.17#3	PASS
		tVONNSourceOff timer check - COMMON.PROC.PD.17#4	PASS
		COMMON_PROC_PD3_1_Sink_Start_an_AMS - COMMON.PROC.PD3.1	PASS
		Sink Start AMS - COMMON.PROC.PD3.1#1	PASS
		COMMON_PROC_PD3_2_UUT_Sent_EPR_Source_Cap_message - COMMON.PROC.PD3.2	PASS
		Validate EPR_Source_Capabilities message initiated by UUT - COMMON.PROC.PD3.2#1	PASS
		UUT should respond with Accept - COMMON.PROC.PD3.2#2	PASS
		UUT should send PS_RDY - COMMON.PROC.PD3.2#3	PASS

SI No	Test ID	Test Name	Test Result
		COMMON_PROC_PD3_3_UUT_Sent_EPR_Get_Source_Cap - COMMON.PROC.PD3.3	PASS
		Validate EPR Get Source Capabilities message initiated by DUT - COMMON.PROC.PD3.3#1	PASS
		DUT's EPR Request message validation - COMMON.PROC.PD3.3#2	PASS
		Requested Voltage and PDP - COMMON.PROC.PD3.3#3	PASS
		COMMON_PROC_PD3_4_UUT_Sent_EPR_Request - COMMON.PROC.PD3.4	PASS
		Validate EPR Request message initiated by DUT - COMMON.PROC.PD.3.4#1	PASS
		COMMON_PROC_PD3_5_Tester_Sent_EPR_Mode_Enter - COMMON.PROC.PD3.5	PASS
		Validate EPR Enter Enter fail initiated by DUT - COMMON.PROC.PD3.5#1	PASS
		VIF Field Has Invariant PDOs check - COMMON.PROC.PD3.5#2	PASS
		UUT Request message check - COMMON.PROC.PD3.5#3	PASS
		UUT sends a wait message - COMMON.PROC.PD3.5#4	PASS
		UUT sends PSRdy Message - COMMON.PROC.PD3.5#5	PASS
		VIF specified Source Capabilities - COMMON.PROC.PD3.5#6	PASS
		Source Cap message - COMMON.PROC.PD3.5#7	PASS
		UUT EPR Mode Enter Failed - COMMON.PROC.PD3.5#8	PASS
		UUT Not Supported Message - COMMON.PROC.PD3.5#9	PASS
		UUT EPR Mode Enter Acknowledged - COMMON.PROC.PD3.5#10	PASS
		UUT VCONN Swap Message - COMMON.PROC.PD3.5#11	PASS
		UUT EPR Source Capabilities Message - COMMON.PROC.PD3.5#12	PASS
		UUT EPR Contract - COMMON.PROC.PD3.5#13	PASS
		COMMON_PROC_PD3_6_UUT_Sent_EPR_Mode_Enter - COMMON.PROC.PD3.6	PASS
		Validate EPR Mode Enter initiated by DUT - COMMON.PROC.PD3.6#1	PASS
		Validate EPR Mode Enter response - COMMON.PROC.PD3.6#2	PASS
		Tester sends a Vconn Swap message - COMMON.PROC.PD3.6#3	PASS
		Validate EPR Mode Enter failed message - COMMON.PROC.PD3.6#4	PASS
		Validate SOP' Discover_Id and EPR Mode Enter Succeeded message - COMMON.PROC.PD3.6#5	PASS

SI No	Test ID	Test Name	Test Result
		EPR_Source_Cap message - COMMON.PROC.PD3.6#6	PASS
		UUT establishes EPR contract - COMMON.PROC.PD3.6#7	PASS
		COMMON_PROC_PD3_7_Tester_Sends_EPR_KeepAlive_Message - COMMON.PROC.PD3.7	PASS
		Validate EPR_KeepAlive response message initiated by DUT - COMMON.PROC.PD3.7#1	PASS

BMC Eye Diagram



Functional Tests Result Summary:

SI No	Test ID	Test Name	Result	Details
1	TD.4.11.2	TD.4.11.2 Sink Dead Battery Test	PASS	
2	TD.4.1.1	TD.4.1.1 Initial Voltage Test	PASS	

SI No	Test ID	Test Name	Result	Details
3	TD.4.2.1	TD.4.2.1 Source Connect Sink Test	NA	Type_C_State_Machine Expected state: SRC. Obtained state: DRP
4	TD.4.2.2	TD.4.2.2 Source Connect SNKAS Test	NA	Type_C_State_Machine is not Source
5	TD.4.2.3	TD.4.2.3 Source Connect DRP	NA	Type_C_State_Machine is not Source
6	TD.4.2.4	TD.4.2.4 Source Connect Try SRC DRP	NA	Type_C_State_Machine is not Source
7	TD.4.2.5	TD.4.2.5 Source Connect Try SNK DRP	NA	Type_C_State_Machine is not Source
8	TD.4.2.6	TD.4.2.6 Source Connect Audio Accessory	NA	Type_C_State_Machine is not Source
9	TD.4.2.7	TD.4.2.7 Source Connect Debug Accessory	NA	Type_C_State_Machine is not Source
10	TD.4.2.8	TD.4.2.8 Source Connect Vconn Accessory	NA	Type_C_State_Machine is not Source TYPE_C_SOURCES_VCONN is not set to YES
11	TD.4.3.1	TD.4.3.1 Sink Connect Source Test	NA	Type_C_State_Machine is not set to sink
12	TD.4.3.2	TD.4.3.2 Sink Connect DRP Test	NA	Type_C_State_Machine is not set to sink
13	TD.4.3.3	TD.4.3.3 Sink Connect Try SRC DRP Test	NA	Type_C_State_Machine is not set to sink
14	TD.4.3.4	TD.4.3.4 Sink Connect Try SNK DRP Test	NA	Type_C_State_Machine is not set to sink
15	TD.4.3.5	TD.4.3.5 Sink.Connect.SNKAS.Test	NA	Type_C_State_Machine is not set to sink
16	TD.4.3.6	TD.4.3.6 Sink.Connect.Accessories.Test	NA	Type_C_State_Machine is not set to SNK
17	TD.4.4.1	TD.4.4.1 SNKAS Connect Source Test	NA	Type_C_State machine is not set to SNK TYPE_C_SUPPORTS_AUDIO_ACCESSORY is not set to YES TYPE_C_SUPPORTS_VCONN_POWERED_ACCESSORY is not set to YES
18	TD.4.4.2	TD.4.4.2 SNKAS Connect DRP Test	NA	Type_C_State machine is not set to SNK TYPE_C_SUPPORTS_AUDIO_ACCESSORY is not set to YES TYPE_C_SUPPORTS_VCONN_POWERED_ACCESSORY is not set to YES
19	TD.4.4.3	TD.4.4.3 SNKAS Connect Try SRC DRP Test	NA	Type_C_State machine is not set to SNK TYPE_C_SUPPORTS_AUDIO_ACCESSORY is not set to YES TYPE_C_SUPPORTS_VCONN_POWERED_ACCESSORY is not set to YES

SI No	Test ID	Test Name	Result	Details
20	TD.4.4.4	TD.4.4.4 SNKAS Connect Try SNK DRP Test	NA	Type_C_State machine is not set to SNK TYPE_C_SUPPORTS_AUDIO_ACCESSORY is not set to YES TYPE_C_SUPPORTS_VCONN_POWERED_ACCESSORY is not set to YES
21	TD.4.4.5	TD.4.4.5 SNKAS Connect SNKAS Test	NA	Type_C_State machine is not set to SNK TYPE_C_SUPPORTS_AUDIO_ACCESSORY is not set to YES TYPE_C_SUPPORTS_VCONN_POWERED_ACCESSORY is not set to YES
22	TD.4.4.6	TD.4.4.6 SNKAS Connect Audio Acc	NA	Type_C_State machine is not set to SNK TYPE_C_SUPPORTS_AUDIO_ACCESSORY is not set to YES TYPE_C_SUPPORTS_VCONN_POWERED_ACCESSORY is not set to YES
23	TD.4.4.7	TD.4.4.7 SNKAS Connect Debug Accessory	NA	Type_C_State machine is not set to SNK TYPE_C_SUPPORTS_AUDIO_ACCESSORY is not set to YES TYPE_C_SUPPORTS_VCONN_POWERED_ACCESSORY is not set to YES
24	TD.4.4.8	TD.4.4.8 SNKAS Connect PoweredAcc	NA	Type_C_State machine is not set to SNK TYPE_C_SUPPORTS_AUDIO_ACCESSORY is not set to YES TYPE_C_SUPPORTS_VCONN_POWERED_ACCESSORY is not set to YES
25	TD.4.5.1	TD.4.5.1 DRP Connect Sink Test	NA	TYPE_C_IMPLEMENTES_TRY_SNK is not set to NO
26	TD.4.5.2	TD.4.5.2 DRP Connect SNKAS Test	NA	TYPE_C_IMPLEMENTES_TRY_SNK is not set to NO
27	TD.4.5.3	TD.4.5.3 DRP Connect Source Test	NA	TYPE_C_IMPLEMENTES_TRY_SNK is not set to NO
28	TD.4.5.4	TD.4.5.4 DRP Connect DRP Test	NA	TYPE_C_IMPLEMENTES_TRY_SNK is not set to NO
29	TD.4.5.5	TD.4.5.5 DRP Connect Try SRC DRP Test	NA	TYPE_C_IMPLEMENTES_TRY_SNK is not set to NO
30	TD.4.5.6	TD.4.5.6 DRP Connect Try SNK DRP Test	NA	TYPE_C_IMPLEMENTES_TRY_SNK is not set to NO
31	TD.4.6.1	TD.4.6.1 Try SRC DRP Connect Source Test	NA	TYPE_C_IMPLEMENTES_TRY_SRC is not set to YES

SI No	Test ID	Test Name	Result	Details
32	TD.4.6.2	TD.4.6.2 Try SRC DRP Connect DRP Test	NA	TYPE_C_IMPLEMENTES_TRY_SNK is not set to YES
33	TD.4.6.3	TD.4.6.3 Try SRC DRP Connect Try SRC DRP Test	NA	TYPE_C_IMPLEMENTES_TRY_SRC is not set to YES
34	TD.4.6.4	TD.4.6.4 Try SRC DRP Connect Try SNK DRP Test	NA	TYPE_C_IMPLEMENTES_TRY_SRC is not set to YES
35	TD.4.6.5	TD.4.6.5 Try SRC DRP Connect Sink Test	NA	TYPE_C_IMPLEMENTES_TRY_SRC is not set to YES
36	TD.4.6.6	TD.4.6.6 Try SRC DRP Connect SNKAS Test	NA	TYPE_C_IMPLEMENTES_TRY_SRC is not set to YES
37	TD.4.7.1	TD.4.7.1 Try SNK DRP Connect Source Test	PASS	
38	TD.4.7.2	TD.4.7.2 Try SNK DRP Connect DRP Test	PASS	
39	TD.4.7.3	TD.4.7.3 Try SNK DRP Connect Try SRC DRP Test	PASS	
40	TD.4.7.4	TD.4.7.4 Try SNK DRP Connect Try SNK DRP Test	PASS	
41	TD.4.7.5	TD.4.7.5 Try SNK DRP Connect Sink Test	PASS	
42	TD.4.7.6	TD.4.7.6 Try SNK DRP Connect SNKAS Test	PASS	
43	TD.4.8.1	TD.4.8.1 DRP Connect Audio Acc Test	PASS	
44	TD.4.8.2	TD.4.8.2 DRP Connect Debug Acc Test	PASS	
45	TD.4.8.3	TD.4.8.3 DRP Connect Vconn Accessory Test	PASS	
46	TD.4.9.1	TD.4.9.1 Source Suspend Test	NA	DUT is not PUT_V
47	TD.4.9.2	TD.4.9.2 USB Type C Current Advertisement Test	PASS	
48	TD.4.9.3	TD.4.9.3 Source PR Swap Test	PASS	
49	TD.4.9.4	TD.4.9.4 Source Vconn Swap Test	NA	PUT is not PUT_V VIF field VCONN_SWAP_TO_OFF_SUPPORTED is not set to YES
50	TD.4.9.5	TD.4.9.5 Source Alternate Mode Test	NA	VIF field TYPE_C_IS_ALT_MODE_CONTROLLER is not set to YES
51	TD.4.10.1	TD.4.10.1 Sink Power Sub States Test	PASS	
52	TD.4.10.2	TD.4.10.2 Sink Power Precedence Test	PASS	
53	TD.4.10.3	TD.4.10.3 Sink Suspend Test	PASS	

SI No	Test ID	Test Name	Result	Details
54	TD.4.10.4	TD.4.10.4 Sink PR Swap Test	PASS	
55	TD.4.10.5	TD.4.10.5 Sink.VCONN Swap Test	NA	VCONN_SWAP_TO_ON_SUPPORTED is not set to YES
56	TD.4.10.6	TD.4.10.6 Sink Alternate Mode Test	PASS	
57	TD.4.11.1	TD.4.11.1 DR Swap Test	PASS	
58	TD.4.12.2	TD.4.12.2 Hub Port Types Test	NA	VIF field TYPE_C_PORT_ON_HUB is not set to YES
59	TD.4.1.2	TD.4.1.2 Unpowered CC Voltage Test	NA	PORT_BATTERY_POWERED is set to YES
60	TD.4.13.5	TD.4.13.5 Cable EnterUSB and Data Reset Test	NA	USB4_Supported is not set to YES Product_Type is not set to Cable

Attachment 2

Photo Documentation

Report No.: TCT250324S002

Product:

Smartphone

Type Designation:

X100

Photo 1- Front view



Photo 2- Back view



Attachment 2

Photo Documentation

Report No.: TCT250324S002

Product:

Smartphone

Type Designation:

X100

Photo 3- Input terminal view



Photo 4- Test view



---End of Attachment ---